500 mA, Very Low Dropout Bias Rail CMOS Voltage Regulator

NCP134

The NCP134 is a 500 mA VLDO equipped with NMOS pass transistor and a separate bias supply voltage (V_{BIAS}). The device provides very stable, accurate output voltage with low noise suitable for space constrained, noise sensitive applications. In order to optimize performance for battery operated portable applications, the NCP134 features low I_Q consumption. The XDFN4 1.2 mm x 1.2 mm package is optimized for use in space constrained applications.

Features

- Input Voltage Range: 0.8 V to 5.5 V
- Bias Voltage Range: 2.4 V to 5.5 V
- Fixed Voltage Versions Available
- Output Voltage Range: 0.8 V to 2.1 V (Fixed)
- ±1.5% Accuracy over Temperature, 0.5% V_{OUT} @ 25°C
- Ultra−Low Dropout: Max. 150 mV at 500 mA, 1.1 V Output, 3.3 V Bias, 85°C
- Very Low Bias Input Current of Typ. 80 μA
- Very Low Bias Input Current in Disable Mode: Typ. 0.5 μA
- Logic Level Enable Input for ON/OFF Control
- Output Active Discharge Option Available
- Stable with a 2.2 μF Ceramic Capacitor
- Available in XDFN4 − 1.2 mm x 1.2 mm x 0.4 mm Package
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Battery−powered Equipment
- Smartphones, Tablets
- Cameras, DVRs, STB and Camcorders

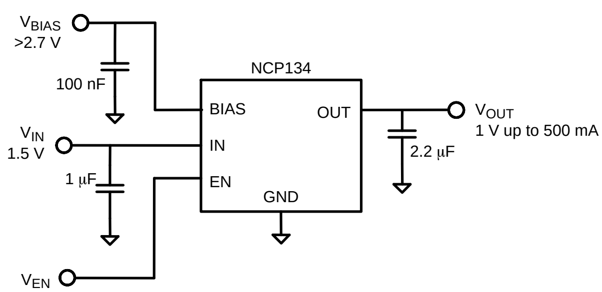

Figure 1. Typical Application Schematics

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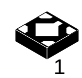
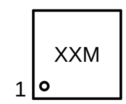


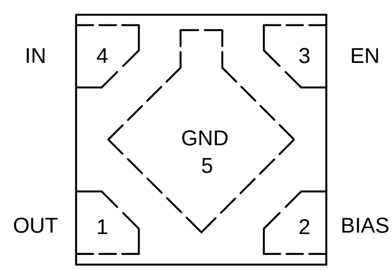
XDFN4
CASE 711BC

MARKING DIAGRAM



XX = Specific Device Code
M = Date Code

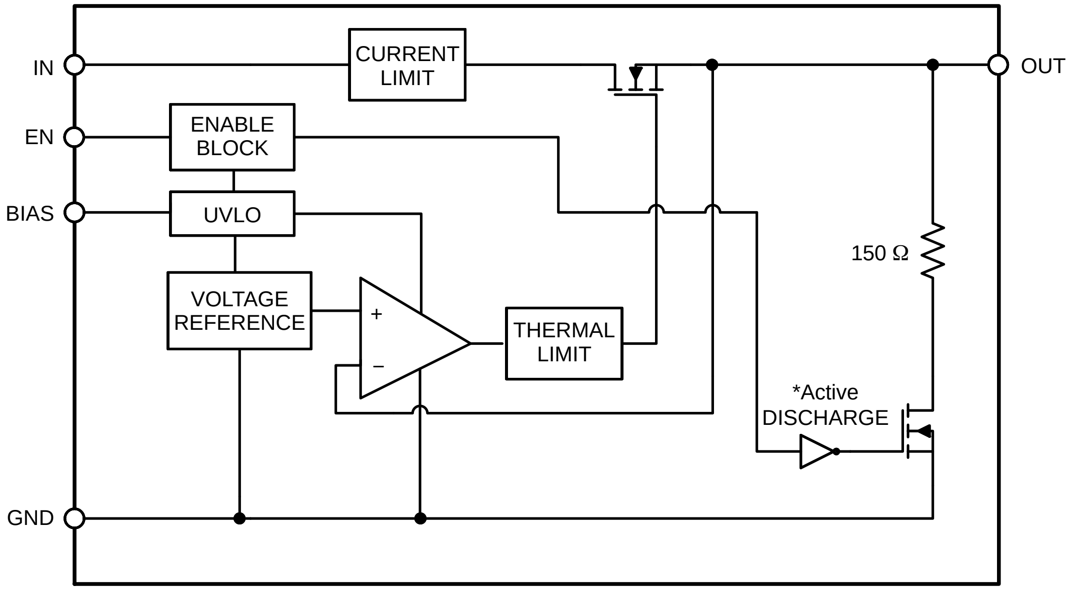
PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 10 of this data sheet.



*Active output discharge function is present only in NCP134AMXyyyTCG devices.
yyy denotes the particular output voltage option.

Figure 2. Simplified Schematic Block Diagram − Fixed Version

PIN FUNCTION DESCRIPTION

Pin No. XDFN4	Pin Name	Description
1	OUT	Regulated Output Voltage pin
2	BIAS	Bias voltage supply for internal control circuits. This pin is monitored by internal Under-Voltage Lockout Circuit.
3	EN	Enable pin. Driving this pin high enables the regulator. Driving this pin low puts the regulator into shutdown mode.
4	IN	Input Voltage Supply pin
5	GND	Ground

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage (Note 1)	V_{IN}	−0.3 to 6	V
Output Voltage	V_{OUT}	−0.3 to (V_{IN}+0.3) ≤ 6	V
Chip Enable, Bias Input	$V_{EN,}$ V_{BIAS}	−0.3 to 6	V
Output Short Circuit Duration	t_{SC}	unlimited	s
Maximum Junction Temperature	T_J	150	°C
Storage Temperature	T_{STG}	−55 to 150	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2000	V
ESD Capability, Machine Model (Note 2)	ESD_{MM}	200	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection (except OUT pin) and is tested by the following methods:
   ESD Human Body Model tested per EIA/JESD22−A114
   ESD Machine Model tested per EIA/JESD22−A115
   Latchup Current Maximum Rating tested per JEDEC standard: JESD78.

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, XDFN4 1.2 mm x 1.2 mm Thermal Resistance, Junction−to−Air (Note 3)	$R_{\theta JA}$	170	°C/W

3. This data was derived by thermal simulations for a single device mounted on the 40 mm x 40 mm x 1.6 mm FR4 PCB with 2−ounce 800 sq mm copper area on top and bottom.

ELECTRICAL CHARACTERISTICS $-40°C \le T_J \le 85°C$; V_{BIAS} = 2.7 V or (V_{OUT} + 1.6 V), whichever is greater, $V_{IN} = V_{OUT(NOM)}$ + 0.3 V, I_{OUT} = 1 mA, V_{EN} = 1 V, unless otherwise noted. C_{IN} = 1 μF, C_{OUT} = 2.2 μF. Typical values are at T_J = +25°C. Min/Max values are for $-40°C \le T_J \le 85°C$ unless otherwise noted. (Note 4)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Operating Input Voltage Range		V_{IN}	V_{OUT} + V_{DO}		5.5	V
Operating Bias Voltage Range		V_{BIAS}	(V_{OUT} + 1.40) ≥ 2.4		5.5	V
Undervoltage Lock−out	V_{BIAS} Rising Hysteresis	UVLO		1.6 0.2		V
Output Voltage Accuracy		V_{OUT}		±0.5		%
Output Voltage Accuracy	$-40°C \le T_J \le 85°C$, $V_{OUT(NOM)}$ + 0.3 V ≤ V_{IN} ≤ $V_{OUT(NOM)}$ + 1.0 V, 2.7 V or ($V_{OUT(NOM)}$ + 1.6 V), whichever is greater < V_{BIAS} < 5.5 V, 1 mA < I_{OUT} < 500 mA	V_{OUT}	−1.5		+1.5	%
V_{IN} Line Regulation	$V_{OUT(NOM)}$ + 0.3 V ≤ V_{IN} ≤ 5.0 V	$Line_{Reg}$		0.01		%/V
V_{BIAS} Line Regulation	2.7 V or ($V_{OUT(NOM)}$ + 1.6 V), whichever is greater < V_{BIAS} < 5.5 V	$Line_{Reg}$		0.01		%/V
Load Regulation	I_{OUT} = 1 mA to 500 mA	$Load_{Reg}$		1.5		mV
V_{IN} Dropout Voltage	I_{OUT} = 150 mA (Note 5)	V_{DO}		37	75	mV
	I_{OUT} = 500 mA (Note 5)	V_{DO}		140	250	
V_{IN} Dropout Voltage	NCP134AMX110TCG device, $V_{OUT(NOM)}$ = 1.1 V, V_{BIAS} = 3.3 V, I_{OUT} = 500 mA (Note 5)	V_{DO}		100	150	
V_{BIAS} Dropout Voltage	I_{OUT} = 500 mA, V_{IN} = V_{BIAS} (Notes 5, 6)	V_{DO}		1.1	1.5	V
Output Current Limit	V_{OUT} = 90% $V_{OUT(NOM)}$	I_{CL}	550	800	1000	mA
Bias Pin Operating Current	V_{BIAS} = 2.7 V	I_{BIAS}		80	110	μA
Bias Pin Disable Current	V_{EN} ≤ 0.4 V	$I_{BIAS(DIS)}$		0.5	1	μA
Vinput Pin Disable Current	V_{EN} ≤ 0.4 V	$I_{VIN(DIS)}$		0.5	1	μA
EN Pin Threshold Voltage	EN Input Voltage “H”	$V_{EN(H)}$	0.9			V
	EN Input Voltage “L”	$V_{EN(L)}$			0.4	
EN Pull Down Current	V_{EN} = 5.5 V	I_{EN}		0.3	1	μA
Turn−On Time	From assertion of V_{EN} to V_{OUT} = 98% $V_{OUT(NOM)}$. $V_{OUT(NOM)}$ = 1.0 V	t_{ON}		150		μs
Power Supply Rejection Ratio	V_{IN} to V_{OUT}, f = 1 kHz, I_{OUT} = 150 mA, $V_{IN} \ge V_{OUT}$ +0.5 V	PSRR(V_{IN})		70		dB
	V_{BIAS} to V_{OUT}, f = 1 kHz, I_{OUT} = 150 mA, $V_{IN} \ge V_{OUT}$ +0.5 V	PSRR(V_{BIAS})		80		dB
Output Noise Voltage	V_{IN} = V_{OUT} +0.5 V, $V_{OUT(NOM)}$ = 1 V, f = 10 Hz to 100 kHz	V_N		40		μV_{RMS}
Thermal Shutdown Threshold	Temperature increasing			160		°C
	Temperature decreasing			140		
Output Discharge Pull−Down	V_{EN} ≤ 0.4 V, V_{OUT} = 0.5 V, NCP134A options only	R_{DISCH}		150		Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Performance guaranteed over the indicated operating temperature range by design and/or characterization. Production tested at T_A = 25°C. Low duty cycle pulse techniques are used during the testing to maintain the junction temperature as close to ambient as possible.
5. Dropout voltage is characterized when V_{OUT} falls 3% below $V_{OUT(NOM)}$.
6. For output voltages below 0.9 V, V_{BIAS} dropout voltage does not apply due to a minimum Bias operating voltage of 2.4 V.

TYPICAL CHARACTERISTICS

At T_J = +25°C, V_{IN} = $V_{OUT(TYP)}$ + 0.3 V, V_{BIAS} = 2.7 V, V_{EN} = V_{BIAS}, $V_{OUT(NOM)}$ = 1.0 V, I_{OUT} = 500 mA, C_{IN} = 1 μF, C_{BIAS} = 0.1 μF, and C_{OUT} = 2.2 μF (effective capacitance), unless otherwise noted.

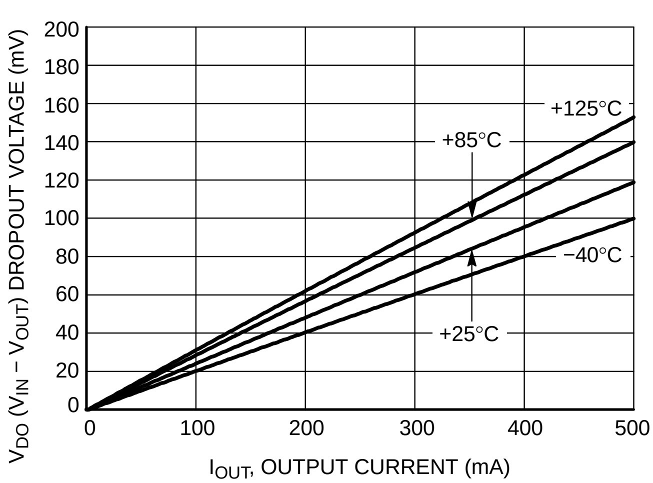


Figure 3. V_{IN} Dropout Voltage vs. I_{OUT} and Temperature T_J

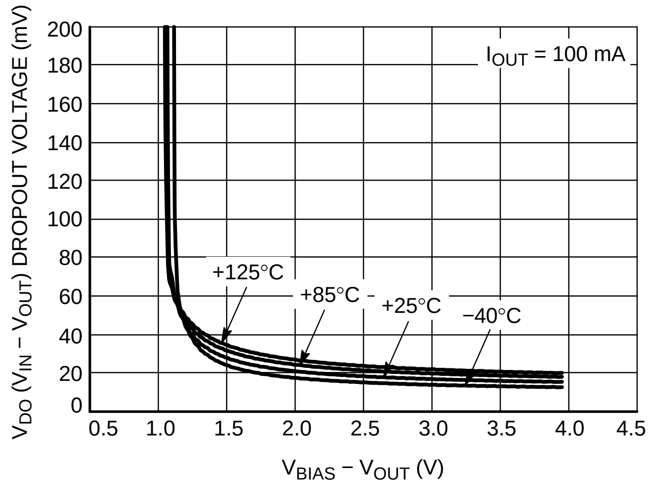


Figure 4. V_{IN} Dropout Voltage vs. (V_{BIAS} − V_{OUT}) and Temperature T_J

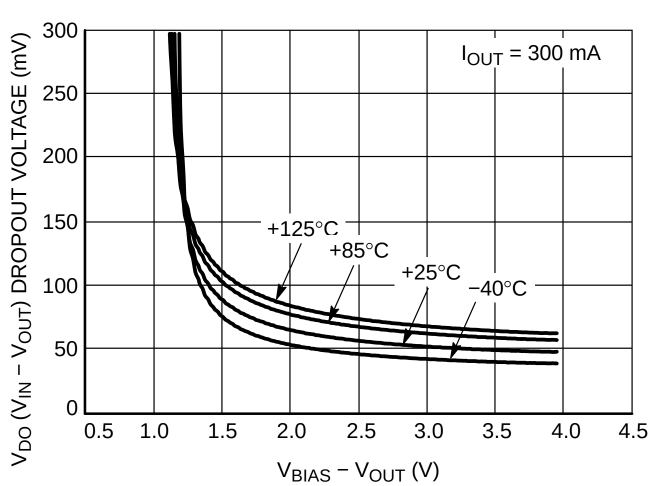


Figure 5. V_{IN} Dropout Voltage vs. (V_{BIAS} − V_{OUT}) and Temperature T_J

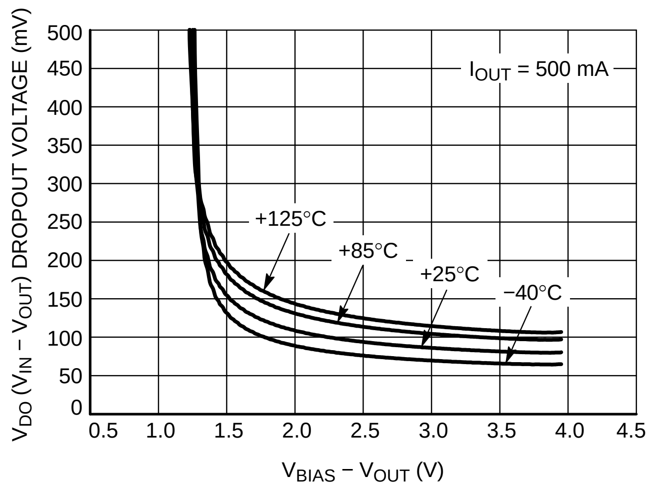


Figure 6. V_{IN} Dropout Voltage vs. (V_{BIAS} − V_{OUT}) and Temperature T_J

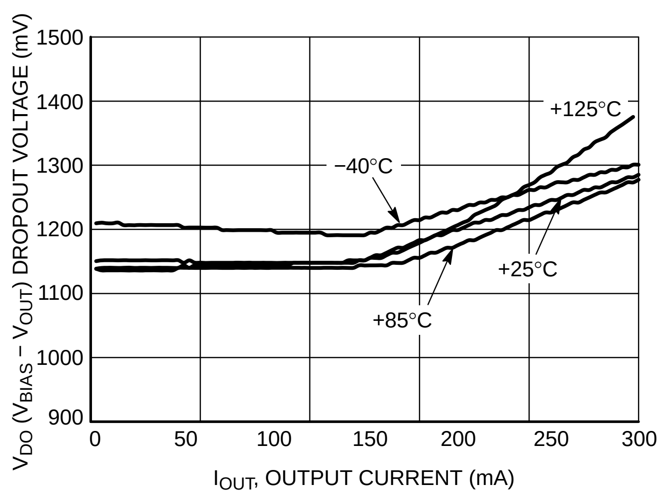


Figure 7. V_{BIAS} Dropout Voltage vs. I_{OUT} and Temperature T_J

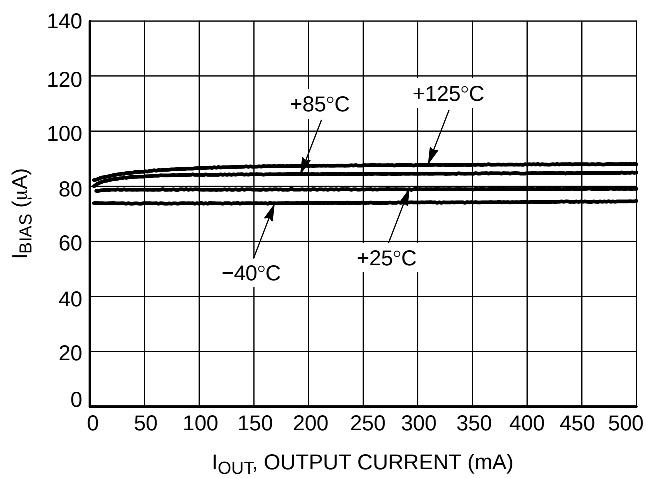


Figure 8. BIAS Pin Current vs. I_{OUT} and Temperature T_J

TYPICAL CHARACTERISTICS

At T_J = +25°C, V_{IN} = $V_{OUT(TYP)}$ + 0.3 V, V_{BIAS} = 2.7 V, V_{EN} = V_{BIAS}, $V_{OUT(NOM)}$ = 1.0 V, I_{OUT} = 500 mA, C_{IN} = 1 μF, C_{BIAS} = 0.1 μF, and C_{OUT} = 2.2 μF (effective capacitance), unless otherwise noted.

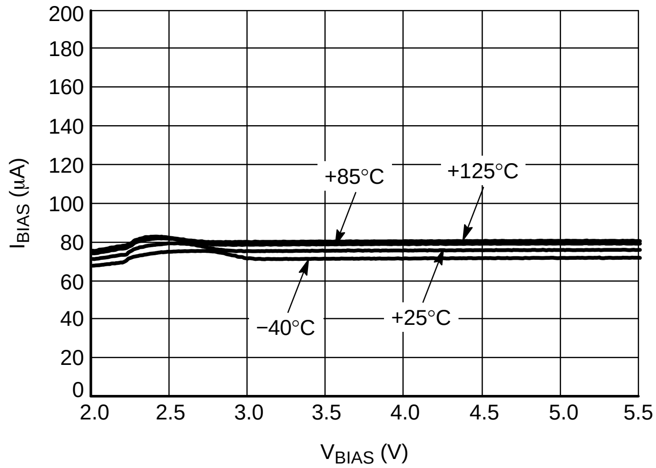


Figure 9. BIAS Pin Current vs. V_{BIAS} and Temperature T_J

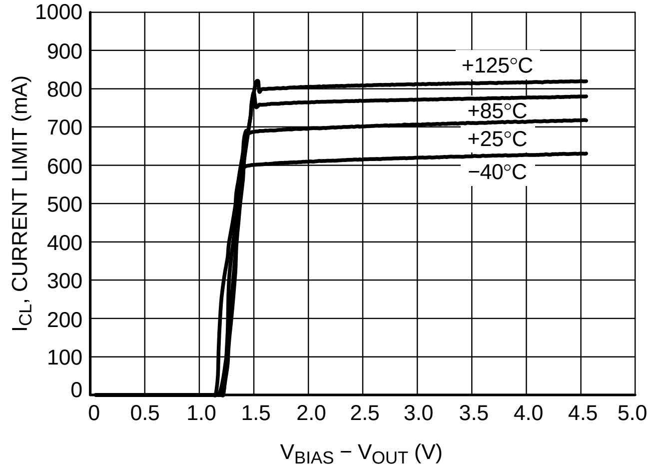


Figure 10. Current Limit vs. (V_{BIAS} − V_{OUT})

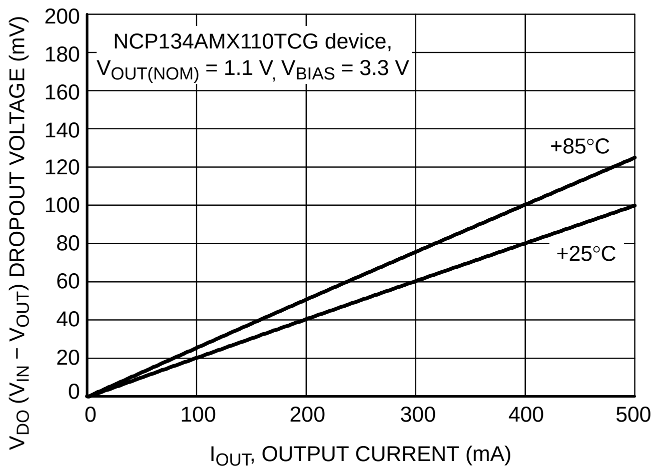


Figure 11. V_{IN} Dropout Voltage vs. I_{OUT} and Temperature T_J

TYPICAL CHARACTERISTICS

At T_J = +25°C, V_{IN} = $V_{OUT(TYP)}$ + 0.3 V, V_{BIAS} = 2.7 V, V_{EN} = V_{BIAS}, $V_{OUT(NOM)}$ = 1.0 V, I_{OUT} = 500 mA, C_{IN} = 1 µF, C_{BIAS} = 0.1 µF, and C_{OUT} = 2.2 µF (effective capacitance), unless otherwise noted.

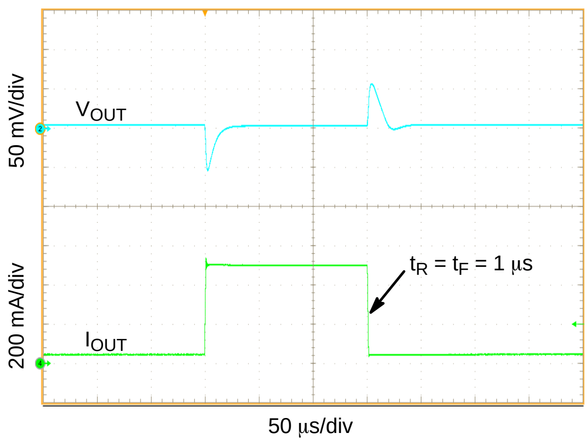


Figure 12. Load Transient Response, I_{OUT} = 50 mA to 500 mA, C_{OUT} = 10 µF

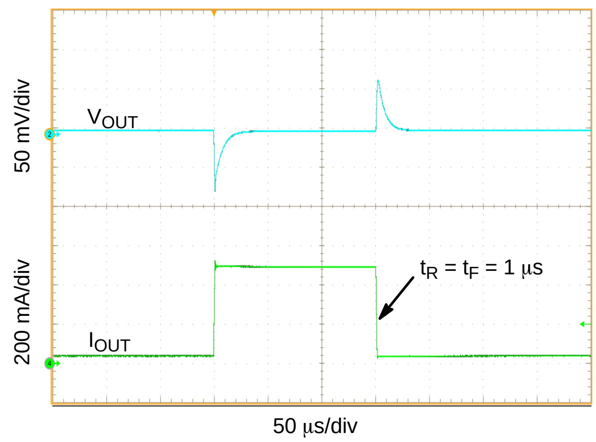


Figure 13. Load Transient Response, I_{OUT} = 50 mA to 500 mA, C_{OUT} = 2.2 µF

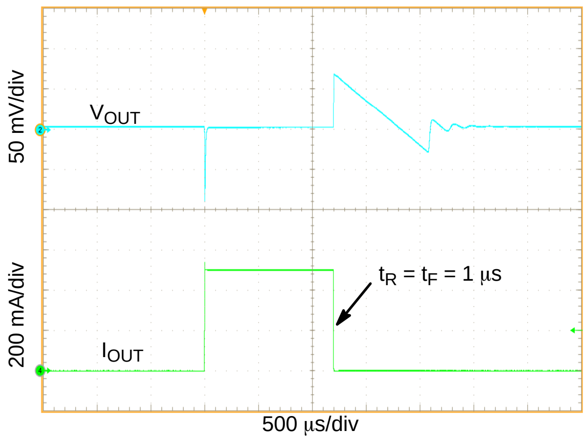


Figure 14. Load Transient Response, I_{OUT} = 1 mA to 500 mA, C_{OUT} = 10 µF

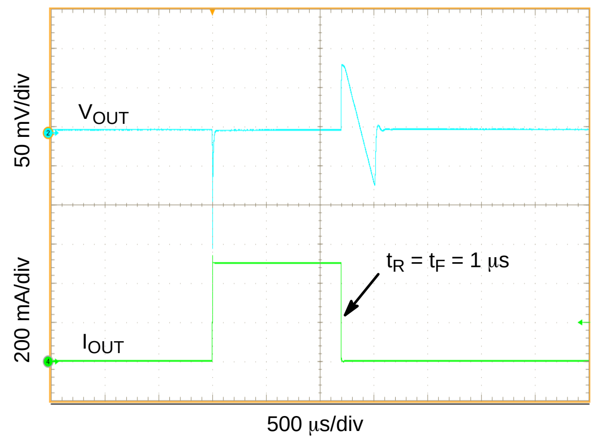


Figure 15. Load Transient Response, I_{OUT} = 1 mA to 500 mA, C_{OUT} = 2.2 µF

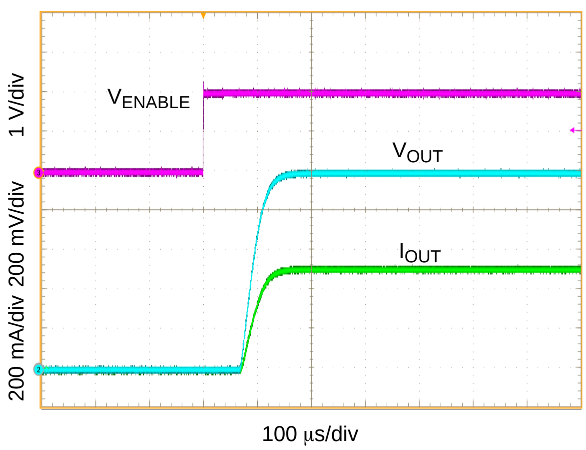


Figure 16. Enable Turn−on Response, Output Resistive Load 500 mA, C_{OUT} = 10 µF

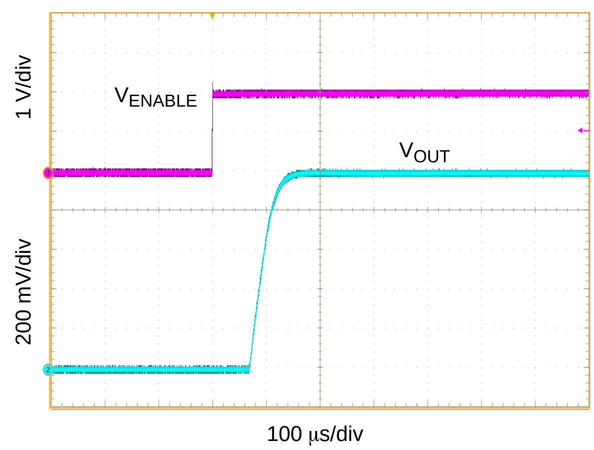


Figure 17. Enable Turn−on Response, I_{OUT} = 0 mA, C_{OUT} = 2.2 µF

TYPICAL CHARACTERISTICS

At T_J = +25°C, $V_{IN} = V_{OUT(TYP)}$ + 0.3 V, V_{BIAS} = 2.7 V, $V_{EN} = V_{BIAS}$, $V_{OUT(NOM)}$ = 1.0 V, I_{OUT} = 500 mA, C_{IN} = 1 μF, C_{BIAS} = 0.1 μF, and C_{OUT} = 2.2 μF (effective capacitance), unless otherwise noted.

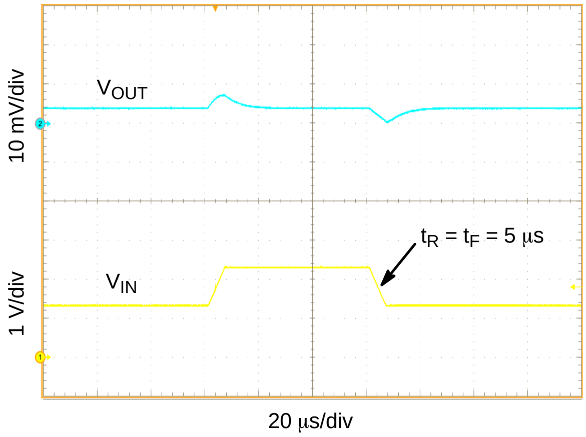


Figure 18. V_{IN} Line Transient Response, V_{IN} = 1.3 V to 2.3 V, I_{OUT} = 100 mA, C_{OUT} = 10 μF

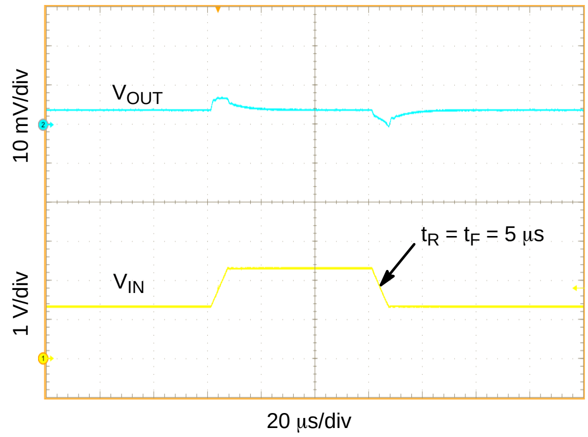


Figure 19. V_{IN} Line Transient Response, V_{IN} = 1.3 V to 2.3 V, I_{OUT} = 100 mA, C_{OUT} = 2.2 μF

APPLICATIONS INFORMATION

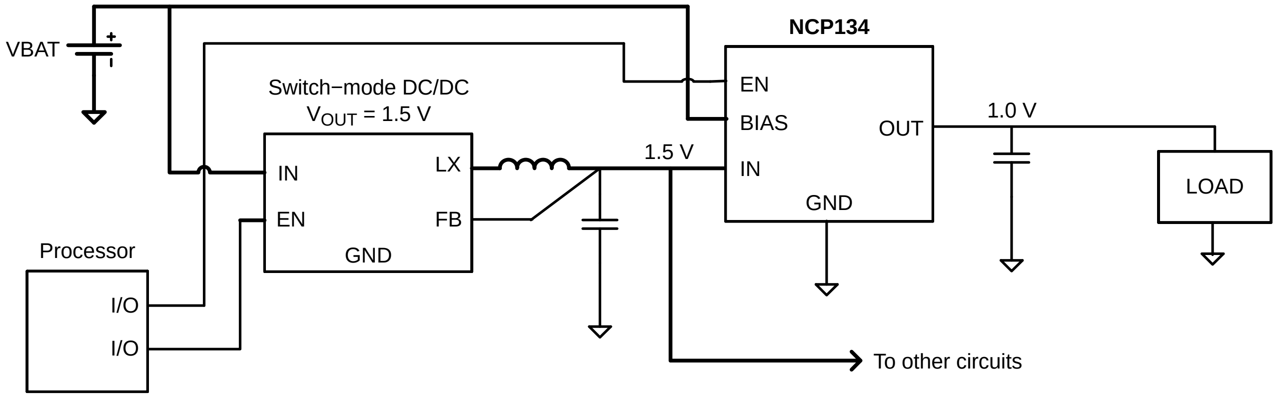


Figure 20. Typical Application: Low−Voltage DC/DC Post−Regulator with ON/OFF Functionality

The NCP134 dual−rail very low dropout voltage regulator is using NMOS pass transistor for output voltage regulation from V_{IN} voltage. All the low current internal control circuitry is powered from the V_{BIAS} voltage.

The use of an NMOS pass transistor offers several advantages in applications. Unlike PMOS topology devices, the output capacitor has reduced impact on loop stability. Vin to Vout operating voltage difference can be very low compared with standard PMOS regulators in very low Vin applications.

The NCP134 offers smooth monotonic start-up. The controlled voltage rising limits the inrush current.

The Enable (EN) input is equipped with internal hysteresis. NCP134 Voltage linear regulator Fixed version is available.

Dropout Voltage

Because of two power supply inputs V_{IN} and V_{BIAS} and one V_{OUT} regulator output, there are two Dropout voltages specified.

The first, the V_{IN} Dropout voltage is the voltage difference ($V_{IN} – V_{OUT}$) when V_{OUT} starts to decrease by percent specified in the Electrical Characteristics table. V_{BIAS} is high enough; specific value is published in the Electrical Characteristics table.

The second, V_{BIAS} dropout voltage is the voltage difference ($V_{BIAS} – V_{OUT}$) when V_{IN} and V_{BIAS} pins are joined together and V_{OUT} starts to decrease.

Input and Output Capacitors

The device is designed to be stable for ceramic output capacitors with Effective capacitance in the range from 2.2 μF to 10 μF. The device is also stable with multiple capacitors in parallel, having the total effective capacitance in the specified range.

In applications where no low input supplies impedance available (PCB inductance in V_{IN} and/or V_{BIAS} inputs as example), the recommended $C_{IN} = 1$ μF and $C_{BIAS} = 0.1$ μF or greater. Ceramic capacitors are recommended**.** For the best performance all the capacitors should be connected to the NCP134 respective pins directly in the device PCB copper layer, not through vias having not negligible impedance.

When using small ceramic capacitor, their capacitance is not constant but varies with applied DC biasing voltage, temperature and tolerance. The effective capacitance can be much lower than their nominal capacitance value, most importantly in negative temperatures and higher LDO output voltages. That is why the recommended Output capacitor capacitance value is specified as Effective value in the specific application conditions.

Enable Operation

The enable pin will turn the regulator on or off. The threshold limits are covered in the electrical characteristics table in this data sheet. If the enable function is not to be used then the pin should be connected to V_{IN} or V_{BIAS}.

Current Limitation

The internal Current Limitation circuitry allows the device to supply the full nominal current and surges but protects the device against Current Overload or Short.

Thermal Protection

Internal thermal shutdown (TSD) circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When TSD activated , the regulator output turns off. When cooling down under the low temperature threshold, device output is activated again. This TSD feature is provided to prevent failures from accidental overheating.

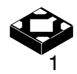
Activation of the thermal protection circuit indicates excessive power dissipation or inadequate heatsinking. For reliable operation, junction temperature should be limited to +125°C maximum.

ORDERING INFORMATION

Device	Nominal Output Voltage	Marking	Option	Package	Shipping†
NCP134AMX080TCG	0.80 V	GG	Output Active Discharge	XDFN4 (Pb−Free)	3000 / Tape & Reel
NCP134AMX085TCG	0.85 V	GL			
NCP134AMX090TCG	0.90 V	GF			
NCP134AMX100TCG	1.00 V	GA			
NCP134AMX105TCG	1.05 V	GC			
NCP134AMX110TCG	1.10 V	GD			
NCP134AMX120TCG	1.20 V	GE			
NCP134AMX135TCG	1.35 V	GJ			
NCP134AMX150TCG	1.50 V	GH			
NCP134AMX180TCG	1.80 V	GK			

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

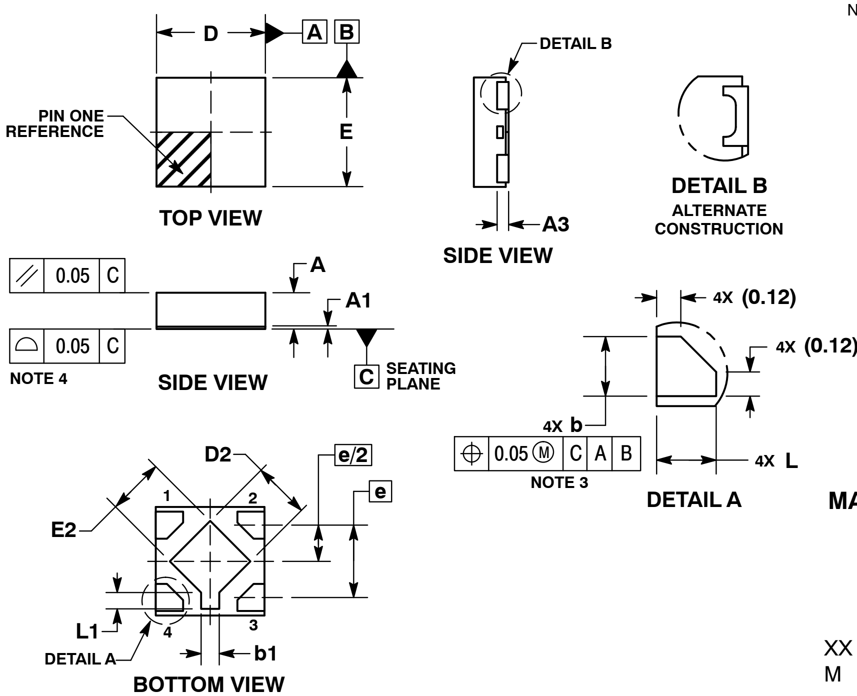
To order other package and voltage variants, please contact your ON Semiconductor sales representative



SCALE 4:1

XDFN4 1.2x1.2, 0.8P
CASE 711BC
ISSUE O

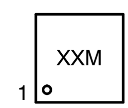
DATE 15 SEP 2015



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 mm FROM THE TERMINAL TIPS.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.35	0.45
A1	0.00	0.05
A3	0.13 REF	
b	0.25	0.35
b1	0.15	0.25
D	1.15	1.25
D2	0.58	0.68
E	1.15	1.25
E2	0.58	0.68
e	0.80 BSC	
L	0.25	0.35
L1	0.13	0.23

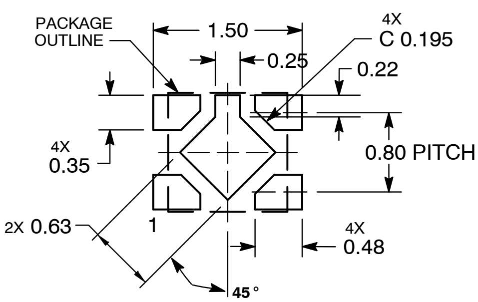
GENERIC MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking.
Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED MOUNTING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	XDFN4, 1.2X1.2, 0.8P	PAGE 1 OF 1

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