NCP373

Overvoltage Up to +30 V and Down to -30 V with Load Switch Function

NCP373 is an over−voltage and over−current protection device. From IN to VBUS , the part acts as a load switch protection, with programmable current regulation. The current protection is externally adjustable, up to 400 mA or 1300 mA, depending on selected version.

Additional voltage protection is available, from VBUS to IN. Due to built−in low $R_{DS(on)}$ NMOS FET, the host system is protected against positive and negative voltages up to ±28 V.

The embedded over−current and over−voltage protection allow the device to sustain extreme conditions from short circuit on USB connector, or defective WA or USB port.

Because to the NCP373 using internal NMOS, the system cost and the PCB area of the application board are minimized.

NCP373 provides a negative going flag ($\overline{FLAG}$) output, which alerts the system that a fault has occurred.

Features

- Adjustable Over−current
- Over−voltage Protection Up to 28 V and Down to −28 V
- Logic pins $\overline{EN}$ and $\overline{DIR}$
- Thermal Shutdown
- On−chip low $R_{DS(on)}$ NMOS Transistors
- Over−voltage Lockout (OVLO)
- Soft−start
- Real Shutdown Mode
- Alert $\overline{FLAG}$ Output
- Compliance to IEC61000−4−2 (Level 4)
  - 8 kV (Contact)
  - 15 kV (Air)
- ESD Ratings: Machine Model = B
  Human Body Model = 2
- 12 Leads LLGA 3X3 mm Package
- These are Pb−Free Devices

Typical Applications

- USB ports
- Tablets
- Set Top Box
- Cell Phones

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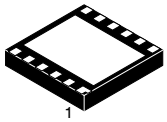
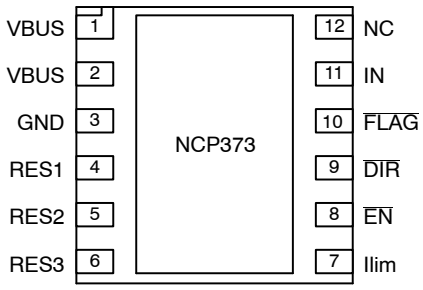


12 PIN LLGA
MU SUFFIX
CASE 513AK

MARKING DIAGRAM

A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)



(Top View)

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 9 of this data sheet.

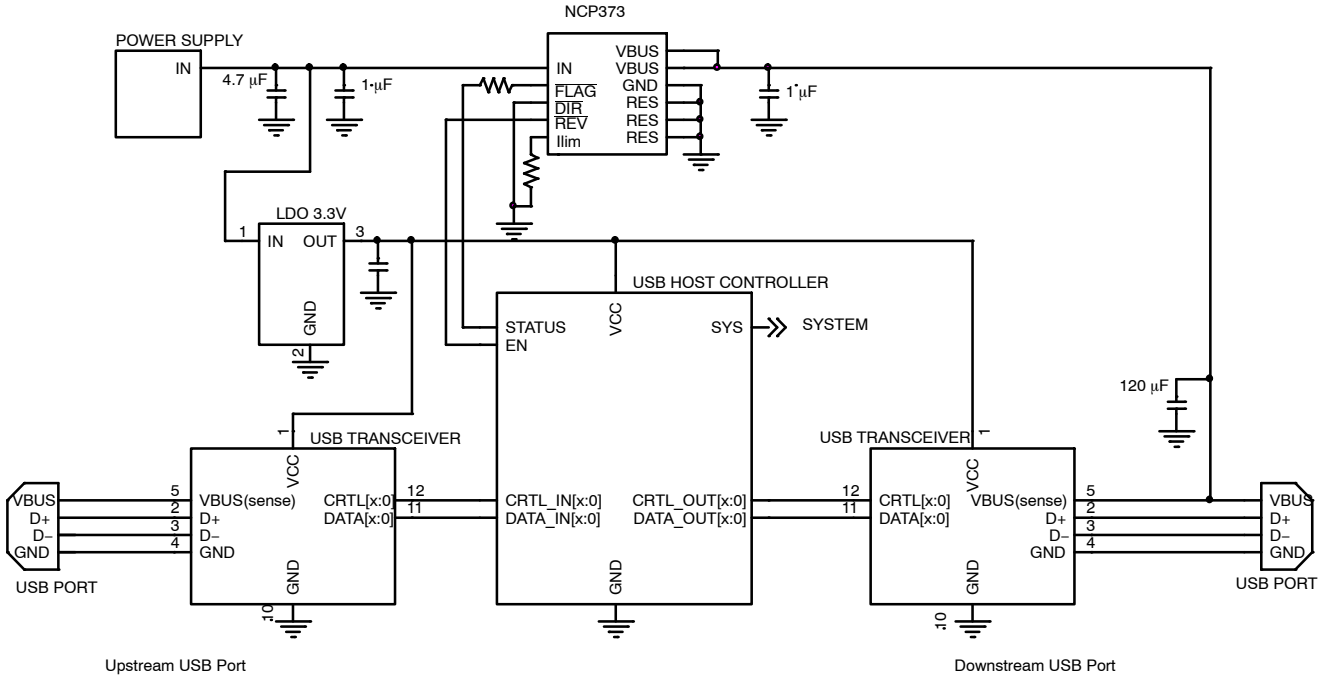


Figure 1. Typical Host Application Circuit

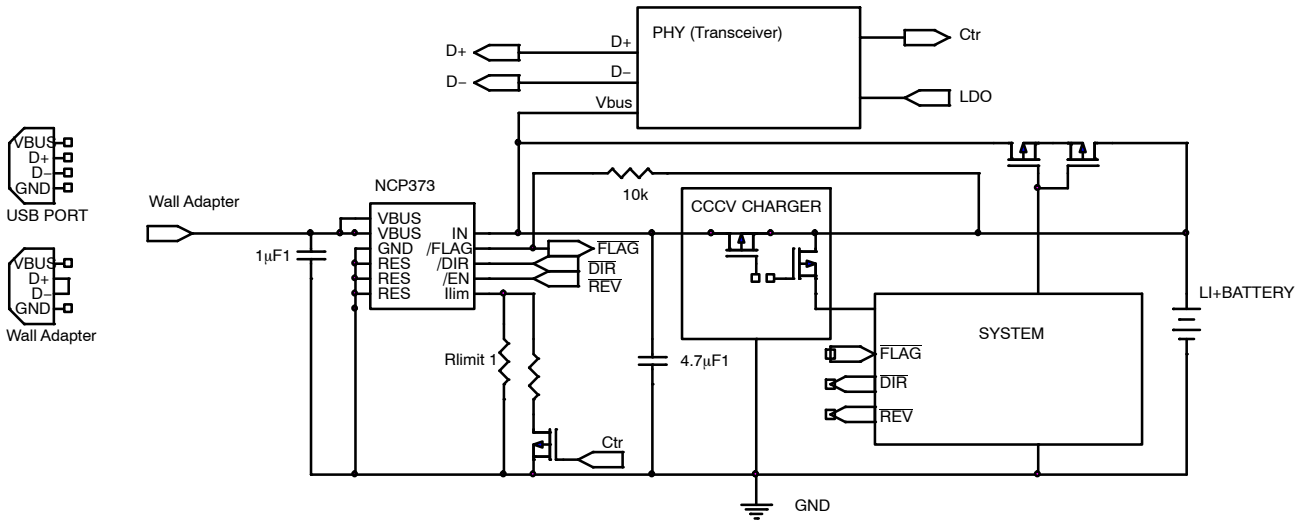


Figure 2. Typical Portable Application Circuit

FUNCTIONAL BLOCK DIAGRAM

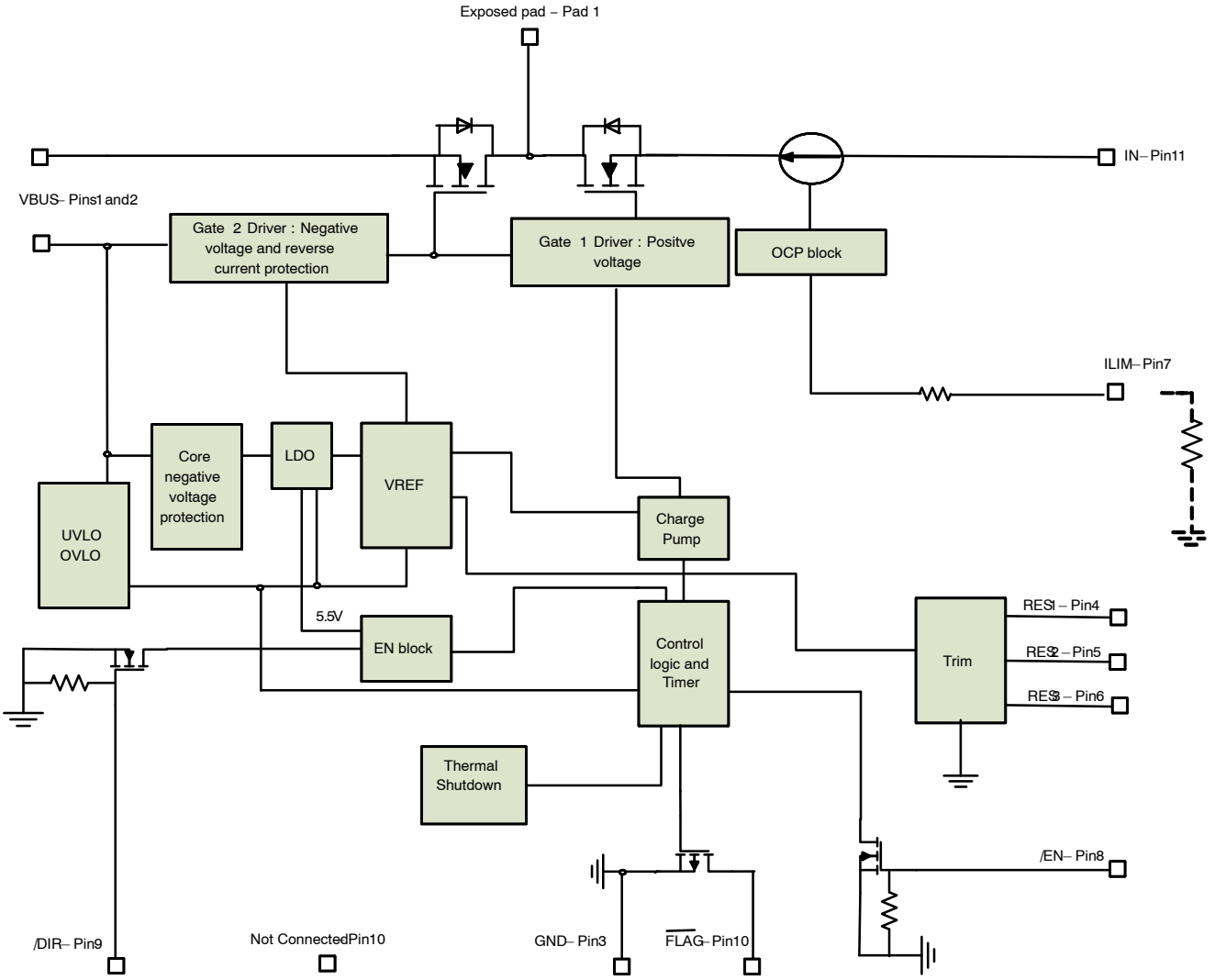


Figure 3. Functional Block Diagram

PIN FUNCTION DESCRIPTION

Pin	Pin Name	Type	Description
1,2	VBUS	POWER	VBUS voltage pins: must be hardwired together on the PCB. These pins are connected to the VBUS connector, and are protected against positive and negative overvoltage events. A 1 μF low ESR ceramic capacitor, or larger, must be connected between these pins and GND.
3	GND	POWER	Ground
4	RES1	INPUT	Reserved pin. Must be connected to GND potential and used for IC test.
5	RES2	INPUT	Reserved pin. Must be connected to GND potential and used for IC test.
6	RES3	INPUT	Reserved pin. Must be connected to GND potential and used for IC test.
7	Ilim	OUTPUT	Current Limit Pin. This pin provides the reference, based on the internal band−gap voltage reference, to limit the over current, across internal N−MOSFET. A 0.1% tolerance resistor shall be used to get the highest accuracy of the Over Current Limit.

PIN FUNCTION DESCRIPTION

Pin	Pin Name	Type	Description
8	$\overline{EN}$	INPUT	Enable Pin. In combination with $\overline{DIR}$, the internal NMOSes are turned on if Battery is applied on the IN pins. (See logic table) In enable mode, the internal Over−Current protection is activated from IN to VBUS. When enable mode is disabled, the NCP373 current consumption, into IN pin, is drastically decreased to limit current leakage of the self powered devices.
9	$\overline{DIR}$	INPUT	Direct Mode pin. This pin can be used, in combination with Enable pin, for the front end protection applications like wireless devices. In this case, the part can be used as +/− OVP only. See logic table.
10	$\overline{FLAG}$	OUTPUT	Fault indication pin. This pin allows an external system to detect fault condition. The $\overline{FLAG}$ pin goes low when input voltage exceeds OVLO threshold or drops below UVLO threshold (charging mode), charge current from IN to VBus exceeds current limit or internal temperature exceeds thermal shutdown limit. Since the $\overline{FLAG}$ pin is open drain functionality, an external pull up resistor to VBat must be added (10 kΩ minimum value).
11	IN	POWER	IN pin. In Front end application this pin is connected to CCCV device input or PMIC input. In host application, this pin is connected to upstream DCDC. This pin is used as power supply of the core and current from IN to VBUS is then limited to the external
12	NC	NA	Not internally connected. Can be connected to any potential.
13	PAD1	POWER	Drain connection of the back to back MOSFET's. This exposed pad mustn't be connected to any other potential and must be used for thermal dissipation of the internal MOSFETs.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Minimum Voltage (VBus to GND)	$Vmin_{VBUS}$	−30	V
Minimum Voltage (All others to GND)	V_{min}	−0.3	V
Maximum Voltage (VBus to GND)	$Vmax_{VBUS}$	30	V
Maximum Voltage (IN to GND)	$Vmax_{IN}$	10	V
Maximum Voltage (VBus to Vin)	$Vmax_{VBUS-VIN}$	±30	V
Maximum Voltage (All others to GND)	V_{max}	7	V
Maximum DC current NCP373MU04TXG Charge Mode Vbus Mode NCP373MU13TXG Charge Mode Vbus Mode	I_{in}	 500 500 2 1.5	 mA mA A A
Thermal Resistance, Junction−to−Air, (Note 1)	$R_{\theta JA}$	200	°C/W
Operating Ambient Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Junction Operating temperature	T_J	150	°C
ESD Withstand Voltage (IEC 61000−4−2) Human Body Model (HBM), Model = 2, (Note 2) Machine Model (MM) Model = B, (Note 3)	Vesd	15 kV air, 8 kV contact 2000 V 200 V	kV V V
Moisture Sensitivity	MSL	Level 1	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. The $R_{\theta JA}$ is highly dependent on the PCB heat sink area (connected to PAD1). See PCB recommendation paragraph.
2. Human Body Model, 100 pF discharged through a 1.5 kΩ resistor following specification JESD22/A114.
3. Machine Model, 200 pF discharged through all pins following specification JESD22/A115.

ELECTRICAL CHARACTERISTICS Min / Max limits values (−40°C < T_A < +85°C) and IN = +5 V (Unless otherwise noted). Typical values are T_A = +25°C

Characteristics	Symbols	Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{in}		2.5		5.5	V
Vbus Voltage Range	Vvbus	All modes	−28		28	V
		All modes IN = 5 V	−23			
Under Voltage Lockout Threshold	UVLO	Vbus falls down UVLO threshold Disable, Charge mode and Enhance Modes	2.6	2.7	2.8	V
Under Voltage Lockout Hysteresis	$UVLO_{hyst}$	Vbus rises up UVLO threshold + $UVLO_{hyst}$	45	60	75	mV
Over voltage Lockout threshold	OVLO	Vbus rises up OVLO threshold	5.6	5.77	5.9	V
Over Voltage Lockout Hysteresis	$OVLO_{hyst}$	Vbus falls down to OVLO − $OVLO_{hyst}$	45	65	90	mV
Vbus versus IN Resistance IN versus Vbus Resistance	R_{Dson}	Vbus = 5 V, or IN = 5 V Direct Mode, Load connected to V_{out} NCP373MU04TXG NCP373MU13TXG		 200 130	 300 220	mΩ
Quiescent Current	Idd_{IN}	No load. Vbus mode, Vin= 5 V		200	315	μA
Standby Current	Idd_{STD}	No load, IN = 5 V. Standby mode, No Vbus		0.02	1	μA
Current limit	I_{OCP}	IN = 5 V, Load on Vbus, Vbus mode R_{ILIM} = 0 Ω NCP373MU04TXG NCP373MU13TXG	 330 1100	 400 1300	 470 1500	mA
$\overline{FLAG}$ Output Low Voltage	Vol_{flag}	Fault mode Sink 1 mA on $\overline{FLAG}$ pin			400	mV
$\overline{FLAG}$ Leakage Current	$\overline{FLAG}_{leak}$	$\overline{FLAG}$ level = 5.5 V		1		nA
$\overline{DIR}$ Voltage High	V_{ih}		1.2			V
$\overline{DIR}$ Voltage Low	Vol				0.4	V
$\overline{DIR}$ Leakage current	$\overline{DIR}_{leak}$	$\overline{DIR}$ = 5.5 V		300		nA
$\overline{EN}$ Voltage High	V_{ih}		1.2			V
$\overline{EN}$ Voltage Low	V_{ol}				0.4	V
$\overline{EN}$ Leakage current	EN_{leak}	$\overline{EN}$ = 5.5 V		300		nA
Thermal Shutdown temperature	T_{SD}			150		°C
Thermal Shutdown Hysteresis	T_{SDHYST}			30		°C

TIMINGS

Vbus MODE

Start Up Delay	Ton_{Vbus}	IN ≥ 2.5 V, from $\overline{EN}$ = 1.2 to 0.4 to Vbus ≥ 0.3 V Vbus Mode	0.6	1.2	1.8	ms
$\overline{FLAG}$ going up Delay	$Tstart_{vbus}$	From IN ≥ 0.3 V $\overline{FLAG}$ = 1.2 V, Vbus Mode	0.6	1.2	1.8	ms
Rearming Delay	t_{RRD}	IN > .2.5 V, R_{in} = 1 Ω Vbus Mode, after fault	15	30	45	ms
Over Current Regulation Time	t_{reg}	IN > 2.6, Vbus > 0.3 V Vbus Mode	0.5	1.2	1.8	ms
OCP delay time	t_{OCP}	From I Vbus > I_{lim}, 1 A/1 μs		5		μs

NOTE: Electrical parameters are guaranteed by correlation across the full range of temperature.

ELECTRICAL CHARACTERISTICS Min / Max limits values (−40°C < T_A < +85°C) and IN = +5 V (Unless otherwise noted). Typical values are T_A = +25°C

Characteristics	Symbols	Conditions	Min	Typ	Max	Unit
TIMINGS						
Vbus MODE						
Vbus Disable time	$T_{VbusDIS}$	From $\overline{EN}$ = 0.4 V to 1.2 V, to Vbus < 0.3 V. IN = 5 V		2.5		µs
Turn off delay	t_{off}	From IN > OVLO to Vbus ≤ 0.3 V Vin increasing from 5 V to 8 V at 3 V/µs		1.5	5	µs
CHARGING MODE						
Start Up Delay	t_{on}	From Vbus > UVLO to IN = 0.3 V , charging mode	15	30	45	ms
$\overline{FLAG}$ going up Delay	t_{start}	From IN>0.3V to $\overline{FLAG}$ = 1.2 V	15	30	45	ms
Turn off delay	t_{off}	From Vbus > OVLO to IN ≤ 0.3 V Vin increasing from 5 V to 8V at 3V/µs		1.5	5	µs
Alert delay	t_{stop}	From Vbus > OVLO to $\overline{FLAG}$ ≤ 0.4 V See Figures 3and 9 Vin increasing from 5 V to 8 V at 3 V/µs		1.5		µs
Disable time	t_{dis}	$\overline{EN}$ = 1.2 V, From $\overline{DIR}$ = 0.4 to 1.2 V to IN ≤ 0.3 V		2.5		µs

NOTE: Electrical parameters are guaranteed by correlation across the full range of temperature.

TYPICAL OPERATING CHARACTERISTICS

Operation

The NCP373acts as an over−voltage in charge mode, when wall adapter or Vbus cable is connected to Vbus pin of the device. The downstream system (transceiver, CCCV charger..) are protected up to +30 V if charging voltage exceeds OVLO threshold (5.77 V). Thanks to a back to back architecture, the Vbus pin is also protected against reverse polarity connection, coming from wrong USB cables. This negative protection acts down to −30 V.

In *disable mode* ($\overline{EN}$ = 1, $\overline{DIR}$ = 1), there is no current consumption on IN pin and MSOFETs are turned off (Vbus cable disconnected)

The NCP373 provides over−current from IN to Vbus by selecting Vbus mode.

To active Vbus mode (USB port on), the $\overline{EN}$ pin must be tied low. In this case, MOSFET are turned on and current is measure in the branch. If the sinking current on the Vbus pin is above the programmed current on Ilim pin (can be programmed up to 400 mA), the Vbus current is regulated around Iocp during treg time. If the overload is present at the end of this timer, the MOSFET are turned off and automatic rearming cycle is activated. With T_{reg}/T_{rrd} cycle until overload is present.

Over−voltage Lockout (OVLO)

To protect the connected system on IN pins, from external over−voltage coming from USB connector or Wall Adapter, through Vbus pin , the device has a built−in over−voltage lock out (OVLO) circuit. During over−voltage condition, the output remains disabled until the input voltage exceeds OVLO (Vbus pin).

The OVLO comparator is available in all modes.

Additional OVLO thresholds ranging from OVLO can be manufactured. Please contact your ON Semiconductor representative for further information.

$\overline{FLAG}$ output is tied to low until Vin is higher than OVLO. This circuit has a built−in hysteresis to provide noise immunity to transient conditions.

Over−Current protection (OCP)

This device integrates over current protection function, from IN to Vbus port (400 mA version and 1300 mA version).

That means the current across the internal NMOS is regulated when the value, set by external R_{lim} resistor, exceeds I_{limit} during an internal timer.

An internal resistor is placed in series with the pin allowing to have a maximum OCP value when I lim pin is directly connected to GND.

By adding external resistors in series with I lim and GND, the OCP value is decreased. The Rlim tolerance is important to keep a good accuracy. So a value between 0.1% and 1% won't have an impact on the OCP accuracy. Nevertheless, the higher R_{lim} value, the lower Over current protection accuracy.

Indeed, the current is measured by a voltage comparator on a serial resistance. If this voltage drop comes very small, the offset of the internal comparator will have an impact on

the accuracy. So a division by more than three times with Rlim will degrade drastically the overcurrent accuracy.

The current limit calculation formula for the NCP373MU04TXG is:

$$R_{LIM04} = \left(\frac{11521}{I_{OCP}}\right) - 29035 \quad \Omega$$

The current limit calculation formula for the NCP373MU13TXG is:

$$R_{LIM13} = \left(\frac{37717}{I_{OCP}}\right) - 29035 \quad \Omega$$

During over current event, NMOSes are opened and $\overline{FLAG}$ output is tied to low, allowing the µController to take into account the fault event and then disable reverse charge path.

VBus Mode

To access to the Vbus mode, $\overline{DIR}$ pin must be tied to high (>1.2) and $\overline{EN}$ must be tied from high to low (< 0.4 V).

In that case, the core of the NCP373 will be supplied by the IN, with a 2.5 V minimum voltage and 5.5 V maximum voltage.

In this state, OCP, OVLO and thermal modes are available.

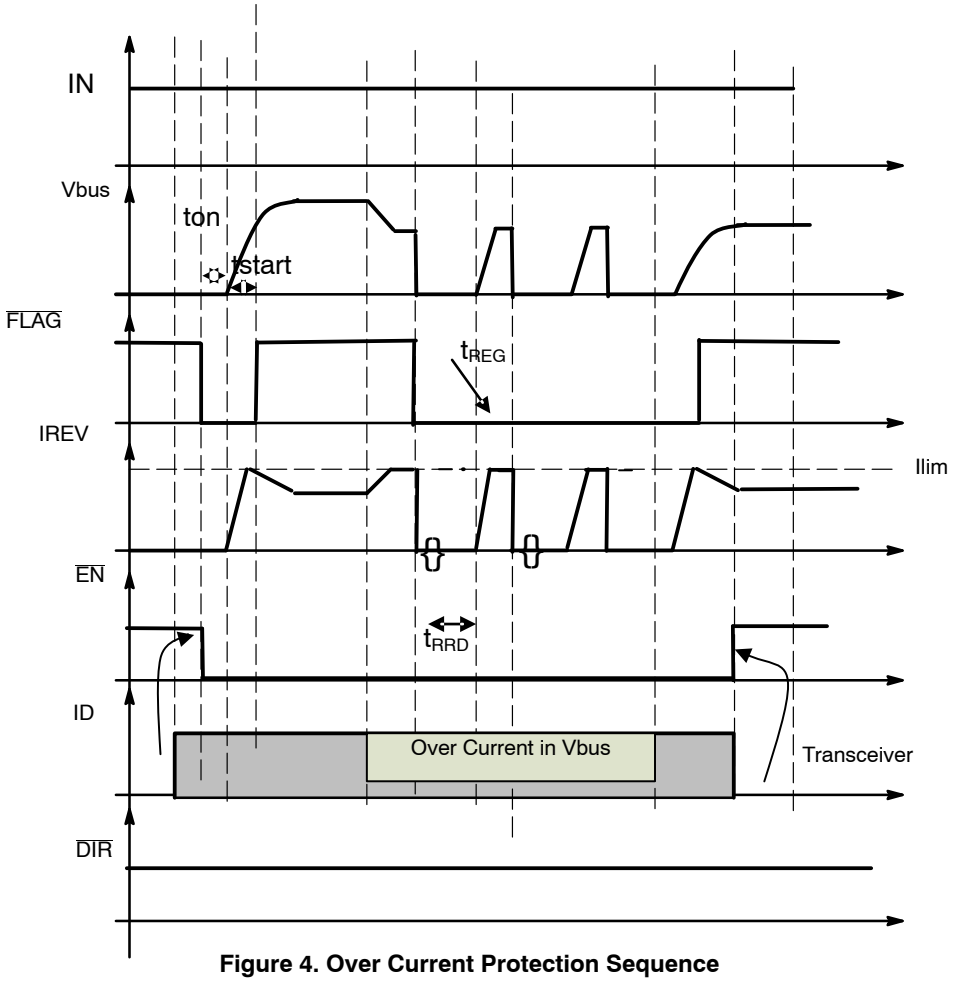


Figure 4. Over Current Protection Sequence

In Vbus Mode, $\overline{FLAG}$ pin remains available, allowing the µcontroller to have a status regarding over−voltage condition, over−current condition or thermal shutdown condition.

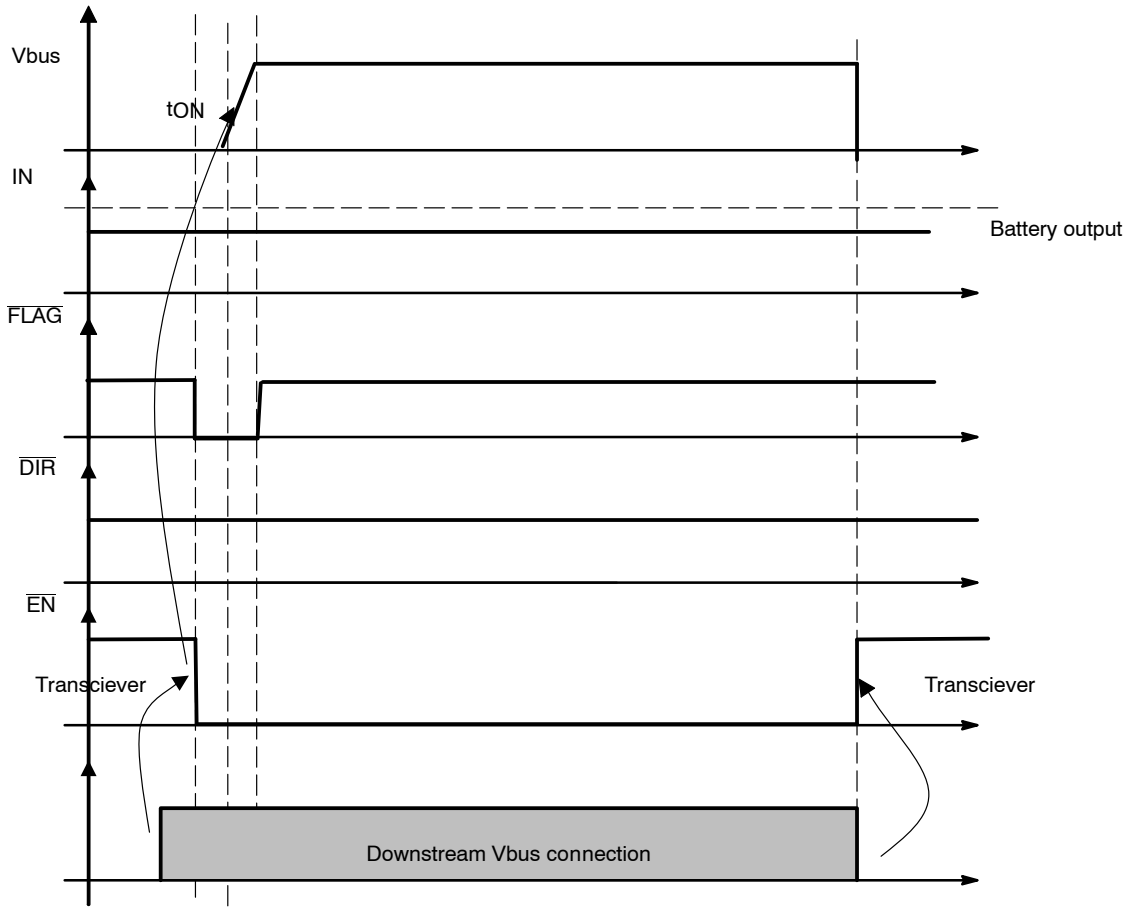


Figure 5. $\overline{\text{FLAG}}$ Status in Vbus Mode

Logic Inputs

To enable Charge operation (Charge Mode), the $\overline{\text{DIR}}$ pin shall be forced to low and $\overline{\text{EN}}$ to high. A high level on the $\overline{\text{DIR}}$ pin disconnects IN pin from Vbus pin. $\overline{\text{DIR}}$ does not overdrive an OVLO or UVLO fault ($\overline{\text{FLAG}}$ status is still available).

Table 1. TABLE SELECTION OF CHARGE MODES

			Protection		
$\overline{\text{DIR}}$	$\overline{\text{EN}}$	MODE	OVP @ VBUS (+28 V, −28 V, OVLO 5.77 V)	OCP (IN to VBUS)	OCP (VBUS to IN)
0	0	NA	NA	NA	NA
0	1	Charge	Yes	NA	NA
1	0	VBUS	Yes	Yes	NA
1	1	Disable	Yes (out off)	NA	NA

Negative Voltage and Reverse Current

The device protects the system connected on IN pin from negative voltage occurring on Vbus pin, down to −28 V. When a negative voltage occurs, the IN pins are disconnected from Vbus pins. This negative protection is available in all modes

Thermal Shutdown Protection

In case of internal overheating, the integrated thermal shutdown protection allows to open the internal MOSFET in order to instantaneously decrease the device temperature. The thermal threshold has been set at 150°C. $\overline{\text{FLAG}}$ is then tied to low to inform the MCU.

As the thermal hysteresis is 30°C, the MOSFET will be closed as soon the device temperature falls down to 120°C.

If the fault event is still present, the temperature increase one more time and engages the thermal shutdown one more time until fault event disappeared.

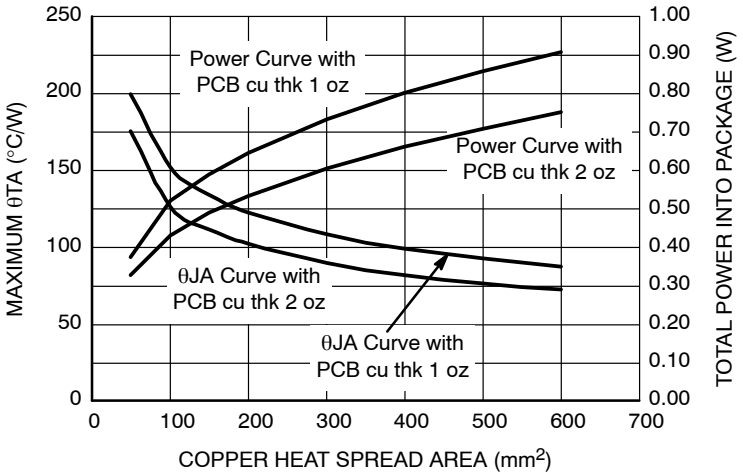


Figure 6. Copper Heat Spread Area

ESD Tests

The NCP373 conforms to the IEC61000−4−2, level 4 on the Input pin. A 1 μF (I.E Murata GRM188R61E105KA12D) must be placed close to the IN pins. If the IEC61000−4−2 is not a requirement, a 100 nF/25 V must be placed between IN and GND.

The above configuration supports 15 kV (Air) and 8 kV (Contact) at the input per IEC61000−4−2 (level 4).

Please refer to Figure 7 for the IEC61000−4−2 electrostatic discharge waveform.

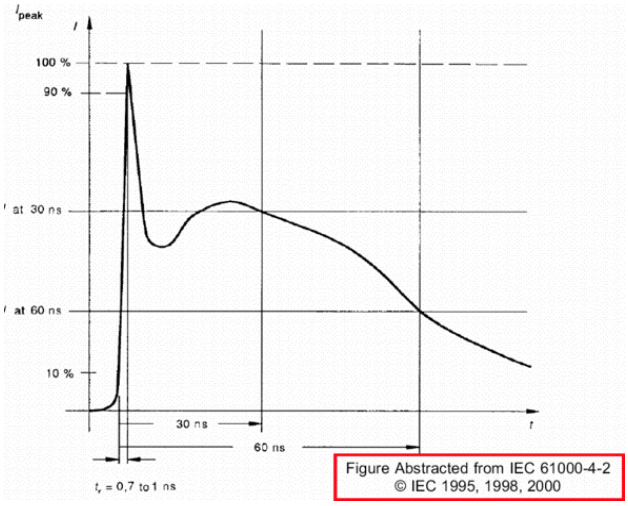


Figure 7. I_{peak} = f(t)/IEC61000−4−2

PCB Recommendations

The under PAD1 of the NCP373 package shall be connected to an isolated PCB area to increase the heat transfer if necessary for an application standpoint.

In any case, the PAD1 shall be not connected to any other potential or GND than the isolated extra copper surface.

Following figure shows copper area according to $R_{\theta JA}$ and allows the design of the transfer plane connected to PAD1.

ORDERING INFORMATION

Device	Marking	Order Current Limit	Package	Shipping†
NCP373MU04TXG	NCAI	400 mA	LLGA12 3 x 3 mm (Pb−Free)	3000 Tape / Reel
NCP373MU13TXG	NC13	1300 mA	LLGA12 3 x 3 mm (Pb−Free)	3000 Tape / Reel

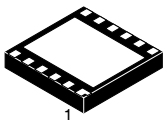
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

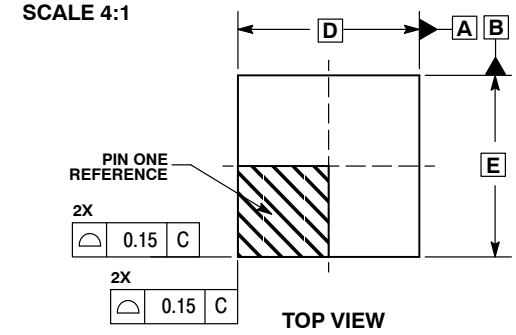
ON Semiconductor®

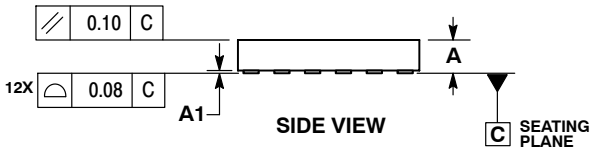
LLGA12 3x3, 0.5P
CASE 513AK−01
ISSUE O

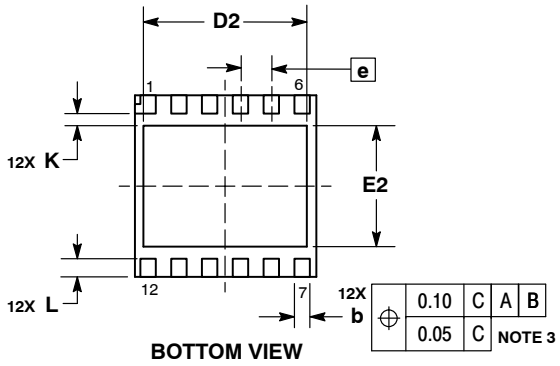
DATE 28 JUN 2007



SCALE 4:1







NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

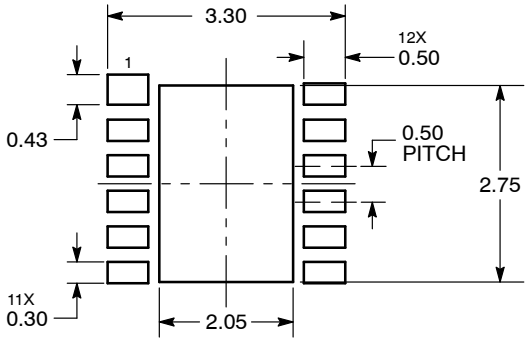
	MILLIMETERS	
DIM	MIN	MAX
A	0.50	0.60
A1	0.00	0.05
b	0.20	0.30
D	3.00 BSC	
D2	2.60	2.80
E	3.00 BSC	
E2	1.90	2.10
e	0.50 BSC	
K	0.20	---
L	0.25	0.35

GENERIC MARKING DIAGRAM*

A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	98AON24833D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	12 PIN LLGA, 3 X 3 X 0.55T, 0.5P	PAGE 1 OF 1

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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