



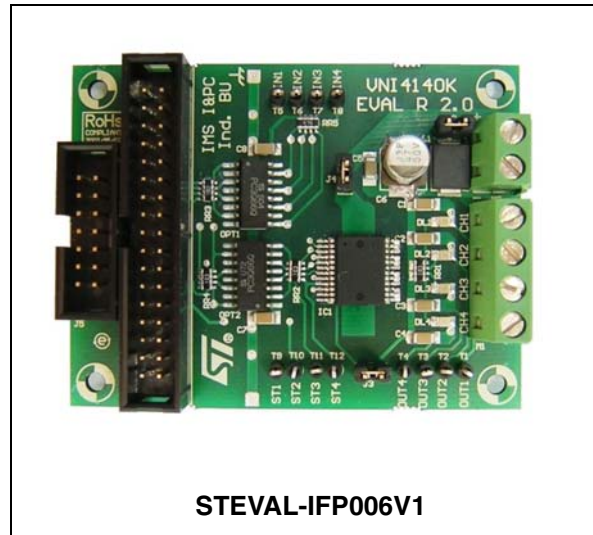
# STEVAL-IFP006V1

Quad high side smart power solid state relay evaluation board  
using the VNI4140K

Data Brief

## Features

- Shorted load protections
- Junction over-temperature protection
- Case over-temperature protection for thermal independence of the channels
- Thermal case shut-down non-simultaneous restart for the various channels
- Protection against loss of ground
- Current limitation
- Undervoltage shut-down
- Open drain diagnostic outputs
- 3.3 V CMOS/TTL compatible inputs
- Fast demagnetization of inductive loads
- Conforms to IEC 61131-2

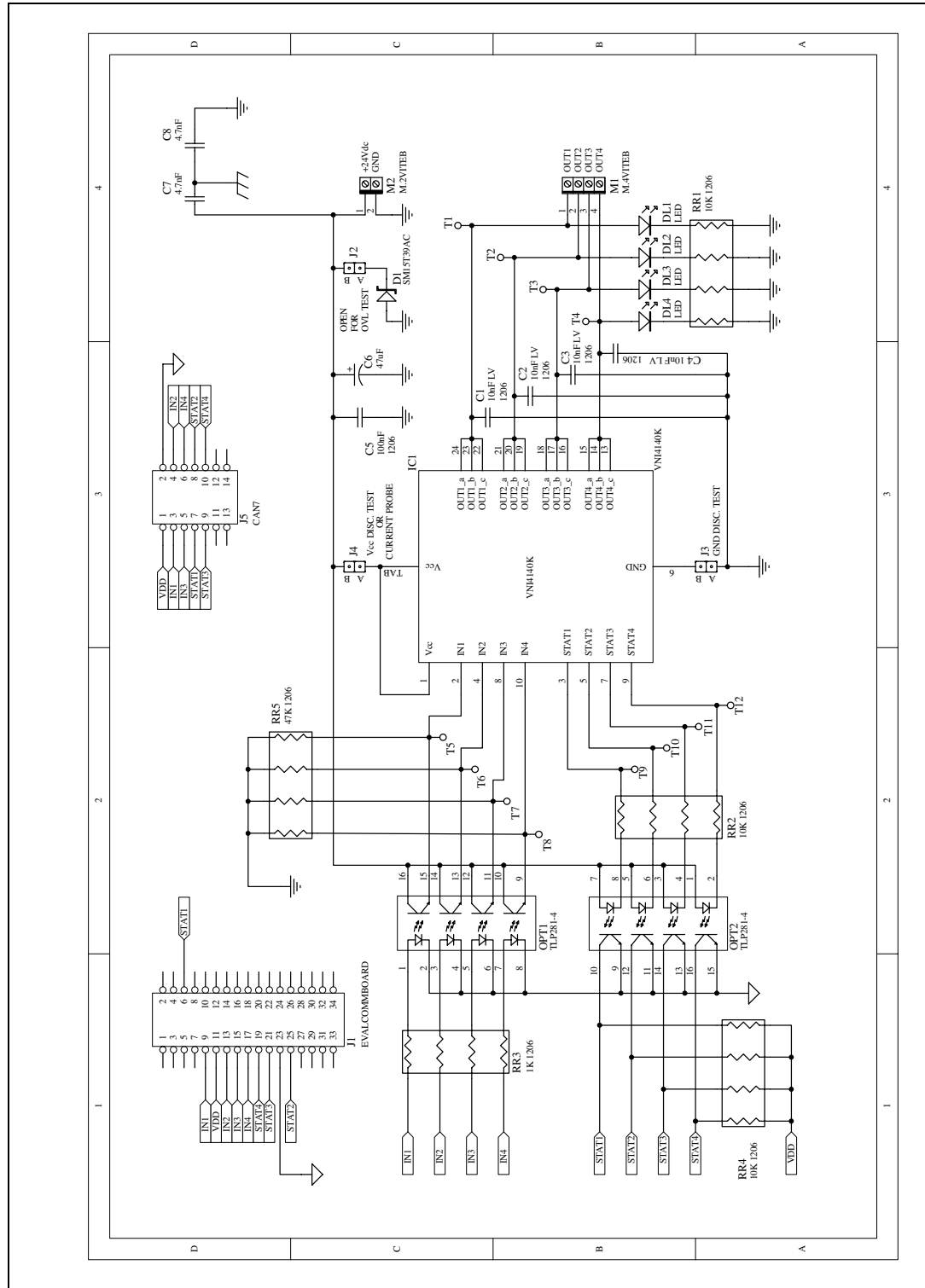


## Description

The purpose of this design is to demonstrate the features of the VNI4140K quad high side smart power solid state relay. The application offers robustness and complies with EMC industrial standards. It implements short-circuit/overload protection and thermal management as well, achieving best-in-class MTBF values. The reference design is suitable for use in programmable logic controllers (PLCs) as well as to drive generic loads which require up to 0.7 A of nominal current (the typical current limitation is 0.7 - 1.7 A). Thanks to the very low  $R_{DS(on)}$  (only 80 m $\Omega$  typ. @ 25 °C per channel) the device allows very low power consumption during operation and for this reason making it an ideal solution for IP65 / IP67 requirements. The device is compliant with IEC 61131-2 (Programmable Controllers International Standard).

# 1 Board schematic

Figure 1. Schematic diagram

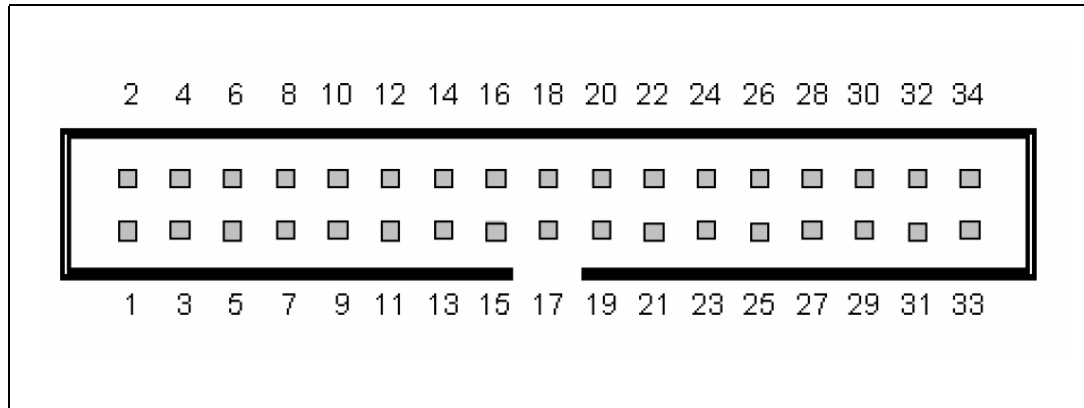


## 2 Connectors

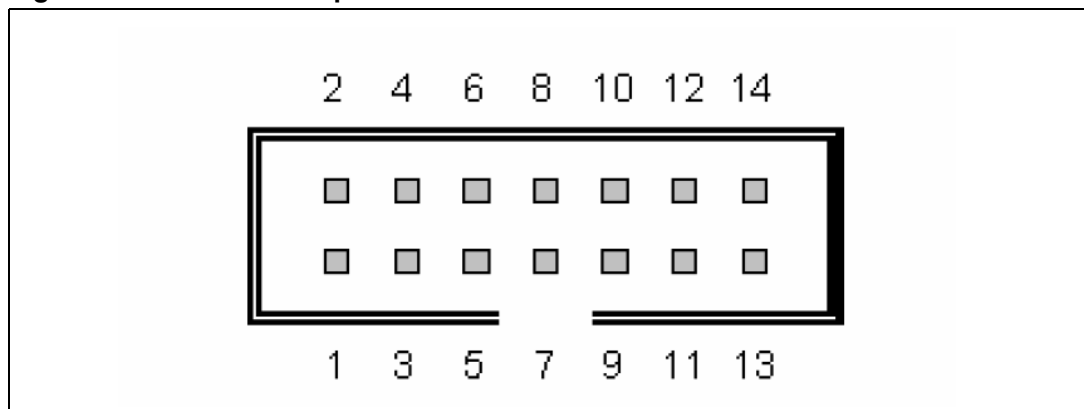
This evaluation board uses two input header connectors, one screw drives the four-channels output connector and one screw drives the two-channel supply connector.

Both input connectors, J5 and J1, provide the same bidirectional evaluation board signalization guaranteeing the maximum compatibility with existing ST tools, such as the ST7540 FSK powerline transceiver evaluation board (see AN2451 ) and similar.

**Figure 2. J1 connector pinout**



**Figure 3. J5 connector pinout**



**Table 1. Connector J1 and J5 pinout mapping**

J1 pin number	J5 pin number	Signal	Type
11	1	Vdd	5/3.3 V supply voltage
23	2	GND	Signal ground
9	3	IN1	Input channel 1
13	4	IN2	Input channel 2
15	5	IN3	Input channel 3
17	6	IN4	Input channel 4
6	7	STAT1	Status channel 1
25	8	STAT2	Status channel 2
21	9	STAT3	Status channel 3
19	10	STAT4	Status channel 4

### 3 Bill of materials

**Table 2. Evaluation board bill of material**

Designator	Part	Description
RR1	10 k $\Omega$ x 4	SMD resistor pack 1206 format
RR2	10 k $\Omega$ x 4	SMD resistor pack 1206 format
RR3	1 k $\Omega$ x 4	SMD resistor pack 1206 format
RR4	10 k $\Omega$ x 4	SMD resistor pack 1206 format
RR5	47 k $\Omega$ x 4	SMD resistor pack 1206 format
C1	10 nF LV	SMD capacitor 1206 format
C2	10 nF LV	SMD capacitor 1206 format
C3	10 nF LV	SMD capacitor 1206 format
C4	10 nF LV	SMD capacitor 1206 format
C5	100 nF	SMD capacitor 1206 format
C6	47 $\mu$ F 50 V	SMD electrolytic capacitor
C7	4.7 nF	SMD capacitor 1206 format
C8	4.7 nF	SMD capacitor 1206 format
D1	SM15T39AC	Transil diode
DL1	LED	SMD LED diode 0805 format
DL2	LED	SMD LED diode 0805 format
DL3	LED	SMD LED diode 0805 format
DL4	LED	SMD LED diode 0805 format
OPT1	PC3Q66Q	4 channel opto isolator
OPT2	PC3Q66Q	4 channel opto isolator
IC1	VNI4140K	ST IC industrial 4 ch hsd
J1	Hader 34 pin	Compatible evalcommboard
J2	Jumper	Over voltage test
J3	Jumper	Ground disconnection test
J4	Jumper	Vcc disconnection test
J5	HADER 14 pin	Compatible ST7CANIC DB
M1	4 screw plug	HSD output connector
M2	2 screw plug	Power supply conector
T1	Test point	HSD output channel 1 voltage
T2	Test point	HSD output channel 2 voltage
T3	Test point	HSD output channel 3 voltage
T4	Test point	HSD output channel 4 voltage

**Table 2. Evaluation board bill of material (continued)**

T5	Test point	HSD input channel 1 signal
T6	Test point	HSD input channel 2 signal
T7	Test point	HSD input channel 3 signal
T8	Test point	HSD input channel 4 signal
T9	Test point	HSD channel 1 status
T10	Test point	HSD channel 2 status
T11	Test point	HSD channel 3 status
T12	Test point	HSD channel 4 status

## 4 Revision history

**Table 3. Document revision history**

Date	Revision	Changes
13-Dec-2007	1	Initial release

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