TN0147
Technical note

SPC56xB/C/Dxx family overview - features comparison

Introduction

The 32-bit SPC56 automotive microcontrollers are a family of System-on-Chip (SoC) devices designed to be central to the development of the next generation of central vehicle body controller, smart junction box, front module, peripheral body, door control and seat control applications.

The SPC56 Car Body family is a series of automotive microcontrollers based on the Power Architecture® technology and designed specifically for embedded automotive applications.

This document describes the overall differences across the SPC56 Car Body family and highlights important electrical and physical characteristics of the devices.

This document gathers products within several products sets that are:

- “SPC560D40”: for sales type SPC560D30 and SPC560D40
- “SPC560B50”: for sales type SPC560C/B50, SPC560C/B44 and SPC560C/B40
- “SPC560B64”: for sales type SPC560B54, SPC560B60 and SPC560B64
- “SPC56EC74”: for sales type SPC564B64/70/74 and SPC56EC64/70/74

The set namings refer to the most featured sale type in each set.

All sets are compared in consecutive pairs in other specific documents, please refer to TN0149, TN0225, TN0241 and TN0398 (see *Appendix A: Reference document*).

Contents

1 Overview of differences

Table 1. Overview of differences per module

Module name	Sub-modules	SPC560D40 module	SPC560B50 module	SPC560B64 module	SPC56EC74 module	Comment
Packages		LQFP64, 80, 100 80 pin available on specific demand only	LQFP100, 144	LQFP100, 144, 176	LQFP176, LQFP208, BGA256	BGA208 available for emulation purposes for entire family (based on SPC560B50 or SPC560B64 silicons) BGA256 available for emulation with full data trace capability on SPC56EC74
Signal Description	All signals are compatible but: – Some packages have additional muxing options – SPC56EC74 voltage regulator scheme requires a pin to be connected to the base of a transistor for ballast purpose. SPC560B64 uses the same pin in a different way (optional) – On some packages PB11 and PD12 are used for ADC reference – For SPC56EC74, and for LQFP176, PI9 and PI10 can be bonded as VSS_LV and VDD_LV (standard offering)					
Clock and Oscillators	32KHz Xosc	NO	YES	YES	YES	
	4-16MHz Xosc	YES	YES	YES	YES (4 to 40MHz)	
	16MHz IRC	YES	YES	YES	YES	
	128kHz IRC	YES	YES	YES	YES	
	Bus clock	48MHz	64MHz	64MHz	120MHz+2%	
Peripheral set groupings	set 1	LINFlex[0..2]	LINFlex[0..3], IIC	LINFlex[0..9], IIC	LINFlex[0..9], IIC	
	set 2	FlexCAN0, SPI[0..1]	FlexCAN[0..5], SPI[0..2]	FlexCAN[0..5], SPI[0..5]	FlexCAN[0..5], SPI[0..7]	
	set 3	ADC1, CTU, eMIOS0	ADC0, CTU, eMIOS[0..1]	ADC[0..1], CTU, eMIOS[0..1]	ADC[0..1], CTU, eMIOS[0..1]	

Table 1. Overview of differences per module (continued)

Module name	Sub-modules	SPC560D40 module	SPC560B50 module	SPC560B64 module	SPC56EC74 module	Comment
Peripheral set max clock	set 1 set 2 set 3	48MHz 48MHz 48MHz	64MHz 64MHz 64MHz	64MHz 64MHz 64MHz	32MHz 64MHz 64MHz	
Supply	The Vdd_BV pin also supports an external ballast resistor on the SPC560B64 and SPC560D40 SPC56EC74 requires an external NPN transistor					
Power Domains	PD0 (always on)	16kB RAM	8kB RAM or 32kB RAM	8kB RAM or 32kB RAM	8kB RAM or 32kB RAM, or 96kB RAM	All device family members have the two power domains, with the user option to disable the main power domain.
	PD1 (main)	Core + peripherals	Remaining RAM + Core + peripherals	Remaining RAM + Core + peripherals	Remaining RAM + Core + peripherals	
MC_RGM (Reset Generation Module)	LVD12 (PD0) LVD12 (PD1) LVD27 SWT POR LVD45 JTAG Core Z0 Core Z4 Software Checkstop FMPLL FXOSC fail CMU Flash error External reset MBIST	Destructive Destructive Destructive Destructive Destructive Functional Functional Functional Functional Functional Functional Functional Functional Functional Functional	Destructive Destructive Destructive Destructive Destructive Functional Functional Functional Functional Functional Functional Functional Functional Functional Functional	Destructive Destructive Destructive Destructive Destructive Functional Functional Functional Functional Functional Functional Functional Functional Functional Functional	Destructive Destructive Destructive Destructive Destructive Functional Functional Functional Functional Functional Functional Functional Functional Functional Functional Functional	

Table 1. Overview of differences per module (continued)

Module name	Sub-modules	SPC560D40 module	SPC560B50 module	SPC560B64 module	SPC56EC74 module	Comment
Operating Modes	STANDBY STOP HALT DRUN RUN0,1,2,3	All supported	All supported	All supported	All supported	All device family members support all the different flexibility offered by the various operating modes
ESCM		Yes	Yes	Yes	Yes	All device members have the same ESCM
Core		e200Z0h	e200Z0h	e200Z0h	e200Z4d, up to 120MHz e200Z0h, up to 80MHz if e200Z4d is running higher than 80MHz, then e200Z0h will run half its frequency	All Harvard e200Z4d includes an MMU and 4k instruction cache
Semaphores		0	0	0	16 gates	
XBAR	Master	Z0 instruction Z0 data eDMA	Z0 instruction Z0 data	Z0 instruction Z0 data eDMA	Z4 instruction Z4 data eDMA Z0 instruction Z0 data FEC FlexRay CSE	

Table 1. Overview of differences per module (continued)

Module name	Sub-modules	SPC560D40 module	SPC560B50 module	SPC560B64 module	SPC56EC74 module	Comment
XBAR	Slave	Flash SRAM Peripheral bridge	Flash SRAM Peripheral bridge	Flash SRAM Peripheral bridge	Flash0 Flash1 PRAM0 PRAM1 Peripheral bridge	On SPC56EC74, there are 2 RAM controllers in parallel (128Kb each), and Flash controller has 2 slave ports
MPU		No	Yes 8 regions	Yes 8 regions	Yes 16 regions	No MPU on SPC560D40
Voltage Reg		3-5V operation	3-5V operation	3-5V operation	3-5V operation	All devices utilise same Vreg structure and approach. The SPC560D40 and SPC560B64 device have an optional external ballast resistor. SPC56EC74 requires an external NPN transistor

Table 1. Overview of differences per module (continued)

Module name	Sub-modules	SPC560D40 module	SPC560B50 module	SPC560B64 module	SPC56EC74 module	Comment
LVD		1.2V: LVD_DIG (PD0) and LVD_DIG(PD1) 3.3V: LVD_MAIN 5V: LVD_MAIN5	1.2V: LVD_DIG (PD0) and LVD_DIG(PD1) 3.3V: LVD_MAIN 5V: LVD_MAIN5	1.2V: LVD_DIG (PD0) and LVD_DIG(PD1) 3.3V: LVD_MAIN 5V: LVD_MAIN5	1.2V: LVD_DIG (PD0) and LVD_DIG(PD1) 3.3V: LVD_MAIN 5V: LVD_MAIN5	All devices utilise same LVD approach. Some devices have an additional LVD3.3 ballast

Table 1. Overview of differences per module (continued)

Module name	Sub-modules	SPC560D40 module	SPC560B50 module	SPC560B64 module	SPC56EC74 module	Comment
Wake Up sources and associated interrupt vectors	Int Vector 0	API RTC PA1, NMI PA2 PB1,CANRX_0, LINRX_0 PC11 PE0 PE9	API RTC PA1, NMI PA2 PB1,CANRX_0 PC11,CANRX_1/4 PE0,CANRX_5 PE9,CANRX_2/3	API RTC PA1, NMI PA2 PB1,CANRX_0, LINRX_0 PC11,CANRX_1/4 PE0,CANRX_5 PE9,CANRX_2/3	API, RTC PA1, CANRX_3, NMI0 PA2, NMI1 PB1, CANRX_0, LINRX_0 PC11, CANRX_1/4 PE0, CANRX_5 PE9,CAN_RX2/3	
	Int Vector 1	PB10, ADC1_S6 PA4, CS0_1 PA15, CS0_0,SCK_0 PB3, LINRX_0 PC7, LINRX_1 PC9, LINRX_2 PE11,CS4_1	PB10, ADC0_S2 PA4 PA15,CS0_0,SCK_0 PB3, LINRX_0, SCL_0 PC7, LINRX_1 PC9, LINRX_2 PE11, LINRX_3, CS4_1 PF11	PB10, ADC0_S2 PA4, LINRX_5, CS0_1 PA15,CS0_0,SCK0 PB3, LINRX_0, SCL_0 PC7, LINRX_1 PC9, LINRX_2 PE11, LINRX_3, CS4_1 PF11,CS2_0, LINRX_4	PB10, ADC0_S2, ADC1_S6 PA4, LINRX_5, CS0_1 PA15,CS0_0,SCK_0 PB3, LINRX_0, SCL_0 PC7, LINRX_1 PC9, LINRX_2 PE11, LINRX_3,CS4_1 PF11, CS2_0, LINRX_4	
	Int Vector 2	PA0	PF13 PG3 PG5 PA0	PF13, LINRX_5 PG3, CS0_3 PG5, SIN_3 PA0 PG7, LINRX_6 PG9, LINRX_7 PF9, CANRX_3/2,CS5_0 PI3, LINRX_9	PF13, LINRX_5 PG3, CS0_3 PG5, SIN_3 PA0 PG7, LINRX_6 PG9, LINRX_7 PF9, CANRX_3/2,CS5_0 PI3, LIN_RX9	
	Int Vector 3	PB8, ADC1_S4 PB9, ADC1_S5 PD0, ADC1_P4 PD1, ADC1_P5		PI1, LINRX_8 PB8, ADC0_S0 PB9, ADC0_S1 PD0, ADC0_P4,ADC1_P4 PD1, ADC0_P5,ADC1_P5	PI1, LINRX_8 PB8, ADC0_S0/ADC1_S4 PB9, ADC0_S1/ADC1_S5 PD0, ADC0_P4/ADC1_P4 PD1, ADC0_P5/ADC1_P5 PE3, FR_A_RX PE5, FR_B_RX, CS0_1 PJ13,ADC1_S12,CANRX_1/4	

Table 1. Overview of differences per module (continued)

Module name	Sub-modules	SPC560D40 module	SPC560B50 module	SPC560B64 module	SPC56EC74 module	Comment
eDMA		16 channels	None	16 channels	32 channels	SPC560B50 does not support DMA
DMA Channel Multiplexer		16 slots	None	37 slots	64 slots	All DMA sources common to the SPC560D40 and SPC560B64 have same DMA slot multiplexer locations.
Embedded Debug		Nexus 1	Nexus 2+	Nexus 2+	Nexus 3+ on Z4d Nexus 3 on Z0h	Nexus 2+ supported on SPC560D40 via SPC560B64 die Nexus 3 with data trace available on SPC56EC74
INTC		Yes	Yes	Yes	Yes Interrupts can be driven to Z0 or Z4, or both. After reset, interrupts are driven to Z4	)

Table 1. Overview of differences per module (continued)

Module name	Sub-modules	SPC560D40 module	SPC560B50 module	SPC560B64 module	SPC56EC74 module	Comment
SRAM with ECC		16Kb	48k	96Kb	256Kb	The entire 16kB system RAM array on the SPC560D40 will be in the 'always on' standby domain. On the SPC560B50, SPC560B64 and SPC56EC74, 8k will be in the always on domain, with the option of an additional 32k. On the SPC560B64 the remainder is in the core domain.

Table 1. Overview of differences per module (continued)

Module name	Sub-modules	SPC560D40 module	SPC560B50 module	SPC560B64 module	SPC56EC74 module	Comment
Code Flash		256Kb	512k	1.5Mb	3Mb	Sectorization is compatible in all the family. ECC algorithm used for SPC560B50, is different than the one used for other products, but they ensure same level of error detection and correction
Data Flash		64Kb made of 4x16Kb blocks ECC 7bits on a 32bits data	64Kb made of 4x16Kb blocks ECC 8bits on a 64bits data	64Kb made of 4x16Kb blocks ECC 8bits on a 64bits data	64Kb made of 4x16Kb blocks ECC 7 bits on a 32bits data	Algorithms are different on all Data Flashs
BAM	Yes SWT enabled in static mode	Yes	Yes	Yes	Yes SWT enabled in static mode MMI configuration intialized when Z4 is primary core (normal case), not on Z0	SPC56EC74 was rewritten to run on Z4 also

Table 1. Overview of differences per module (continued)

Module name	Sub-modules	SPC560D40 module	SPC560B50 module	SPC560B64 module	SPC56EC74 module	Comment
DSPI		DSPI[0..1]	DSPI[0..2]	DSPI[0..5]	DSPI[0..7] DSPI0 chainable with 1 DSPI2 chainable with 3 eMIOS_A can feed DSPI0 and 2 eMIOS_B can feed DSP1 and 3	SPC56EC74 has a newer DSPI cell version (Backward compatible). The 4 first DSPI of SPC56EC74s upport serialization with eMIOS and chaining
LinFlex		LinFlex[0] with DMA LinFlex[1..2] Only LinFlex0 can be slave	LinFlex[0..3] Only LinFlex0 can be slave	LinFlex[0..1] with DMA LinFlex[2..9] Only LinFlex0 can be slave	LinFlex[0..9] with DMA Only LinFlex0 can be slave	LINFlex0 on SPC560D40 will handle DMA requests. LINFlex0 and LINFlex 1 on SPC560B64 will handle DMA requests. No DMA on SPC560B50 so no LIN / DMA support

Table 1. Overview of differences per module (continued)

Module name	Sub-modules	SPC560D40 module	SPC560B50 module	SPC560B64 module	SPC56EC74 module	Comment
FlexCAN		FlexCAN0	FlexCAN[0..5]	FlexCAN[0..5]	FlexCAN[0..5]	32 message buffers and no filter RAM on SPC560D40 (Message filters applicable only to Message Buffers 14 &15). Others have 64 Message buffers per FlexCAN each with individual filters on.
CAN Sampler		0	1	1	1	No CANSampler on SPC560D40
I2C		0	1	1	1	No I2C on SPC560D40
FEC (Fast Ethernet Controller)		0	0	0	1	
FlexRay		0	0	0	1	
eMIOS	module A	28 channels	28 channels	32 channels	32 channels	Different channel types supported across family
	module B	0	28 channels	32 channels	32 channels	
ADC0 (10 bit)	Precise Standard Extended	0 0 0	16 28 4	16 (shared with 12bit) 28 (3 shared with 12bit) 4	16 (shared with 12bit) 32 (3 shared with 12bit) 4	Maximum stated. Package dependent

Table 1. Overview of differences per module (continued)

Module name	Sub-modules	SPC560D40 module	SPC560B50 module	SPC560B64 module	SPC56EC74 module	Comment
ADC1 (12 bit)	Precise Standard Extended	16 13 4	0 0 0	16 (shared with 10bit) 8 (3 shared with 10bit) 0	16 (shared with 10bit) 13(3 shared with 10bit) 0	
CTU (Cross Triggering Unit)		1 No Way to trigger external conversions	1 Channel numbers in CTU_EVTCFGRx are counted contiguously, unlike other family members	1	1	
Register Protection		Yes	Yes	Yes	Yes	All devices utilize same protection mechanism
STCU (Self Test Control Unit)		No	No	No	Yes	MBIST on SPC56EC74
CSE (Cryptographic Services Engine)		No	No	No	Yes	
Watchdog Timer		Yes - Fixeds refresh	Yes - Fixed refresh	Yes - Fixed or pseudo random keyed	Yes - Fixed or pseudo random keyed	
RTC/API		Yes	Yes	Yes	Yes	All devices utilize same RTC / API

Table 1. Overview of differences per module (continued)

Module name	Sub-modules	SPC560D40 module	SPC560B50 module	SPC560B64 module	SPC56EC74 module	Comment
PIT		4	6	8	8 + 1 RTI (Real Time INterrupt) timer, to wakeup the CPU in stop mode	PIT2 is connected on ADC12-bit injection trigger on SPC560D40. On the SPC560B64 PIT 2 is connected to ADC-10bit and PIT 6 is connected to ADC-12bit. Same scheme for SPC56EC74
STM		4 channels	4 channels	4 channels	4 channels	All devices utilise same STM

2 Device ID

The MCU ID registers MIDR1 and MIDR2 contain information pertaining to the device including part number, package type, maskset information, and parametric data such as Flash size and inclusion of data Flash.

The device identification register within the JTAG controller is read by debuggers to identify the device under test.

Table 2 shows the register content for each device and package option. When porting code between the SPC560D40L3, SPC560B50L5, SPC560B64 and SPC56EC74 any software that depends on the contents of these registers should be modified appropriately. Refer to the respective device reference manuals for full bit-level descriptions of these registers.

Table 2. Device ID registers

Device	Package	Flash size	MIDR1	MIDR2	JTAG ID
SPC56EC74	BGA256	3 M	0x5646_30xx	0xB800_4311	0x06E48041
SPC56EC74	LQFP208	3 M	0x5646_54xx	0xB800_4311	0x06E48041
SPC56EC74	LQFP176	3 M	0x5646_44xx	0xB800_4311	0x06E48041
SPC564B74	LQFP208	3 M	0x5646_54xx	0xBA00_4211	0x06E48041
SPC564B74	LQFP176	3 M	0x5646_44xx	0xBA00_4211	0x06E48041
SPC56EC70	BGA256	2 M	0x5645_30xx	0xB800_4311	0x06E48041
SPC56EC70	BGA208	2 M	0x5645_40xx	0xB800_4311	0x06E48041
SPC56EC70	LQFP208	2 M	0x5645_54xx	0xB800_4311	0x06E48041
SPC56EC70	LQFP176	2 M	0x5645_44xx	0xB800_4311	0x06E48041
SPC564B70	LQFP208	2 M	0x5645_54xx	0xB800_4211	0x06E48041
SPC564B70	LQFP176	2 M	0x5645_44xx	0xB800_4211	0x06E48041
SPC56EC64	BGA256	1.5 M	0x5644_30xx	0xB200_4311	0x06E48041
SPC56EC64	BGA208	1.5 M	0x5644_40xx	0xB200_4311	0x06E48041
SPC56EC64	LQFP208	1.5 M	0x5644_54xx	0xB200_4311	0x06E48041
SPC56EC64	LQFP176	1.5 M	0x5644_44xx	0xB200_4311	0x06E48041
SPC564B64	LQFP208	1.5 M	0x5644_54xx	0xB200_4211	0x06E48041
SPC564B64	LQFP176	1.5 M	0x5644_44xx	0xB200_4211	0x06E48041
SPC560B64	LQFP176	1.5 M	0x5607_44xx	0xB200_4210	0x0AE43041
SPC560B64	LQFP144	1.5 M	0x5607_34xx	0xB200_4210	0x0AE43041
SPC560B64	LQFP100	1.5 M	0x5607_24xx	0xB200_4210	0x0AE43041
SPC560B60	LQFP176	1 M	0x5606_44xx	0xB000_4210	0x0AE43041
SPC560B60	LQFP144	1 M	0x5606_34xx	0xB000_4210	0x0AE43041
SPC560B60	LQFP100	1 M	0x5606_24xx	0xB000_4210	0x0AE43041
SPC560B54	LQFP176	768 KB	0x5605_44xx	0xAA00_4210	0x0AE43041

Table 2. Device ID registers (continued)

Device	Package	Flash size	MIDR1	MIDR2	JTAG ID
SPC560B54	LQFP144	768 KB	0x5605_34xx	0xAA00_4210	0x0AE43041
SPC560B54	LQFP100	768 KB	0x5605_24xx	0xAA00_4210	0x0AE43041
SPC560B50	LQFP144	512 KB	0x5604_34xx	0xA800_4210	0x0AE41041
SPC560B50	LQFP100	512 KB	0x5604_24xx	0xA800_4210	0x0AE41041
SPC560C50	LQFP100	512 KB	0x5604_24xx	0xA800_4310	0x0AE41041
SPC560B44	LQFP144	384 KB	0x5603_34xx	0xA200_4210	0x0AE41041
SPC560B44	LQFP100	384 KB	0x5603_24xx	0xA200_4210	0x0AE41041
SPC560C44	LQFP100	384 KB	0x5603_24xx	0xA200_4310	0x0AE41041
SPC560B40	LQFP144	256 KB	0x5602_34xx	0xA000_4210	0x0AE41041
SPC560B40	LQFP100	256 KB	0x5602_24xx	0xA000_4210	0x0AE41041
SPC560C40	LQFP100	256 KB	0x5602_24xx	0xA000_4310	0x0AE41041
SPC560D40	LQFP100	256 KB	0x5602_24xx	0xA000_4410	0x0AE44041
SPC560D40	LQFP64	256 KB	0x5602_04xx	0xA000_4410	0x0AE44041
SPC560D30	LQFP100	128 KB	0x5601_24xx	0x9800_4410	0x0AE44041
SPC560D30	LQFP64	128 KB	0x5601_04xx	0x9800_4410	0x0AE44041

Appendix A Reference document

1. Migration guide and device emulation for SPC560Dx with SPC560B54/6x (TN0149, DocID16507)
2. Migration guide for SPC560C/B50, SPC560C/B4x with SPC560B54/6x (TN0225, DocID17155)
3. Migration guide for SPC560Dx with SPC560C/B50 (TN0241, DocID17246)
4. Migration difference between SPC56EC74 and SPC560B64 (TN0398, DocID18086)

3 Document revision history

Figure 1. Revision history

Date	Revision	Changes
13-Dec-2010	1	Initial release.
05-May-2013	2	Added SPC564Bx and SPC56ECx devices information
17-Sep-2013	3	Updated Disclaimer.