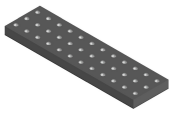
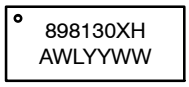
OIS/CL-AF & Zoom Control LSI

Advance Information
LC898130DP



WLCSP36
CASE 567ZU

MARKING DIAGRAM



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping†
LC898130DP1XHTBG	WLCSP36 (Pb−Free)	4,000 / Tape & Reel
LC898130DPNXHTBG	WLCSP36 (Pb−Free)	4,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Overview

This is a system LSI integrating an on−chip 32bit DSP, a FLASH ROM and peripherals including analog circuits for OIS (Optical Image Stabilization) / Closed Loop−AF (Auto Focus) and Zoom control, constant current drivers and PIEZO drivers.

Features

- On−chip 32bit DSP
  - Built−in Software for Digital Servo Filter
  - Built−in Software for Gyro Filter
- Memory
  - Flash Memory
  - Program ROM
  - Program SRAM
  - Data SRAM
- Peripherals
  - AD Converter
  - DA Converter
  - 2−wire Serial I/F Circuit
    (The Communication Protocol is Compatible with I^2C)
  - Hall/MR Bias Circuit
  - VGA (Hall/MR Amp)
  - OSC (Oscillator)
  - LDO (Low Drop−Out Regulator)
  - Digital Gyro I/F (SPI)
  - Interrupt I/F
  - PLL
  - Temperature Sensor
- Driver
  - OIS/CL−AF and Zoom/PIEZO (Bi−direction)
    Constant Current Linear Driver (x2ch, I_{full} = 200 mA)
  - PIEZO (Di−direction)
    PWM Driver (x2ch, Exclusive Use with Constant Current Linear Driver)
- Package
  - WLCSP36 (3 x 12 Pin) Thickness Max. 0.35 mm, with Back Coat
  - Lead−Free
  - Halogen Free
- Power Supply Voltage
  - AD/DA/VGA/LDO/OSC/Flash/PLL/Temp. Sensor:
    AVDD = 2.7 V to 3.6 V
  - Driver: V_M = 2.7 V to 3.6 V
  - 1.8 V I/O: I_{OVDD} = 1.7 V to 3.6 V
  - Core Logic: Generated by On−chip LDO
    Connect 1 μF Capacitor to LDPO Pin

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BLOCK DIAGRAM

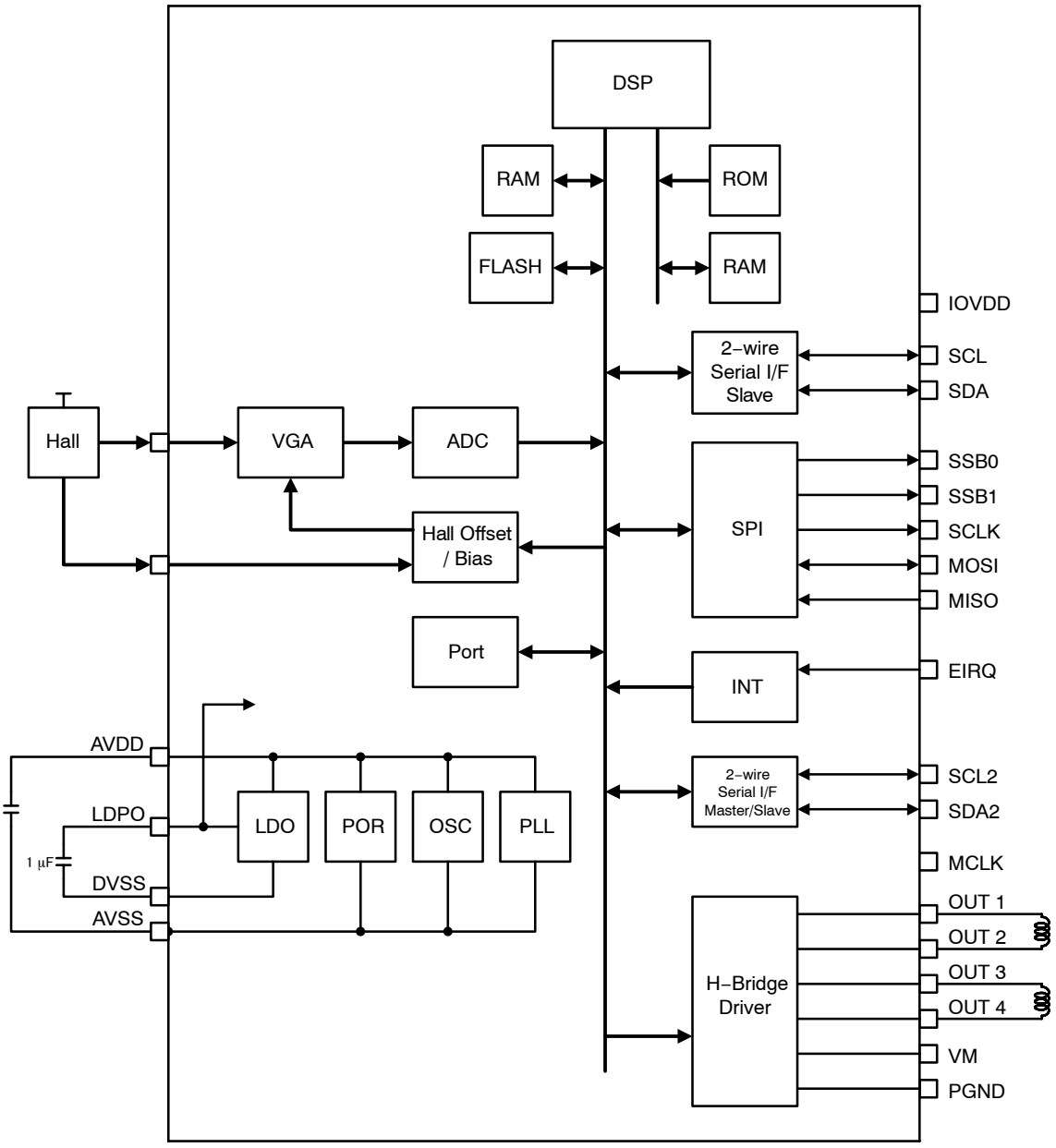

Figure 1. Block Diagram

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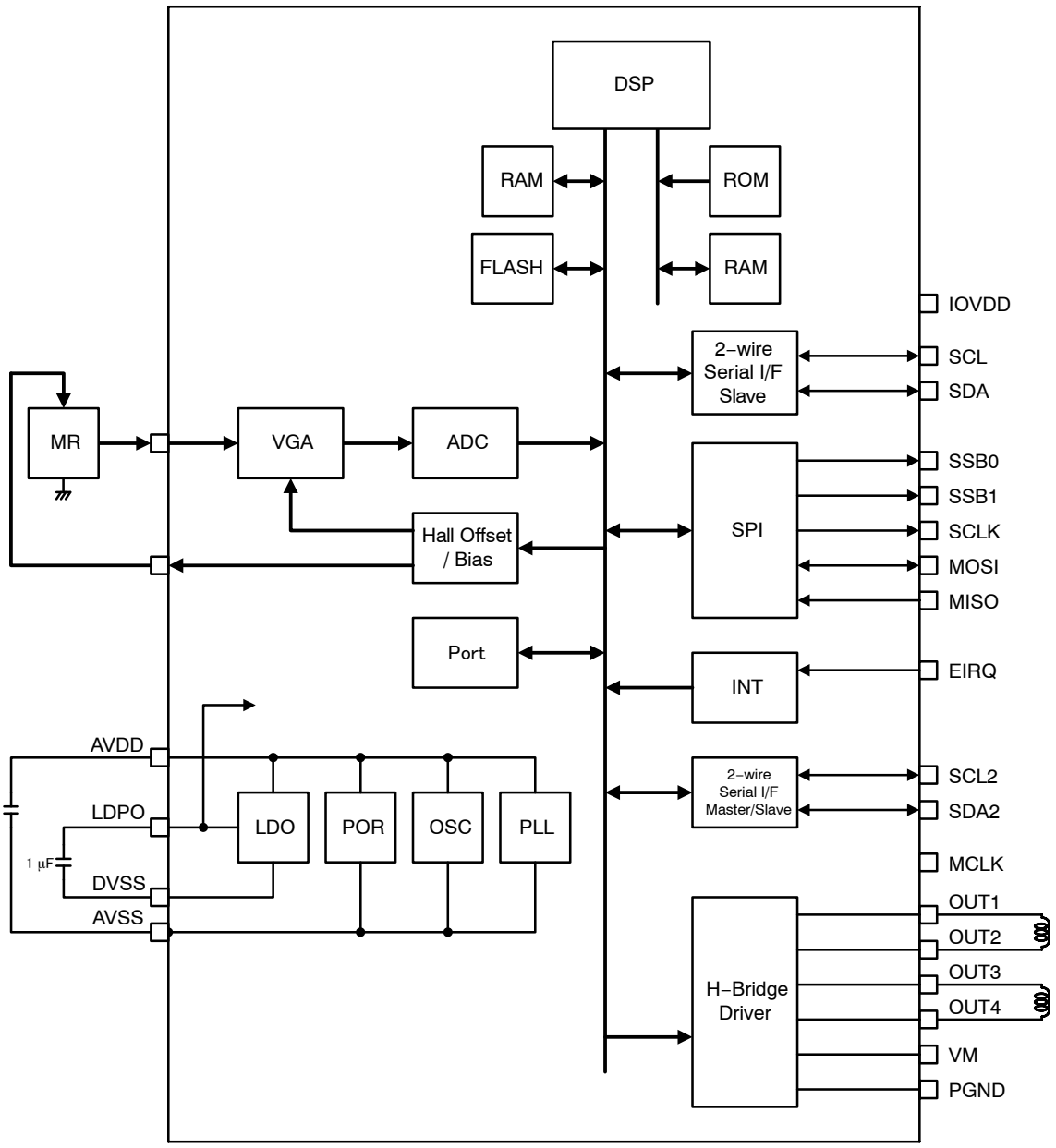

Figure 2. Block Diagram

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PIN LAYOUT

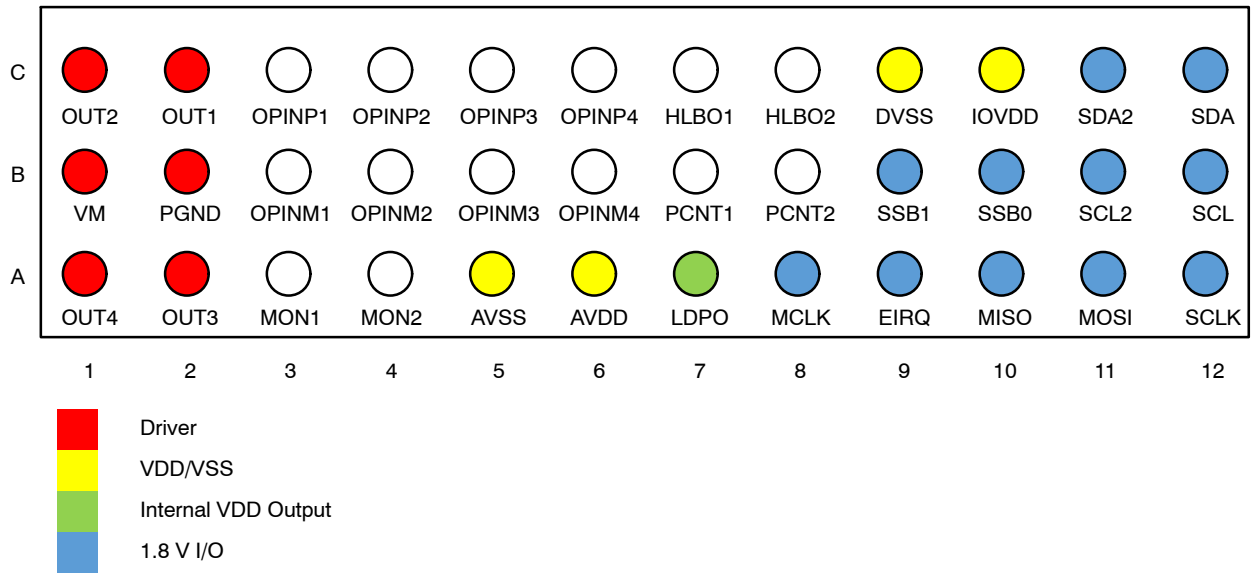

Figure 3. Pin Layout (Bottom View)

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PIN DESCRIPTION

PIN DESCRIPTION

No.	Pin	I/O	I/O Pwr	Function	Init
1	MON1	B	AVDD	Servo Monitor Analog In/Out	Z
2	MON2	B	AVDD	Servo Monitor Analog In/Out	Z
3	SCL	B	IOVDD	2−wire serial HOST I/F Clock Slave	Z
4	SDA	B	IOVDD	2−wire serial HOST I/F Data Slave	Z
5	SSB0	B	IOVDD	Digital Gyro Data I/F Chip Select 0 Out (3/4−wire Master)	Z
6	SCLK	B	IOVDD	Digital Gyro Data I/F Clock Out (3/4−wire Master)	Z
7	MOSI	B	IOVDD	Digital Gyro Data I/F Data InOut (3−wire Master) Digital Gyro Data I/F Data Out (4−wire Master)	Z
8	MISO	B	IOVDD	Digital Gyro Data I/F Data In (4−wire Master) SSB2 SELADR	U
9	EIRQ	B	IOVDD	Interrupt Input	Z
10	MCLK	B	IOVDD	Master Clock	Z
11	SSB1	B	IOVDD	Digital Gyro Data I/F Chip Select 1 Out (3/4−wire Master)	Z
12	SCL2	B	IOVDD	2−wire serial I/F Clock Master/Slave	Z
13	SDA2	B	IOVDD	2−wire serial I/F Data Master/Slave	Z
14	HLBO1	O	AVDD	Hall/MR Bias Output 1	Z
15	HLBO2	O	AVDD	Hall/MR Bias Output 2	Z
16	PCNT1	O	AVDD	External Driver Power Control 1	Z
17	PCNT2	O	AVDD	External Driver Power Control 2	Z
18	OPINM1	I	AVDD	VGA (Hall/MR Amp) Input Minus 1	−
19	OPINP1	I	AVDD	VGA (Hall/MR Amp) Input Plus 1	−
20	OPINM2	I	AVDD	VGA (Hall/MR Amp) Input Minus 2	−
21	OPINP2	I	AVDD	VGA (Hall/MR Amp) Input Plus 2	−
22	OPINM3	I	AVDD	VGA Input Minus 3	−
23	OPINP3	I	AVDD	VGA (MR Amp) Input Plus 3	−
24	OPINM4	I	AVDD	VGA Input Minus 4	−
25	OPINP4	I	AVDD	VGA (MR Amp) Input Plus 4	−
26	OUT1	O	VM	OIS Driver Output 1	Z
27	OUT2	O	VM	OIS Driver Output 2	Z
28	OUT3	O	VM	OIS Driver Output 3	Z
29	OUT4	O	VM	OIS Driver Output 4	Z
30	AVDD	P		Analog Power (2.7 V to 3.6 V)	−
31	AVSS	P		Analog GND	−
32	VM	P		Driver Power (2.7 V to 3.6 V)	−
33	PGND	P		Driver GND	−
34	IOVDD	P		I/O Power (1.7 V to 3.6 V)	−
35	DVSS	P		Digital GND	−
36	LDPO	P		Internal 1.38 V LDO Power Output	−

NOTE: Z: Hi−Z
U: Internal Pull−Up Register On
D: Internal Pull−Down Register On

*Process when pins are not used

- PIN TYPE “O” – Ensure that it is set to OPEN.
- PIN TYPE “I” – OPEN is inhibited. Ensure that it is connected to the V_{DD} or V_{SS} even when it is unused. (Please contact **onsemi** for more information about selection of V_{DD} or V_{SS}.)
- PIN TYPE “B” – If you are unsure about processing method on the pin description of pin layout table, please contact us.

Note that incorrect processing of unused pins may result in defects.

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ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (AVSS = 0 V, PGND = 0 V, DVSS = 0 V)

Parameter	Symbol	Conditions	Ratings	Unit
Power Supply Voltage	V_{AD} max	$T_A \le 25°C$	−0.3 to 4.6	V
	V_M max	$T_A \le 25°C$	−0.3 to 4.6	V
	V_{IO} max	$T_A \le 25°C$	−0.3 to 4.6	V
Input/Output Voltage	V_{AI}, V_{AO}	$T_A \le 25°C$	−0.3 to V_{AD} + 0.3	V
	V_{MI}, V_{MO}	$T_A \le 25°C$	−0.3 to V_M + 0.3	V
	V_{II}, V_{IOO}	$T_A \le 25°C$	−0.3 to V_{IO} + 0.3	V
Storage Temperature	T_{stg}		−55 to 125	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ALLOWABLE OPERATING RATINGS (T_A = −40 to 85°C, AVSS = 0 V, PGND = 0 V, DVSS = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
3.0 V POWER SUPPLY (AVDD)					
Power Supply Voltage	V_{AD}	2.7	2.8	3.6	V
Input Voltage Range	V_{INA}	0	–	V_{AD}	V
3.0 V POWER SUPPLY (VM)					
Power Supply Voltage	V_M	2.7	2.8	3.6	V
Input Voltage Range	V_{INM}	0	–	V_M	V
1.8 V POWER SUPPLY (IOVDD)					
Power Supply Voltage	V_{IO}	1.7	1.8	3.6	V
Input Voltage Range	V_{INI}	0	–	V_{IO}	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC CHARACTERISTICS: INPUT/OUTPUT

(T_A = −40 to 85°C, AVSS = 0 V, PGND = 0 V, DVSS = 0 V, AVDD = 2.7 to 3.6 V, IOVDD = 1.7 to 3.6 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Applicable Pins
High−level Input Voltage	V_{IH}	CMOS Schmitt	0.7 IOVDD	–	–	V	SCL, SDA, SCL2, SDA2, SSB0, SSB1, SCLK, MOSI, MISO, EIRQ, MCLK
Low−level Input Voltage	V_{IL}		–	–	0.3 IOVDD	V	
High−level Input Voltage	V_{IH}	CMOS Schmitt	0.7 AVDD	–	–	V	MON1, MON2
Low−level Input Voltage	V_{IL}		–	–	0.3 AVDD	V	
High−level Output Voltage	V_{OH}	I_{OH} = −3 mA	IOVDD − 0.2	–	–	V	SDA, SCL2, SDA2, SSB0, SSB1, SCLK, MOSI, MISO, EIRQ, MCLK
Low−level Output Voltage	V_{OL}	I_{OL} = 3 mA	–	–	0.2	V	SCL, SDA, SCL2, SDA2, SSB0, SSB1, SCLK, MOSI, MISO, EIRQ, MCLK
High−level Output Voltage	V_{OH}	I_{OH} = −2 mA	AVDD − 0.2	–	–	V	MON1, MON2
Low−level Output Voltage	V_{OL}	I_{OL} = 2 mA	–	–	0.2	V	
Analog Input Voltage	V_{AI}		AVSS	–	AVDD	V	MON1, MON2, OPINP1, OPINM1, OPINP2, OPINM2, OPINP3, OPINM3, OPINP4, OPINM4

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DC CHARACTERISTICS: INPUT/OUTPUT (continued)
(T_A = −40 to 85°C, AVSS = 0 V, PGND = 0 V, DVSS = 0 V, AVDD = 2.7 to 3.6 V, IOVDD = 1.7 to 3.6 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Applicable Pins
Pull Up Resistor	R_{up}		20	–	250	kΩ	SCL2, SDA2, SSB0, SSB1, SCLK, MOSI, MISO, EIRQ, MCLK, MON1, MON2
Pull Down Resistor	R_{dn}		20	–	250	kΩ	

DRIVER OUTPUT
(T_A = 25°C, AVSS = 0 V, PGND = 0 V, DVSS = 0 V, AVDD = VM = 2.8 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output Current, OUT1−OUT4	I_{full}	Full code	190	200	210	mA

NON−VOLATILE MEMORY CHARACTERISTICS
(T_A = −40 to 85°C, AVSS = 0 V, PGND = 0 V, DVSS = 0 V, AVDD = 2.7 to 3.6 V, IOVDD = 1.7 to 3.6 V)

Parameter	Symbol	Conditions	Value	Unit
Operating Temperature	T_{opr1}	Read for FLASH	−40 to 85	°C
	T_{opr2}	Program & Erase for FLASH	−10 to 65 (Note 1)	°C

1. All drivers must be in the standby state.

Item	Symbol	Conditions	Min	Typ	Max	Unit	Applicable Circuit
Endurance	EN		–	–	1000	Cycles	Flash Memory
Data Retention	RT		10	–	–	Years	
Write Time	t_{WT}		–	–	3	ms	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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AC CHARACTERISTICS

Power Supply Timing

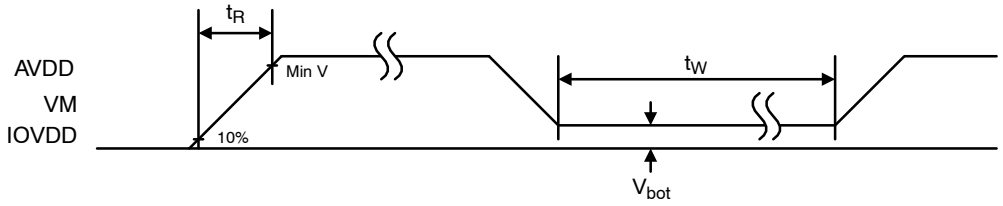

Figure 4. V_{DD} Supply Timing

Table 1.

Item	Symbol	Min	Typ	Max	Unit
Rise Time	t_R	–	–	3	ms
Wait Time	t_W	100	–	–	ms
Bottom Voltage	V_{bot}	–	–	0.2	V

Injection order between AVDD, VM and IOVDD is below.

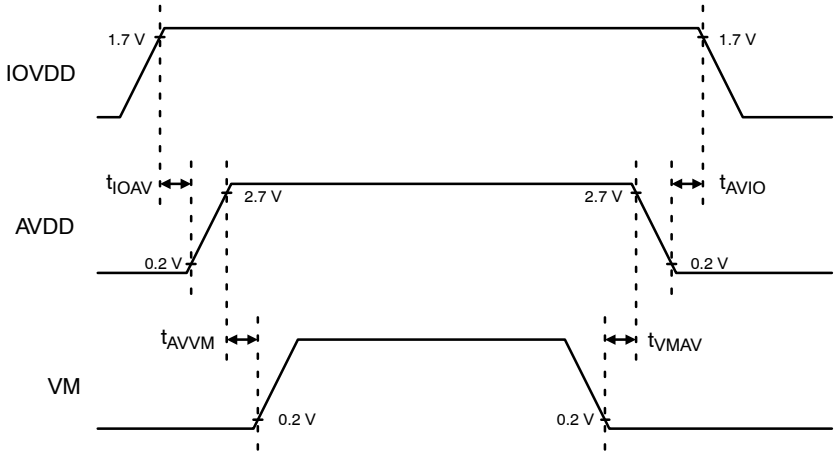

Figure 5. Injection Order between AVDD, VM and IOVDD

Table 2.

Item	Symbol	Min	Typ	Max	Unit
IOVDD On to AVDD ON	t_{IOAV}	0	–	–	ms
AVDD ON to VM ON	t_{AVVM}	0	–	–	ms
VM OFF to AVDD OFF	t_{VMAV}	0	–	–	ms
AVDD OFF to IOVDD OFF	t_{AVIO}	0	–	*	ms

*Please make IOPRSTB (D0_0064h, bit0) = 0 before turning OFF AVDD when AVDD is turned off with keeping IOVDD on.

SDA, SCL, SSB0, SSB1, SCLK, MOSI, MISO, EIRQ, MCLK, SCL2 and SDA2 tolerate 3 V input at the time of IOVDD power off.

The data in the Flash memory may be rewritten unintentionally if you do not keep specifications.

And it is forbidden to power off during Flash memory access. The data in the Flash memory may be rewritten unintentionally.

Drivers are recommended to set standby before VM power off.

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2−wire Serial Interface Timing

The 2−wire serial interface timing definition and electric characteristics are shown below. The communication protocol is compatible with I^2C. This circuit has clock stretch function.

Static Address: 7'b0100100

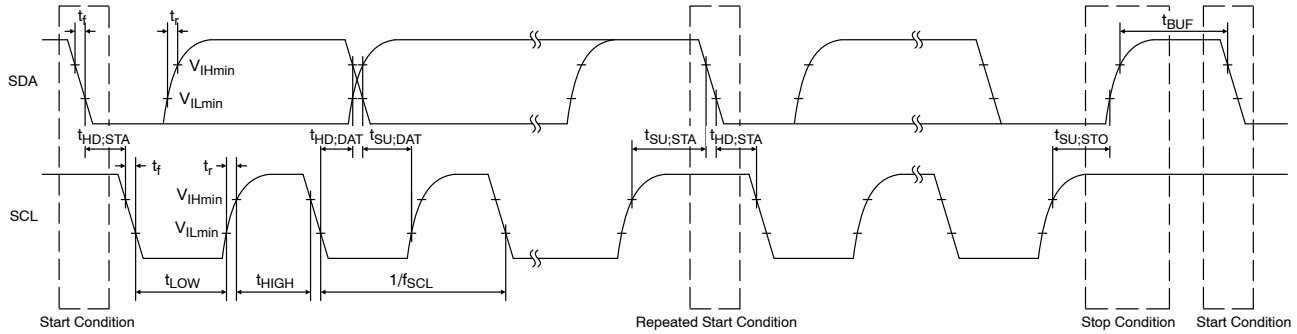

Figure 6. 2−wire Serial Interface Timing

Table 3.

Item	Symbol	Standard−mode		Fast−mode		Fast−mode Plus		Units
		Min	Max	Min	Max	Min	Max	
SCL Clock Frequency	f_{SCL}	−	100	−	400	−	1000	kHz
START Condition Hold Time	$t_{HD;STA}$	4.0	−	0.6	−	0.26	−	μs
SCL Clock Low Period	t_{LOW}	4.7	−	1.3	−	0.5	−	μs
SCL Clock High Period	t_{HIGH}	4.0	−	0.6	−	0.26	−	μs
Setup Time for Repetition START Condition	$t_{SU;STA}$	4.7	−	0.6	−	0.26	−	μs
Data Hold Time	$t_{HD;DAT}$	0 (Note 2)	3.45	0 (Note 2)	0.9	0 (Note 2)	0.45	μs
Data Setup Time	$t_{SU;DAT}$	250	−	100	−	50	−	ns
SDA, SCL Rising Time	t_r	−	1000	−	300	−	120	ns
SDA, SCL Falling Time	t_f	−	300	−	300	−	120	ns
STOP Condition Setup Time	$t_{SU;STO}$	4.0	−	0.6	−	0.26	−	μs
Bus Free Time between STOP and START	t_{BUF}	4.7	−	1.3	−	0.5	−	μs

2. Although the I_2C specification defines a condition that 300 ns of hold time is required internally, this LSI is designed for a condition with typ. 33 ns of hold time. If SDA signal is unstable around falling point of SCL signal, please implement an appropriate treatment on board, such as inserting a resister.

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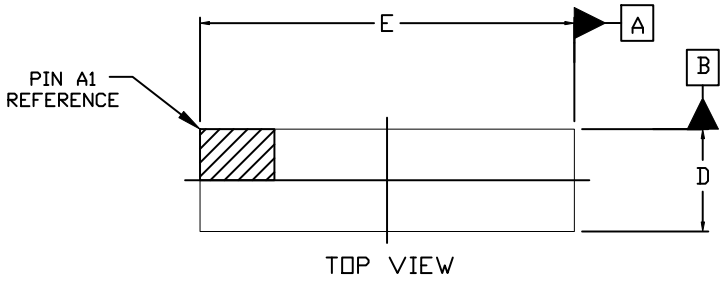
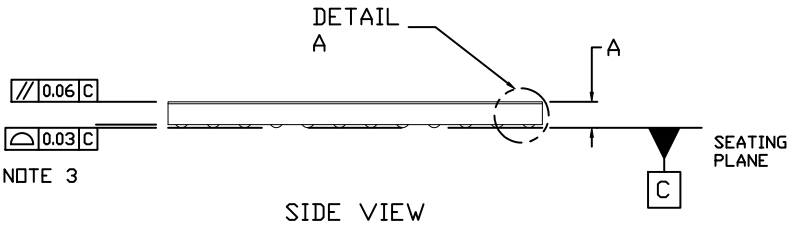
LC898130DP

PACKAGE DIMENSIONS

WLCSP36 1.295x4.74x0.33
CASE 567ZU
ISSUE O



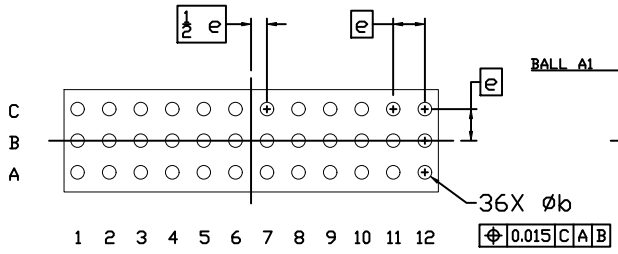
TOP VIEW



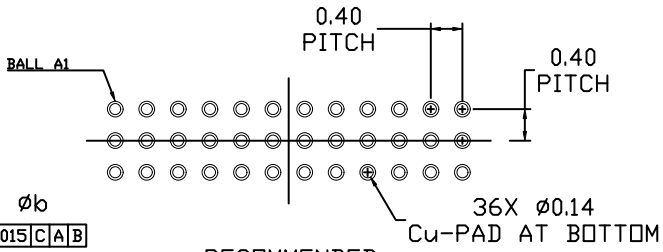
SIDE VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
4. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. DIMENSION b IS MEASURED AT THE MAXIMUM BALL DIAMETER, PARALLEL TO DATUM C.

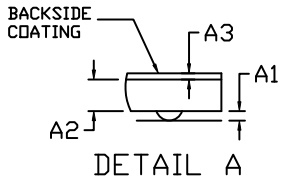
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.31	0.33	0.35
A1	0.025	0.040	0.055
A2	0.25	0.265	0.28
A3		0.025 REF	
b	0.14	0.17	0.20
D	1.245	1.295	1.345
E	4.69	4.74	4.79
e		0.40 BSC	



BOTTOM VIEW



RECOMMENDED
MOUNTING FOOTPRINT*
(NSMD PAD TYPE)



DETAIL A

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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