LV51131T

2-Cell Lithium-Ion Secondary Battery Protection IC

ON Semiconductor®

Overview

The LV5131T is a protection IC for 2-cell lithium-ion secondary batteries.

Features

- Monitoring Function for Each Cell:
  Detects overcharge and over-discharge conditions and controls the charging and discharging operation of each cell.
- High Detection Voltage Accuracy:
  Over-charge detection accuracy   ±25 mV
  Over-discharge detection accuracy ±100 mV
- Hysteresis Cancel Function:
  The hysteresis of over-discharge detection voltage is decreased by sensing the connection of a load after overcharging has been detected.
- Discharge Current Monitoring Function:
  Detects over-currents, load shorting, and excessively high voltage of a charger and regulates charging and discharging operations.
- Low Current Consumption:
  Normal operation mode   typ. 6.0 μA
              Stand by mode   max. 0.2 μA
- 0 V Cell Charging Function:
  Charging is enabled even when the cell voltage is 0 V by giving a potential difference between the V_{DD} pin and V^- pin.
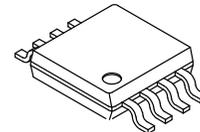
MSOP−8
CASE 846AH

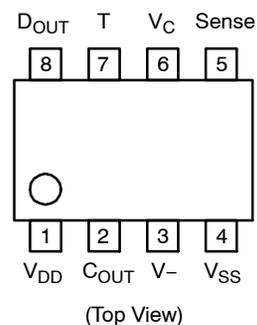### MARKING DIAGRAM

51131
YMWL

51131	= Specific Device Code
Y	= Year of Production
M	= Assembly Operation Month
WL	= Wafer Lot Number

PIN ASSIGNMENT

D_{OUT}	T	V_C	Sense
8	7	6	5
1	2	3	4
V_{DD}	C_{OUT}	V^-	V_{SS}

(Top View)

ORDERING INFORMATION

Device	Package	Shipping[†]
LV51131T−TLM−E	MSOP−8 (Pb−Free)	2,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

January, 2019 − Rev. 2

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LV51131T

Specifications

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Parameter		Symbol	Conditions	Ratings	Unit
Power Supply Voltage		V_{DD}		−0.3 to +12	V
Input Voltage Charger Minus Voltage		V−		V_{DD}−28 to V_{DD}+0.3	V
Output Voltage	Cout Pin Voltage	Vcout		V_{DD}−28 to V_{DD}+0.3	V
	Dout Pin Voltage	Vdout		V_{SS}−0.3 to V_{DD}+0.3	V
Allowable Power Dissipation		Pd max	Independent IC	170	mW
Operating Ambient Temperature		Topr		−30 to +85	°C
Storage Temperature		Tstg		−40 to +125	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Absolute maximum rating shows the permission level that must not surpass even for an instant.
2. Even if LV521131T was used within the absolute maximum rating, if it operate frequently on high temperature and high current or high voltage or great temperature changes in succession, reliability might decrease.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operation input voltage	Vcell	$V_{DD} - V_{SS}$ between voltage	1.5		10	V
0 V cell charging minimum operation voltage	Vmin	$V_{DD} - V_{SS}$ = 0, V_{DD} – V between voltage			1.5	V
Over-charge detection voltage	Vd1		4.325	4.350	4.375	V
		Ta = 0–45°C (Note 4)	4.315	4.350	4.385	V
Over-charge release voltage	Vr1	VM ≤ Vd3	4.100	4.150	4.200	V
		VM > Vd3	4.250		4.360	V
Over-charge detection delay time	td1	V_{DD} – Vc = 3.5 V → 4.5 V, Vc – V_{SS} = 3.5 V	0.5	1.0	1.5	s
Over-charge release delay time	tr1	V_{DD} – Vc = 4.5 V → 3.5 V, Vc – V_{SS} = 3.5 V	20.0	40.0	60.0	ms
Over-discharge detection voltage	Vd2		2.20	2.30	2.40	V
Over-discharge release hysteresis voltage	Vh2		10.0	20.0	40.0	mV
Over-discharge detection delay time	td2	V_{DD} – Vc = 3.5 V → 2.2 V, Vc – V_{SS} = 3.5 V	50	100	150	ms
Over-discharge release delay time	tr2	V_{DD} – Vc = 2.2 V → 3.5 V, Vc – V_{SS} = 3.5 V	0.5	1.0	1.5	ms
Over-current detection voltage	Vd3	V_{DD} – Vc = 3.5 V, Vc – V_{SS} = 3.5 V	0.130	0.150	0.170	V
Over-current release hysteresis voltage	Vh3	V_{DD} – Vc = 3.5 V, Vc – V_{SS} = 3.5 V	5.0	10.0	20.0	mV
Over−current detection delay time	td3	V_{DD} – Vc = 3.5 V, Vc – V_{SS} = 3.5 V	10.0	20.0	30.0	ms
Short−current release delay time	tr3	V_{DD} – Vc = 3.5 V, Vc – V_{SS} = 3.5 V	0.5	1.0	1.5	ms
Short circuit detection voltage	Vd4	V_{DD} – Vc = 3.5 V, Vc – V_{SS} = 3.5 V	1.0	1.3	1.6	V
Short circuit detection delay time	td4	V_{DD} – Vc = 3.5 V, Vc – V_{SS} = 3.5 V	0.125	0.250	0.500	ms
Excessive charger detection voltage	Vd5	V_{DD} – Vc = 3.5 V, Vc – V_{SS} = 3.5 V (V−) – V_{SS} between voltage	−0.60	−0.45	−0.30	V
Release hysteresis voltage	Vh5	V_{DD} – Vc = 3.5 V, Vc – V_{SS} = 3.5 V	25.0	50.0	100.0	mV

ELECTRICAL CHARACTERISTICS (T_A = 25°C, unless otherwise specified) (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Stand−by release voltage	Vstb	V_{DD} − Vc = 2.0 V, Vc − V_{SS} = 2.0 V (V⁻) − V_{SS} between voltage	$V_{DD} \times 0.4$	$V_{DD} \times 0.5$	$V_{DD} \times 0.6$	V
Excessive charger detection delay time	td5	V_{DD} − Vc = 3.5 V, Vc − V_{SS} = 3.5 V (Note 3)	0.5	1.5	3.0	ms
Excessive charger release delay time	tr5	V_{DD} − Vc = 3.5 V, Vc − V_{SS} = 3.5 V	0.5	1.5	3.0	ms
Internal resistance (VM−VDD)	R_{DD}	When overcharge is detected	100	200	400	kΩ
Internal resistance (VM−VSS)	R_{SS}	When over current or short circuit is detected	15	30	60	kΩ
Cout Nch ON voltage	V_OL1	I_OL = 50 μA, V_{DD} − Vc = 4.4 V, Vc − V_{SS} = 4.4 V			0.5	V
Cout Pch ON voltage	V_OH1	I_OL = 50 μA, V_{DD} − Vc = 3.9 V, Vc − V_{SS} = 3.9 V	V_{DD} − 0.5			V
D_{OUT} Nch ON voltage	V_OL2	I_OL = 50 μA, V_{DD} − Vc = 2.2 V, Vc − V_{SS} = 2.2 V			0.5	V
D_{OUT} Pch ON voltage	V_OH2	I_OL = 50 μA, V_{DD} − Vc = 3.9 V, Vc − V_{SS} = 3.9 V	V_{DD} − 0.5			V
V_C input current	Ivc	V_{DD} − Vc = 3.5 V, Vc − V_{SS} = 3.5 V		0.0	1.0	μA
Current consumption	I_{DD}	V_{DD} − Vc = 3.5 V, Vc − V_{SS} = 3.5 V		6.0	13.0	μA
Stand−by current	Istb	V_{DD} − Vc = 2.2 V, Vc − V_{SS} = 3.5 V			0.2	μA
T−terminal input ON voltage	Vtest	V_{DD} − Vc = 3.5 V, Vc − V_{SS} = 3.5 V	$V_{DD} \times 0.4$	$V_{DD} \times 0.5$	$V_{DD} \times 0.6$	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
3. Over charge detection to over discharge battery is It is delay time from after over-discharge return.
4. This specification value is the design target value and does not check at production test.

ELECTRICAL CHARACTERISTICS (T_A = −20°C to 60°C, unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operation input voltage	Vcell	V_{DD} − V_{SS} between voltage	1.65		10	V
0 V cell charging minimum operation voltage	Vmin	V_{DD} − V_{SS} = 0, V_{DD} − V between voltage			1.65	V
Over-charge detection voltage	Vd1	(Note 6)	4.305	4.350	4.390	V
Over-charge reset voltage	Vh1	VM ≤ Vd3	4.080	4.150	4.215	V
		VM > Vd3	4.235		4.375	V
Over-charge detection delay time	td1	V_{DD} − Vc = 3.5 V → 4.5 V, Vc − V_{SS} = 3.5 V	0.350	1.000	2.400	s
Over-charge reset delay time	tr1	V_{DD} − Vc = 4.5 V → 3.5 V, Vc − V_{SS} = 3.5 V	14.0	40.0	96.0	ms
Over-discharge detection voltage	Vd2		2.18	2.30	2.42	V
Over-discharge release hysteresis voltage	Vh2		8.0	20.0	42.0	mV
Over-discharge detection delay time	td2	V_{DD} − Vc = 3.5 V → 2.2 V, Vc − V_{SS} = 3.5 V	35	100	240	ms
Over-discharge release delay time	tr2	V_{DD} − Vc = 2.2 V → 3.5 V, Vc − V_{SS} = 3.5 V	0.35	1.0	2.4	ms
Over-current detection voltage	Vd3	V_{DD} − Vc = 3.5 V, Vc − V_{SS} = 3.5 V	0.120	0.150	0.180	V
Over-current release hysteresis voltage	Vh3	V_{DD} − Vc = 3.5 V, Vc − V_{SS} = 3.5 V	3.5	10.0	23.0	mV

ELECTRICAL CHARACTERISTICS (T_A = −20°C to 60°C, unless otherwise specified) (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Over-current detection delay time	td3	$V_{DD} - Vc$ = 3.5 V, $Vc - V_{SS}$ = 3.5 V	7.0	20.0	48.0	ms
Over-current release delay time	tr3	$V_{DD} - Vc$ = 3.5 V, $Vc - V_{SS}$ = 3.5 V	0.35	1.0	2.4	ms
Short circuit detection voltage	Vd4	$V_{DD} - Vc$ = 3.5 V, $Vc - V_{SS}$ = 3.5 V	0.9	1.3	1.7	V
Short circuit detection delay time	td4	$V_{DD} - Vc$ = 3.5 V, $Vc - V_{SS}$ = 3.5 V	0.049	0.250	0.800	ms
Excessive charger detection voltage	Vd5	$V_{DD} - Vc$ = 3.5 V, $Vc - V_{SS}$ = 3.5 V (V−) − V_{SS} between voltage	−0.70	−0.45	−0.20	V
Release hysteresis voltage	Vh5	$V_{DD} - Vc$ = 3.5 V, $Vc - V_{SS}$ = 3.5 V	21.0	50.0	112.0	mV
Stand−by release voltage	Vstb	$V_{DD} - Vc$ = 2.0 V, $Vc - V_{SS}$ = 2.0 V (V−) − V_{SS} between voltage	$V_{DD} \times 0.4$	$V_{DD} \times 0.5$	$V_{DD} \times 0.6$	V
Excessive charger detection delay time	td5	$V_{DD} - Vc$ = 3.5 V, $Vc - V_{SS}$ = 3.5 V (Note 5)	0.35	1.5	4.8	ms
Excessive charger release delay time	tr5	$V_{DD} - Vc$ = 3.5 V, $Vc - V_{SS}$ = 3.5 V	0.35	1.5	4.8	ms
Internal resistance (VM−V_{DD})	R_{DD}	When overcharge is detected	70	200	520	kΩ
Internal resistance (VM−VSS)	R_{SS}	When over current or short circuit is detected	10.5	30	78	kΩ
Cout Nch ON voltage	V_OL1	I_OL = 50 µA, $V_{DD} - Vc$ = 4.4 V, $Vc - V_{SS}$ = 4.4 V			0.5	V
Cout Pch ON voltage	V_OH1	I_OL = 50 µA, $V_{DD} - Vc$ = 3.9 V, $Vc - V_{SS}$ = 3.9 V	$V_{DD} - 0.5$			V
Dout Nch ON voltage	V_OL2	I_OL = 50 µA, $V_{DD} - Vc$ = 2.2 V, $Vc - V_{SS}$ = 2.2 V			0.5	V
Dout Pch ON voltage	V_OH2	I_OL = 50 µA, $V_{DD} - Vc$ = 3.9 V, $Vc - V_{SS}$ = 3.9 V	$V_{DD} - 0.5$			V
Vc input current	Ivc	$V_{DD} - Vc$ = 3.5 V, $Vc - V_{SS}$ = 3.5 V		0.0	1.0	µA
Current consumption	I_{DD}	$V_{DD} - Vc$ = 3.5 V, $Vc - V_{SS}$ = 3.5 V		6.0	16.9	µA
Stand−by current	Istb	$V_{DD} - Vc$ = 2.2 V, $Vc - V_{SS}$ = 3.5 V			0.2	µA
T−terminal input ON voltage	Vtest	$V_{DD} - Vc$ = 3.5 V, $Vc - V_{SS}$ = 3.5 V	$V_{DD} \times 0.4$	$V_{DD} \times 0.5$	$V_{DD} \times 0.6$	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
5. Over charge detection to over discharge battery is It is delay time from after over-discharge return.
6. This specification value is the design target value and does not check at production test.
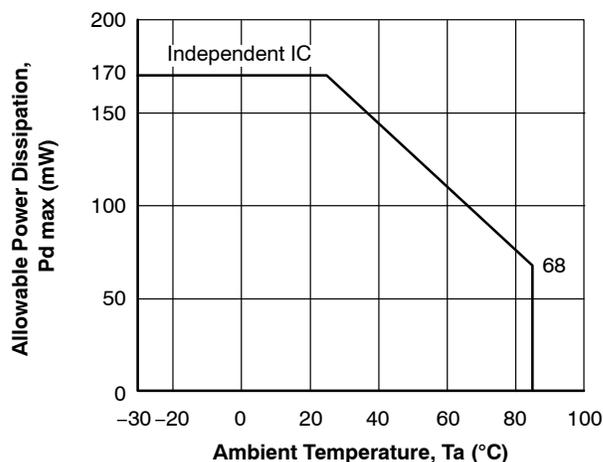

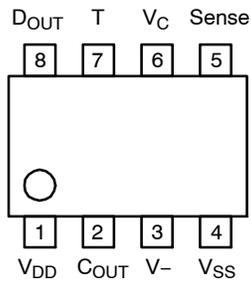
Figure 1. Pd max vs. Ta

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PIN ASSIGNMENT

Figure 2. Pin Assignment (Top View)

PIN FUNCTION

Pin No.	Symbol	Description
1	V_{DD}	V_{DD} pin
2	C_{OUT}	Overcharge detection output pin
3	V^-	Charger minus voltage input pin
4	V_{SS}	V_{SS} pin
5	Sense	Sense pin
6	Vc	Intermediate voltage input pin
7	T	Pin to shorten detection time ([H]: Shortening mode, [L] or [open]: normal mode)
8	D_{OUT}	Over-discharge detection output pin

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BLOCK DIAGRAM
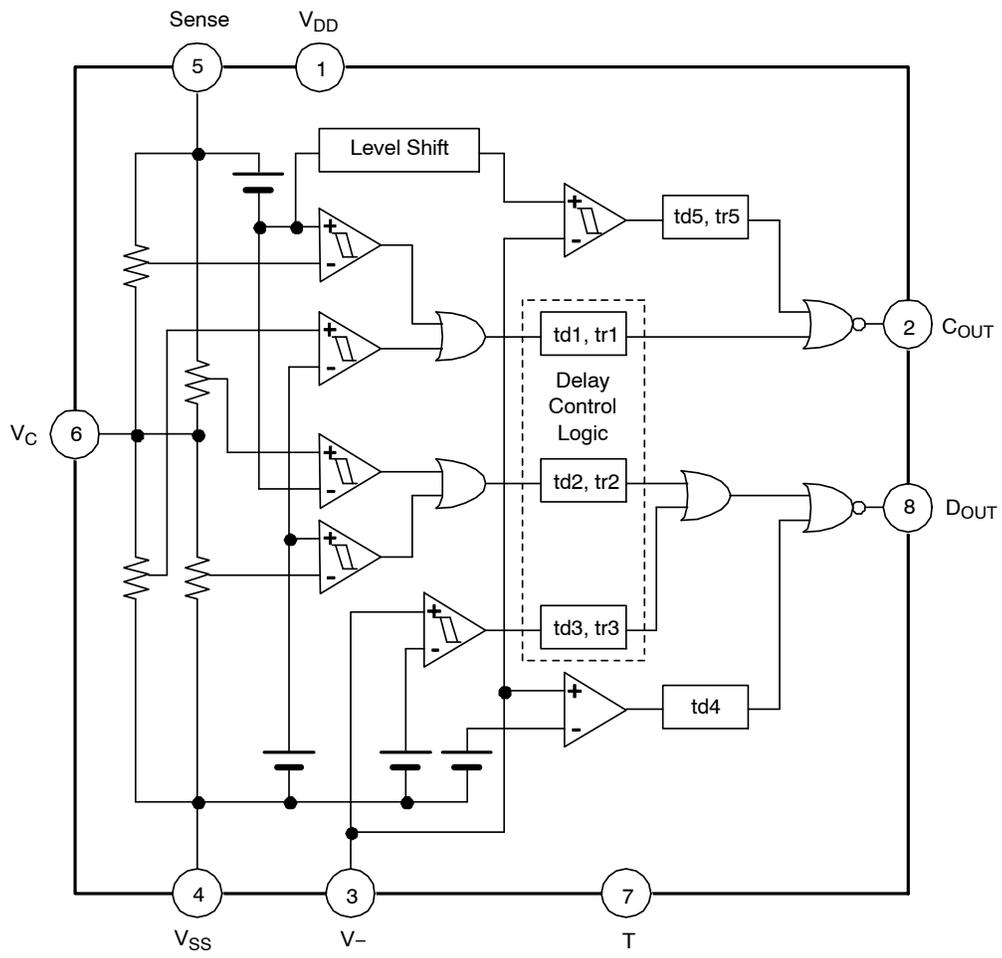
Figure 3. Block Diagram

FUNCTIONAL DESCRIPTION

Over-charge Detection

If either of the cell voltage is equal to or more than the over-charge detection voltage, stop further charging by turning "L" the Cout pin and turning off external Nch MOS FET after the over-charge detection delay time. This delay time is set by the internal counter.

The over−charge detection comparator has the hysteresis function. Note that this hysteresis can be cancelled by connecting the load after detection of over-charge detection, and hysteresis become decrease to value peculiar to comparator.

Once over-charge detection is made, over-current detection is not made to prevent malfunction. Note that short-circuit can be detected.

Over-charge Return

If charger is connected and both cell voltages become equal to or lower than the over-charge recovery voltage or over-charge detection voltage when load is connected, the Cout pin returns to "H" after the over-charge recovery delay time set by the internal counter.

When load is connected and either cell or both cell voltages are equal to or more than the over-charge detection voltage, the Cout pin does not return to "H." When the load current is passed through the external Cout pin parasite diode of Nch MOS FET after the over-charge recovery delay time and each cell voltage becomes equal to or below over-charge detection voltage, the Cout returns to "H."

However, high voltage charger is connected as mentioned below, Cout pin does not return to "H" because over-charger detection sequence starts after over-charge recovery.

Over-discharge Detection

When either cell voltage is equal to or below over-discharge voltage, stop further discharge by turning "L" the Dout pin and turning off external Nch MOS FET after the over-charge detection delay time.
The IC becomes standby state after detecting over-discharge and its consumption current is kept at about 0 A. After detection, the V^- pin will be connected to V_{DD} pin via 200 kΩ.

Over-discharge Return

Return from over-discharge is made by connecting charger. If the V^- pin voltage becomes equal to or lower than the standby return voltage by connecting charger after detecting over-discharge, it returns from the standby state to start cell voltage monitoring. If both voltages become equal to or more than the over-discharge detection voltage by charging, the Dout pin returns to "H" after the over-discharge return delay time set by the internal counter.

Over-current Detection

When high current is passed through the battery, the V potential rises by the ON resister of external MOS FET and becomes equal to or more than the over-current detection

voltage, that will be deemed over-current state. Turn "L" the Dout pin after the over-current detection delay time and turn off the external Nch MOS FET to prevent high current in the circuit. The delay time is set by the internal counter. After detection, the V^- pin will be connected to V_{SS} via 30 kΩ. It will not go into standby state after detecting over-current.

Short Circuit Detection

If greater discharge current is passed and the V^- pin voltage becomes equal to or more than the short-circuit detection voltage, it will go into short-circuit detection state after the short circuit delay time shorter than the over-current detection delay time. When short-circuit is detected, just like the time of over-current detection, turn Dout pin "L" and turn off external Nch MOS FET to prevent high current in the circuit. The V^- pin will be connected to V_{SS} after detection via 30 kΩ. It will not go into standby state after detecting short-circuit.

Over-current/Short-detection Return

After detecting over-current or short circuit, the return resistor (typ. 30 kΩ) between V^- pin and V_{SS} pin becomes effective and if the resistor is opened the V^- pin voltage will be pulled by the V_{SS} pin voltage. Thereafter, the IC will return from the over-current/short-circuit detection state when the V^- pin voltage becomes equal to or below the over-current detection voltage and the Dout pin returns to "H" after over-current return delay time set by the internal counter.

Over-charger Detection/Return

If the potential difference between V^- pin and V_{SS} pin becomes equal to or below the over-charger detection voltage by connecting a charger, no charging can be made by turning "L" the Cout pin after certain delay time and turning off the external Nch MOS FET. If this difference returns to equal to or more than the over-charger detection voltage during detection delay time, the over-charger detection will be stopped. If the potential difference between V^- pin and V_{SS} pin becomes equal to or more than the over-charger detection voltage after over-charger detection, the Cout returns to "H" after certain time. The detection/return delay time is set internally.

If Dout pin is "L" charging will be made through the external Nch FET parasite diode of Dout pin. In that case, the potential difference between V^- pin and V_{SS} pin becomes −Vf which is equal to or less than the over-charger detection voltage, no over-charger detection will be made during over-discharge, over-current or short-circuit detection. Further, if over-discharged battery is connected to over-charger, no over-charger detection is made while the Dout pin is "L."

If the battery voltage rises to the over-discharge detection voltage through the parasite diode and the Dout pin becomes "H", and the potential difference between V^- pin and V_{SS}

pin is equal to or below the over-charger detection voltage, the delay operation will be started after Dout pin becoming "H."

0 V Cell Charge

If the cell voltage is 0 V but a potential difference between V_{DD} and V becomes equal to or greater than the 0 V cell charging lowest operation voltage, the Cout pin will output "H" and enable charging.

Test Time Reduction Function

By turning T pin to the V_{DD} potential, the delay times set by the counter can be cut. Normal time settings if T pin is open. Delay time not set by the counter cannot be controlled by this pin. Recommend that connect the T terminal to VSS terminal if it is possible. Because the malfunction such as it becoming a standby mode by the power supply voltage drop caused by the excessive electric current at the time of load short circuits is assumed by a board layout.

OPERATION IN CASE OF DETECTION OVERLAP

OPERATION IN CASE OF DETECTION OVERLAP

Overlap State		Operation in Case of Detection Overlap	State after Detection
When, during over-charge detection	Over-discharge detection is made	Over-charge detection is preferred. If over-discharge state continues even after over-charge detection, over-discharge detection is resumed.	When over-charge detection is made first, V⁻ is released. When over-discharge is detected after over-charge detection, the standby state is not effectuated. Note that V⁻ is connected to V_{DD} via 200 kΩ.
	Over-current detection is made	(*1) Both detections' can be made in parallel. Over-charge detection continues even when the over-current state occurs. If the over-charge state occurs first, over-current detection is interrupted.	(*2) When over-current is detected first, V⁻ is connected to V_{SS} via 30 kΩ. When over-charge detection is made first, V⁻ is released.
When, during over-discharge detection	Over-charge detection is made	Over-discharge detection is interrupted and over-charge detection is preferred. When over-discharge state continues even after over-charge detection, over-discharge detection is resumed.	The standby state is not effectuated when over-discharge detection is made after over-charge detection. Note that V⁻ is connected to V_{DD} via 200 kΩ.
	Over-current detection is made	(*3) Both detections can be made in parallel. Over-discharge detection continues even when the over-current state is effectuated first. Over-current detection is interrupted when the over-discharge state is effectuated first,	(*4) If over-current is detected in advance, V will be connected to V_{SS} via 30 kΩ. After detecting over-discharge, V will be connected to V_{DD} via 200 kΩ to get into standby state. If over-discharge is detected in advance, V will be connected to V_{DD} via 200 kΩ to get into standby state.
When, during over-current detection	Over-charge detection is made	(*1)	(*2)
	Over-discharge detection is made	(*3)	(*4)

NOTE: Short-circuit detection can be made independently.
Over-charger detection does not work during over-discharge, over-current or short-circuit detection and the delay time starts after return from these states.
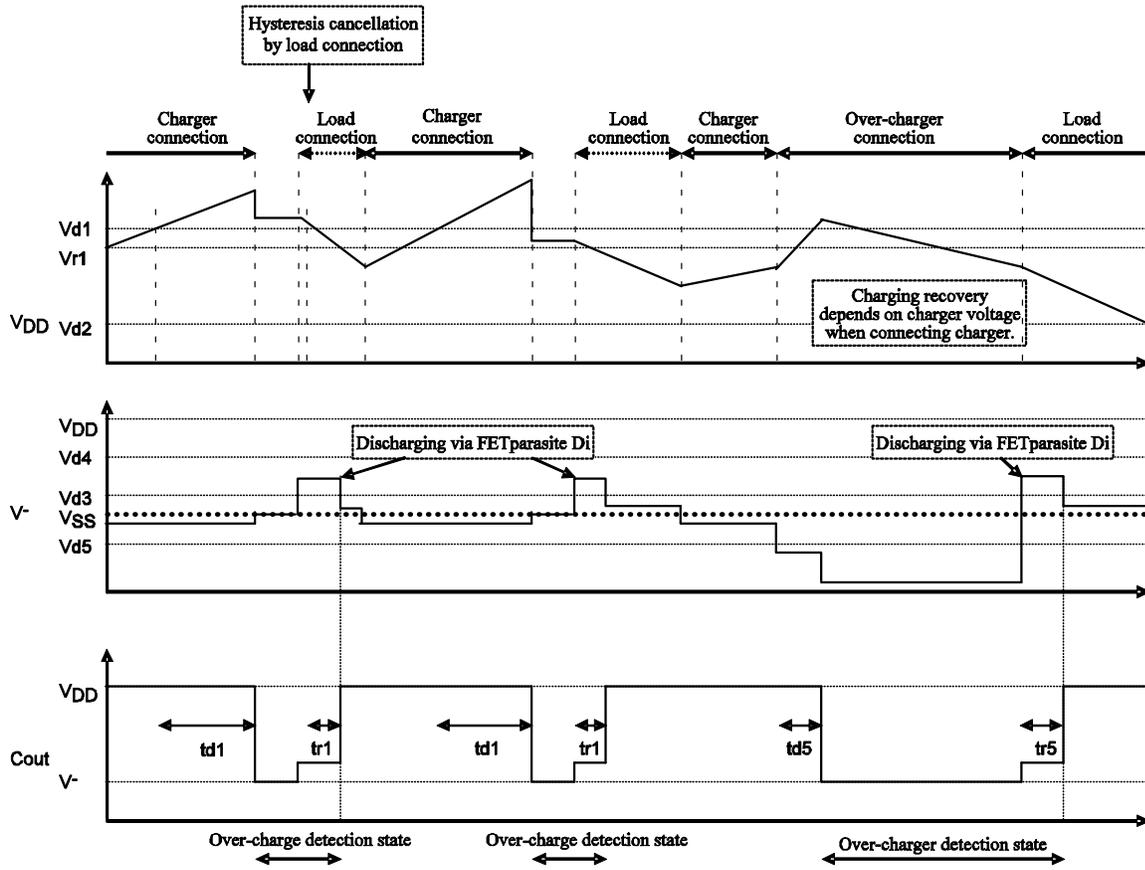
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TIMING CHART

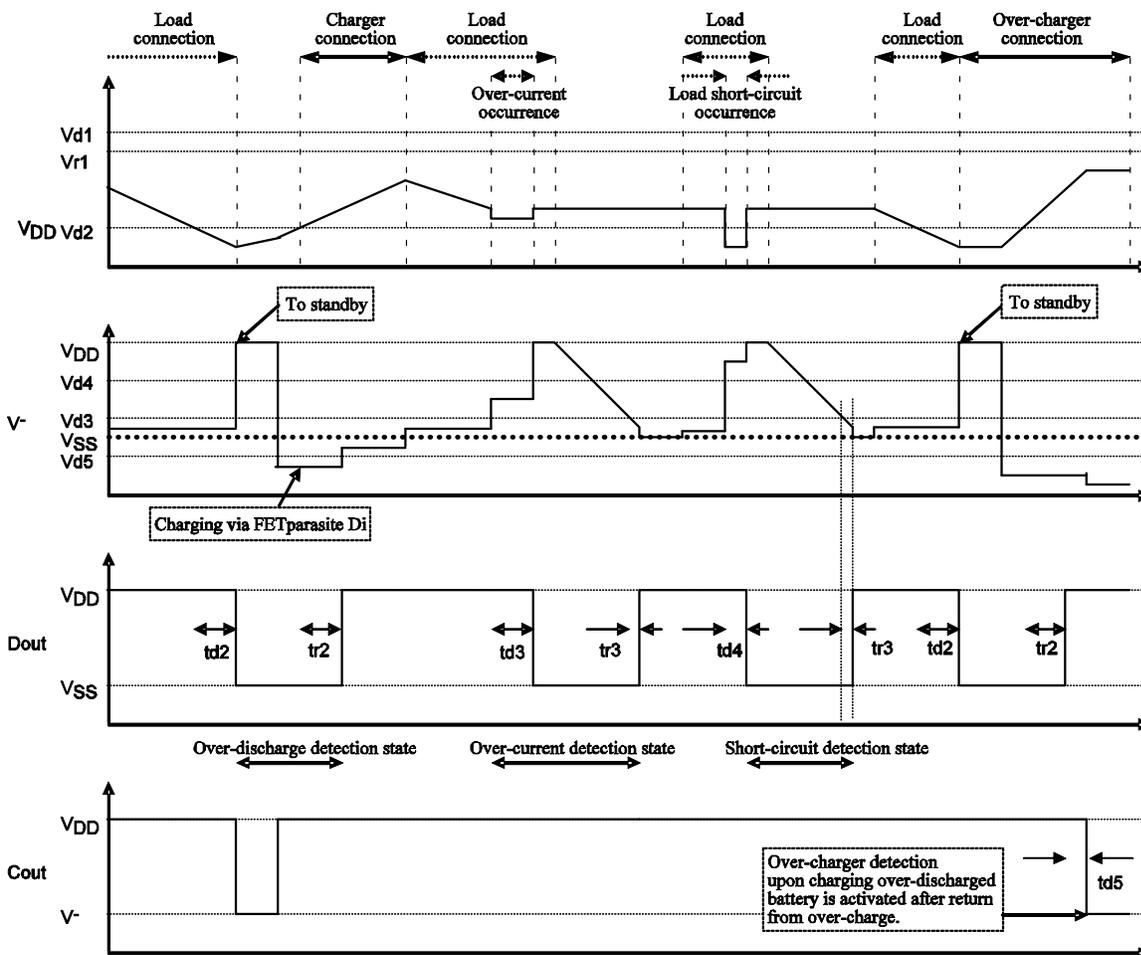
Figure 4. C$_{OUT}$ Output System

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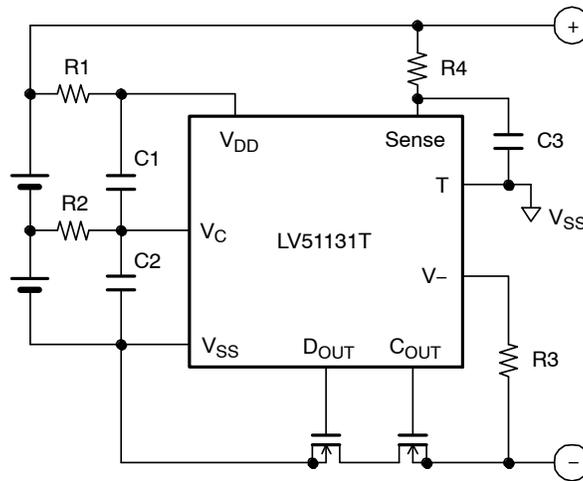**Figure 5. D$_{OUT}$ Output System**

APPLICATION CIRCUIT EXAMPLE

Figure 6. Application Circuit Example

Components	Recommended Value	Max	Unit
R1, R2	100	500	Ω
R3	2	4	$k\Omega$
R4	100	500	Ω
C1, C2, C3	0.1	1	μF

*These numbers don't mean to guarantee the characteristic of the IC.
*In addition to the components in the upper diagram, it is necessary to insert a capacitor with enough capacity between V_{DD} and V_{SS} of the IC as near as possible to stabilize the power supply voltage to the IC.

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PACKAGE DIMENSIONS

Micro8 / MSOP8 (150 mil)
CASE 846AH
ISSUE A

3.4 MAX

3.0±0.1

8

3.0±0.1

4.9±0.25

(0.53)

1   2

0.65

0.25 +0.05 −0.04

⊕ 0.10 Ⓜ

0~10°

0.5±0.2

0.125 +0.07 −0.02

1.1 MAX

(0.85)

0.08 +0.1 −0.05

◁ 0.10
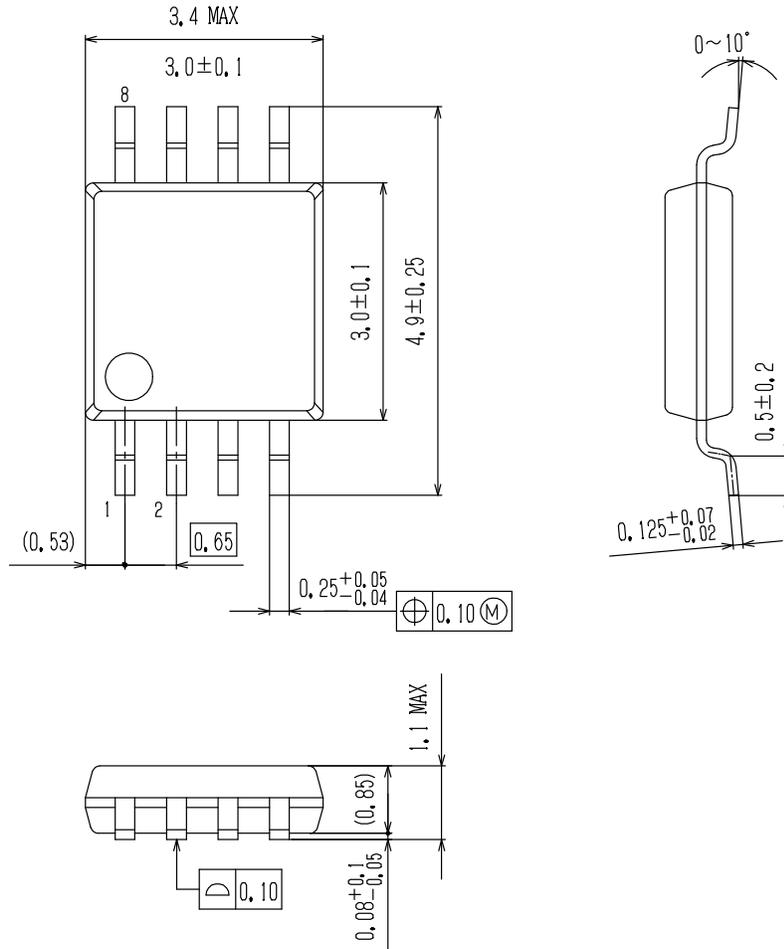
SOLDERING FOOTPRINT*

4.30

1.0

(Unit: mm)

0.35

0.65
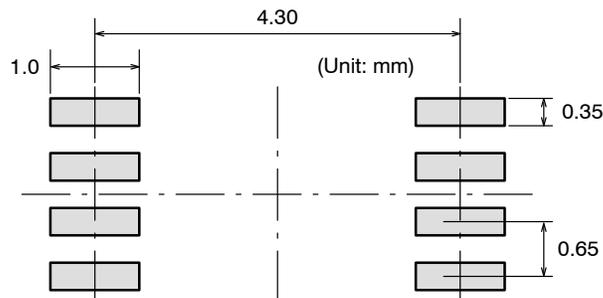
NOTE: The measurements are not to guarantee but for reference only.

*For additional information on our Pb−Free strategy and soldering
details, please download the ON Semiconductor Soldering and
Mounting Techniques Reference Manual, SOLDERRM/D.

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PUBLICATION ORDERING INFORMATION

◊   **LV51131T/D**