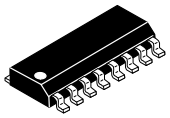
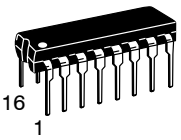
PFC/PWM Controller Combination

FAN4800AS/CS/01S/2S

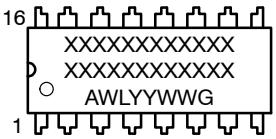


SOIC−16
CASE 751BG



PDIP−16
CASE 648−08

MARKING DIAGRAM



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information on page 16 of this data sheet.

Description

The highly integrated FAN4800AS/CS/01S/02S parts are specially designed for power supplies that consist of boost PFC and PWM. They require very few external components to achieve versatile protections / compensation. They are available in 16−pin DIP and SOP packages.

The PWM can be used in either current or voltage mode. In voltage mode, feed−forward from the PFC output bus can reduce the secondary output ripple.

Compared with older productions, ML4800 and FAN4800, FAN4800AS/CS/01S/02S have lower operation current that saves power consumption in external devices. FAN4800AS/CS/01S/02S have accurate 49.9% maximum duty of PWM that makes the hold−up time longer. Brownout protection and PFC soft−start functions available in this series are not available in ML4800 and FAN4800.

To evaluate FAN4800AS/CS/01S/02S for replacing existing FAN4800 and ML4800 boards, five things must be completed before the fine−tuning procedure:

1. Change R_{AC} resister from the old value to a higher resister: between 6 MΩ to 8 MΩ.
2. Change RT/CT pin from the existing values to R_T = 6.8kW and C_T = 1000 pF to have f_{PFC} = 64 kHz and f_{PWM} = 64 kHz.
3. The VRMS pin needs to be 1.224 V at V_{IN} = 85 V_{AC} for universal input application from line input from 85 V_{AC} to 270 V_{AC}.
4. At full load, the average V_{VEA} needs to be ~4.5 V and the ripple of V_{VEA} needs to be less than 400 mV.
5. For the Soft−Start pin, the soft−start current has been reduced to half the FAN4800 capacitor.

There are two differences from FAN4800A/C/01/02 to FAN4800AS/CS/01S/02S:

1. Under−voltage protection debounce time is extended to one second.
2. PWM gate clamp voltage is raised to 19 V.

Features

- Pin−to−Pin Compatible with ML4800 and FAN4800 and CM6800 and CM6800A
- PWM Configurable for Current Mode or Feedforward Voltage−Mode Operation
- Internally Synchronized Leading−Edge PFC and Trailing−Edge PWM in One IC
- Low Operating Current
- Innovative Switching−Charge Multiplier Divider
- Average−Current Mode for Input−Current Shaping
- PFC Over−Voltage and Under−Voltage Protections
- PFC Feedback Open−Loop Protection
- Cycle−by−Cycle Current Limiting for PFC/PWM
- Power−on Sequence Control and Soft−Start
- Brownout Protection
- Interleaved PFC/PWM Switching
- Improved Efficiency at Light Load
- $f_{RTCT} = 4 \cdot f_{PFC} = 4 \cdot f_{PWM}$ for FAN4800AS/01S
- $f_{RTCT} = 4 \cdot f_{PFC} = 2 \cdot f_{PWM}$ for FAN4800CS/02S
- These are Pb−Free Devices

Applications

- Desktop PC Power Supply
- Internet Server Power Supply
- LCD TV, Monitor Power Supply
- UPS
- Battery Charger
- DC Motor Power Supply
- Monitor Power Supply
- Telecom System Power Supply
- Distributed Power

Related Resources

- AN−8027 − FAN480X PFC+PWM Combination Controller Application

Application Diagram

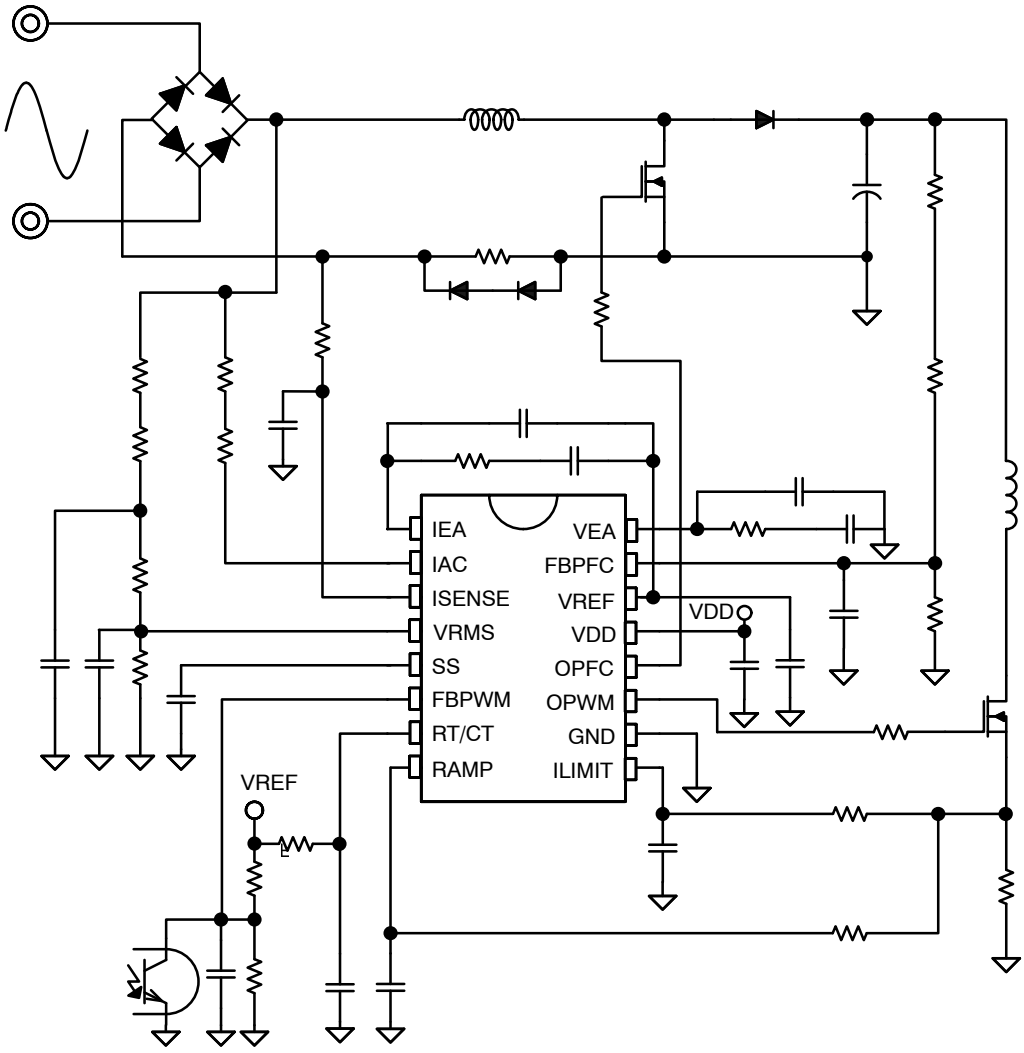


Figure 1. Typical Application, Current Mode

Application Diagram

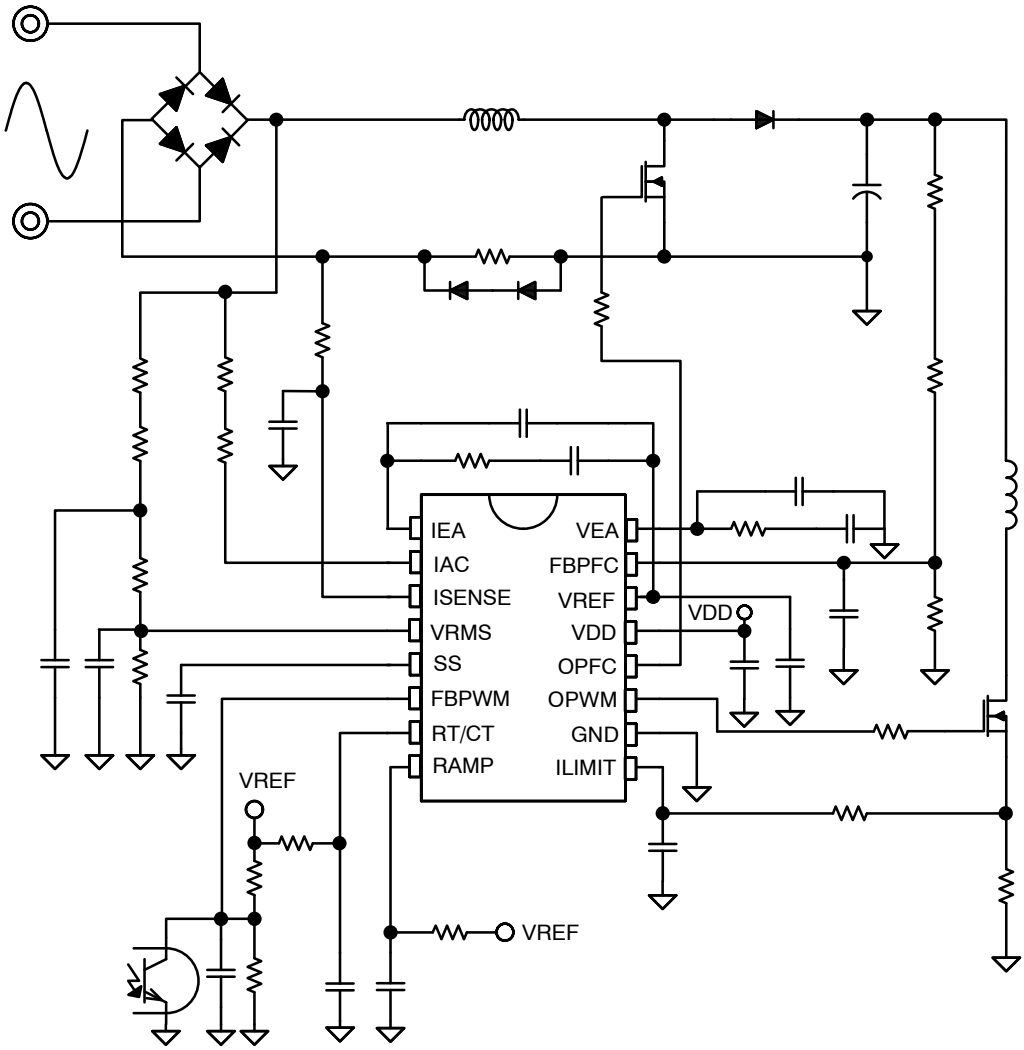


Figure 2. Typical Application, Voltage Mode

Block Diagram

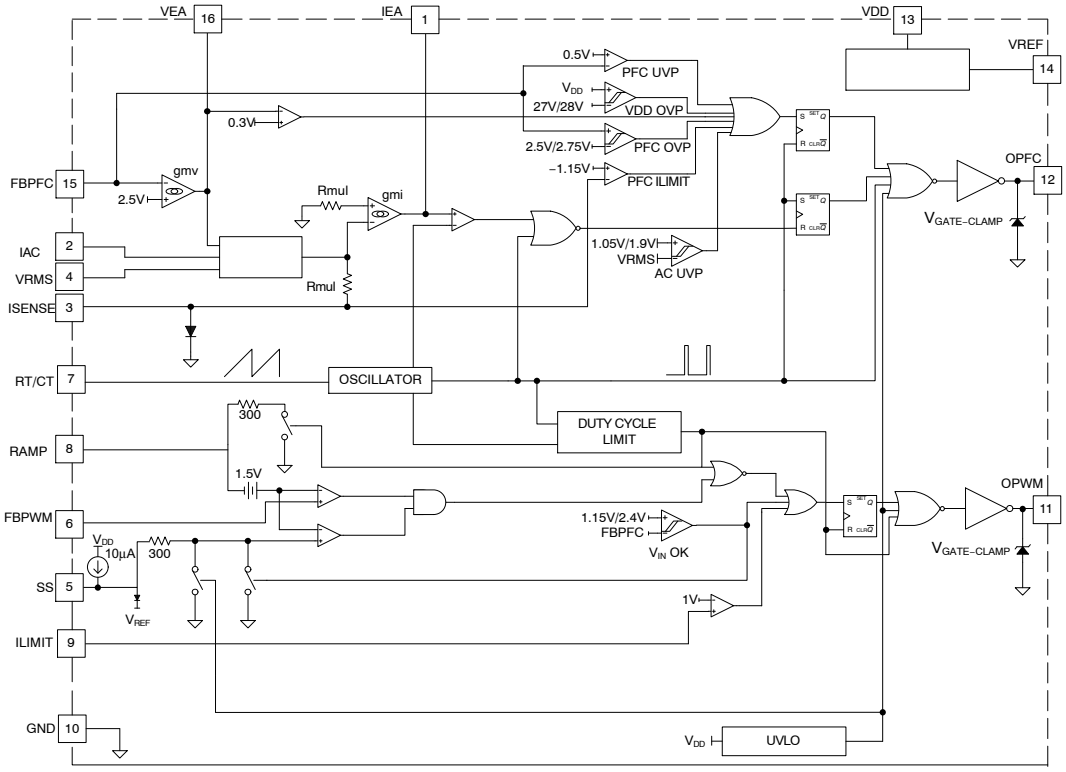


Figure 3. FAN4800AS/CS Function Block Diagram

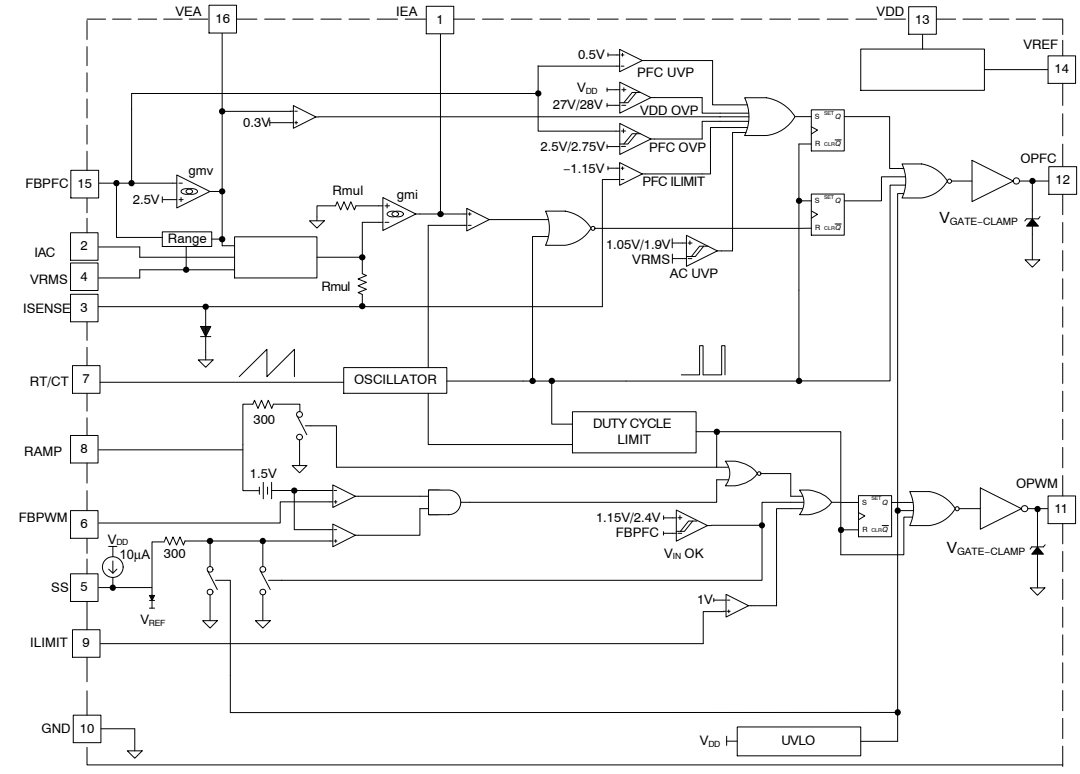


Figure 4. FAN4801S/02S Function Block Diagram

Pin Configuration

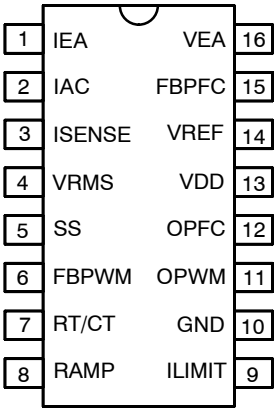


Figure 5. Pin Configuration (Top View)

Table 1. PIN DEFINITIONS

Pin No.	Name	Description
1	IEA	Output of PFC Current Amplifier. The signal from this pin is compared with an internal sawtooth to determine the pulse width for PFC gate drive.
2	IAC	Input AC Current. For normal operation, this input provides current reference for the multiplier. The suggested maximum IAC is 100 mA.
3	ISENSE	PFC Current Sense. The non−inverting input of the PFC current amplifier and the output of multiplier and PFC ILIMIT comparator.
4	VRMS	Line−Voltage Detection. The pin is used for the PFC multiplier.
5	SS	PWM Soft−Start. During startup, the SS pin charges an external capacitor with a 10 mA constant current source. The voltage on FBPWM is clamped by SS during startup. If a protection condition occurs and/or PWM is disabled, the SS pin is quickly discharged.
6	FBPWM	PWM Feedback Input. The control input for voltage−loop feedback of PWM stage.
7	RC/CT	Oscillator RC Timing Connection. Oscillator timing node; timing set by R_T and C_T.
8	RAMP	PWM RAMP Input. In current mode, this pin functions as the current−sense input; when in voltage mode, it is the feedforward sense input from PFC output 380 V (feedforward ramp).
9	ILIMIT	Peak Current Limit Setting for PWM. The peak current limits setting for PWM.
10	GND	Ground.
11	OPWM	PWM Gate Drive. The totem−pole output drive for PWM MOSFET. This pin is internally clamped under 19 V to protect the MOSFET.
12	OPFC	PFC Gate Drive. The totem−pole output drive for PFC MOSFET. This pin is internally clamped under 15 V to protect the MOSFET.
13	VDD	Supply. The power supply pin. The threshold voltages for startup and turn−off are 11 V and 9.3 V, respectively. The operating current is lower than 10 mA.
14	VREF	Reference Voltage. Buffered output for the internal 7.5 V reference.
15	FBPFC	Voltage Feedback Input for PFC. The feedback input for PFC voltage loop. The inverting input of PFC error amplifier. This pin is connected to the PFC output through a divider network.
16	VEA	Output of PFC Voltage Amplifier. The error amplifier output for PFC voltage feedback loop. A compensation network is connected between this pin and ground.

Table 2. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Min	Max	Unit
V_{DD}	DC Supply Voltage		–	30	V
V_H	SS, FBPWM, RAMP, OPWM, OPFC, VREF		−0.3	30.0	V
V_L	IAC, VRMS, RT/CT, ILIMIT, FBPFC, VEA		−0.3	7.0	V
V_{IEA}	IEA		0	VREF +0.3	V
V_N	ISENSE		−5.0	0.7	V
I_{AC}	Input AC Current		–	1	mA
I_{REF}	V_{REF} Output Current		–	5	mA
$I_{PFC-OUT}$	Peak PFC OUT Current, Source or Sink		–	0.5	A
$I_{PWM-OUT}$	Peak PWM OUT Current, Source or Sink		–	0.5	A
P_D	Power Dissipation T_A < 50°C		–	800	mW
θ_{JA}	Thermal Resistance (Junction−to−Air)	DIP	–	80.80	°C/W
		SOP	–	104.10	
θ_{JC}	Thermal Resistance (Junction−to−Case)	DIP	–	35.38	°C/W
		SOP	–	41.41	
T_J	Operating Junction Temperature		−40	+125	°C
T_{STG}	Storage Temperature Range		−55	+150	°C
T_L	Lead Temperature (Soldering)		–	+260	°C
ESD	Electrostatic Discharge Capability	Human Body Model	–	5.0	kV
		Charged Device Model	–	1.5	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. All voltage values, except differential voltages, are given with respect to GND pin.
2. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.

Table 3. RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
T_A	Operating Ambient Temperature	−40	+105	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 4. ELECTRICAL CHARACTERISTICS

(Unless otherwise noted, V_{DD} = 15 V, T_A = 25°C, T_A = T_J, R_T = 6.8 kΩ, and C_T = 1000 pF)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{DD} SECTION						
V_{DD-OP}	Continuously Operating Voltage		–	–	26	V
I_{DD-ST}	Startup Current	V_{DD} = V_{TH-ON} – 0.1 V, OPFC OPWM Open	–	30	80	μA
I_{DD-OP}	Operating Current	V_{DD} = 13 V, OPFC OPWM Open	2.0	2.6	5.0	mA
V_{TH-ON}	Turn−On Threshold Voltage		10	11	12	V
ΔV_{TH}	Hysteresis		1.3	–	1.9	V
V_{DD-OVP}	V_{DD} OVP		27	28	29	V
ΔV_{DD-OVP}	V_{DD} OVP Hysteresis		–	1	–	V
OSCILLATOR						
$f_{OSC-RT/CT}$	RT/CT Frequency	R_T = 6.8 kΩ, C_T = 1000 pF	240	256	268	kHz
f_{OSC}	PFC & PWM Frequency	R_T = 6.8 kΩ, C_T = 1000 pF	60	64	67	kHz
	PWM Frequency		120	128	134	
f_{DV}	Voltage Stability (Note 3)	11 V ≤ V_{DD} ≤ 22 V	–	–	2	%
f_{DT}	Temperature Stability (Note 3)	−40°C ~ +105°C	–	–	2	%
f_{TV}	Total Variation (PFC & PWM) (Note 3)	Line, Temperature	58	–	70	kHz
f_{RV}	Ramp Voltage	Valley to Peak	–	2.8	–	V
$I_{OSC-DIS}$	Discharge Current	V_{RAMP} = 0 V, $V_{RT/CT}$ = 2.5 V	6.5	–	15.0	mA
f_{RANGE}	Frequency Range		50	–	75	kHz
$t_{PFC-DEAD}$	PFC Dead Time	R_T = 6.8 kΩ, C_T = 1000 pF	400	600	800	ns
V_{REF}						
V_{VREF}	Reference Voltage	I_{REF} = 0 mA, C_{REF} = 0.1 μF	7.4	7.5	7.6	V
ΔV_{VREF1}	Load Regulation of Reference Voltage	C_{REF} = 01 μF, I_{REF} = 0 mA to 3.5 mA V_{VDD} = 14 V, Rise/Fall Time > 20 μs	–	30	50	mV
ΔV_{VREF2}	Line Regulation of Reference Voltage	C_{REF} = 0.1 F, V_{VDD} = 11 V to 22 V	–	–	25	mV
$\Delta V_{VREF-DT}$	Temperature Stability (Note 3)	−40°C ~ +105°C	–	0.4	0.5	%
$\Delta V_{VREF-TV}$	Total Variation (Note 3)	Line, Load, Temp	7.35	–	7.65	V
$\Delta V_{VREF-LS}$	Long−Term Stability (Note 3)	T_J = 125°C, 0 ~ 1000 HRs	5	–	25	mV
$I_{REF-MAX}$	Maximum Current	V_{VREF} > 7.35 V	5	–	–	mA
PFC OVP COMPARATOR						
$V_{PFC-OVP}$	Over−Voltage Protection		2.70	2.75	2.80	V
$\Delta V_{PFC-OVP}$	PFC OVP Hysteresis		200	250	300	mV
LOW−POWER DETECT COMPARATOR						
V_{VEAOFF}	VEA Voltage OFF OPFC		0.2	0.3	0.4	V
V_{IN} OK COMPARATOR						
$V_{RD-FBPFC}$	Voltage Level on FBPFC to Enable OPWM During Startup		2.3	2.4	2.5	V
$\Delta V_{RD-FBPFC}$	Hysteresis		1.15	1.25	1.35	V

Table 4. ELECTRICAL CHARACTERISTICS (continued)
(Unless otherwise noted, V_{DD} = 15 V, T_A = 25°C, T_A = T_J, R_T = 6.8 kΩ, and C_T = 1000 pF)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
VOLTAGE ERROR AMPLIFIER						
V_{REF}	Reference Voltage		2.45	2.50	2.55	V
A_V	Open−Loop Gain (Note 3)		35	42	–	dB
Gm_v	Transconductance	V_{NONINV} = V_{INV}, V_{VEA} = 3.75 V	50	70	90	umho
$I_{FBPFC-L}$	Maximum Source Current	V_{FBPFC} = 2 V, V_{VEA} = 1.5 V	40	50	–	μA
$I_{FBPFC-H}$	Maximum Sink Current	V_{FBPFC} = 3 V, V_{VEA} = 6 V	–	−50	−40	μA
I_{BS}	Input Bias Current		−1	–	1	μA
V_{VEA-H}	Output High Voltage on V_{VEA}		5.8	6.0	–	V
V_{VEA-L}	Output Low Voltage on V_{VEA}		–	0.1	0.4	V
CURRENT ERROR AMPLIFIER						
Gm_I	Transconductance	V_{NONINV} = V_{INV}, V_{IEA} = 3.75 V	78	88	100	umho
V_{OFFSET}	Input Offset Voltage	V_{VEA} = 0 V, IAC Open	−10	–	10	mV
V_{IEA-H}	Output High Voltage		6.8	7.4	8.0	V
V_{IEA-L}	Output Low Voltage		–	0.1	0.4	V
I_L	Source Current	V_{ISENSE} = −0.6 V, V_{IEA} = 1.5 V	35	50	–	μA
I_H	Sink Current	V_{ISENSE} = +0.6 V, V_{IEA} = 4.0 V	–	−50	−35	μA
A_I (Note 3)	Open−Loop Gain		40	50	–	dB
TriFault Detect™						
t_{FBPFC_OPEN}	Time to FBPFC Open	V_{FBPFC} = $V_{PFC-UVP}$ to FBPFC OPEN, 470 pF from FBPFC to GND	–	2	4	ms
$V_{PFC-UVP}$	PFC Feedback Under−Voltage Protection		0.4	0.5	0.6	V
GAIN MODULATOR						
I_{AC}	Input for AC Current (Note 3)	Multiplier Linear Range	0	–	100	μA
GAIN	GAIN Modulator (Note 4)	I_{AC} = 17.67 μA, V_{RMS} = 1.080 V V_{FBPFC} = 2.25 V	7.500	9.000	10.500	
		I_{AC} = 20.00 μA, V_{RMS} = 1.224 V V_{FBPFC} = 2.25 V	6.367	7.004	7.704	
		I_{AC} = 25.69 μA, V_{RMS} = 1.585 V V_{FBPFC} = 2.25 V	3.801	4.182	4.600	
		I_{AC} = 51.62 μA, V_{RMS} = 3.169 V V_{FBPFC} = 2.25 V	0.950	1.045	1.149	
		I_{AC} = 62.23 μA, V_{RMS} = 3.803 V V_{FBPFC} = 2.25 V	0.660	0.726	0.798	
BW	Bandwidth (Note 3)	I_{AC} = 40 μA	–	2	–	kHz
V_o(gm)	Output Voltage = 5.7 kΩ x (I_{SENSE} − I_{OFFSET})	I_{AC} = 20 μA, V_{RMS} = 1.224 V V_{FBPFC} = 2.25 V	0.710	0.798	0.885	V
PFC I_{LIMIT} COMPARATOR						
$V_{PFC-ILIMIT}$	Peak Current Limit Threshold Voltage, Cycle−by−Cycle Limit		−1.35	−1.20	−1.05	V
ΔV_{PK}	PFC I_{LIMIT}−Gain Modulator Output	I_{AC} = 17.67 μA, V_{RMS} = 1.08 V V_{FBPFC} = 2.25 V	200	–	–	mV

Table 4. ELECTRICAL CHARACTERISTICS (continued)
(Unless otherwise noted, V_{DD} = 15 V, T_A = 25°C, T_A = T_J, R_T = 6.8 kΩ, and C_T = 1000 pF)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
PFC OUTPUT DRIVER						
$V_{GATE-CLAMP}$	Gate Output Clamping Voltage	V_{DD} = 22 V	13	15	17	V
V_{GATE-L}	Gate Low Voltage	V_{DD} = 15 V, I_O = 100 mA	–	–	1.5	V
V_{GATE-H}	Gate High Voltage	V_{DD} = 13 V, I_O = 100 mA	8	–	–	V
t_R	Gate Rising Time	V_{DD} = 15 V, C_L = 4.7 nF, O/P = 2 V to 9 V	40	70	120	ns
t_F	Gate Falling Time	V_{DD} = 15 V, C_L = 4.7 nF, O/P = 9 V to 2 V	40	60	110	ns
$D_{PFC-MAX}$	Maximum Duty Cycle	V_{IEA} < 1.2 V	94	97	–	%
$D_{PFC-MIN}$	Minimum Duty Cycle	V_{IEA} > 4.5 V	–	–	0	%
BROWNOUT						
$V_{RMS-UVL}$	V_{RMS} Threshold Low	When V_{RMS} = 1.05 V at 75 V_{RMS}	1.03	1.05	1.08	V
$V_{RMS-UVH}$	V_{RMS} Threshold High	When V_{RMS} = 1.9 V at 85 · 1.414	1.88	1.90	1.94	V
$V_{RMS-UVP}$	Hysteresis		750	850	950	mV
t_{UVP}	Under Voltage Protection Debounce Time		850	1000	1150	ms
SOFT START						
V_{SS-MAX}	Maximum Voltage	V_{DD} = 15 V	9.5	10.0	10.5	V
I_{SS}	Soft−Start Current		–	10	–	μA
PWM I_{LIMIT} COMPATOR						
$V_{PWM-LIMIT}$	Threshold Voltage		0.95	1.00	1.05	V
t_{PD}	Propagation Delay to Output		–	250	–	ns
$t_{PWM-BNK}$	Leading−Edge Blanking Time		170	250	350	ns
RANGE (FAN4801S/02S)						
V_{VRMS-L}	RMS AC Voltage Low	When V_{VRMS} = 1.95 V at 132 V_{RMS}	1.90	1.95	2.00	V
V_{VRMS-H}	RMS AC Voltage High	When V_{VRMS} = 2.45 V at 150 V_{RMS}	2.40	2.45	2.50	V
V_{VEA-L}	VEA LOW	When V_{VEA} = 1.95 V at 30% Loading	1.90	1.95	2.00	V
V_{VEA-H}	VEA HIGH	When V_{VEA} = 2.45 V at 40% Loading	2.40	2.45	2.50	V
I_{TC}	Source Current from FBPFC		18	20	22	μA
PWM OUTPUT DRIVER						
$V_{GATE-CLAMP}$	Gate Output Clamping Voltage	V_{DD} = 22 V	18	19	20	V
V_{GATE-L}	Gate Low Voltage	V_{DD} = 15 V, I_O = 100 mA	–	–	1.5	V
V_{GATE-H}	Gate High Voltage	V_{DD} = 13 V, I_O = 100 mA	8	–	–	V
t_R	Gate Rising Time	V_{DD} = 15 V, C_L = 4.7 nF	30	60	120	ns
t_F	Gate Falling Time	V_{DD} = 15 V, C_L = 4.7 nF	30	50	110	ns
$D_{PWM-MAX}$	Maximum Duty Cycle		49.0	49.5	50.0	%
V_{PWM-LS}	PWM Comparator Level Shift		1.3	1.5	1.8	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
3. This parameter, although guaranteed by design, is not 100% production tested.
4. This GAIN is the maximum gain of modulation with a given V_{RMS} voltage when V_{VEA} is saturated to HIGH.
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

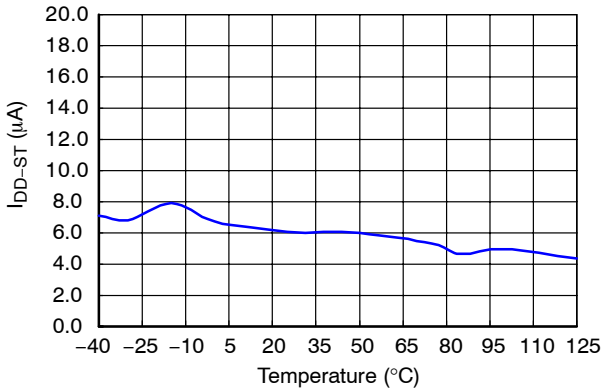


Figure 6. I_{DD-ST} vs. Temperature

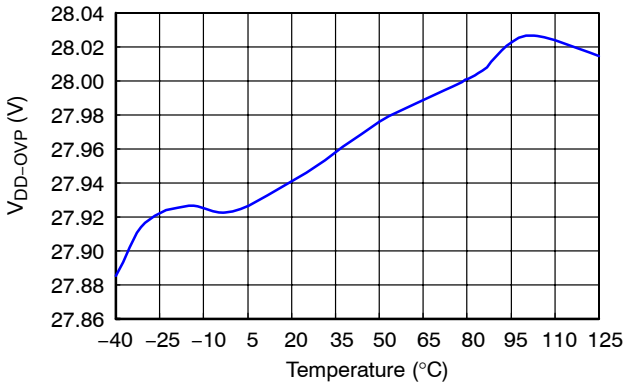


Figure 7. V_{DD-OVP} vs. Temperature

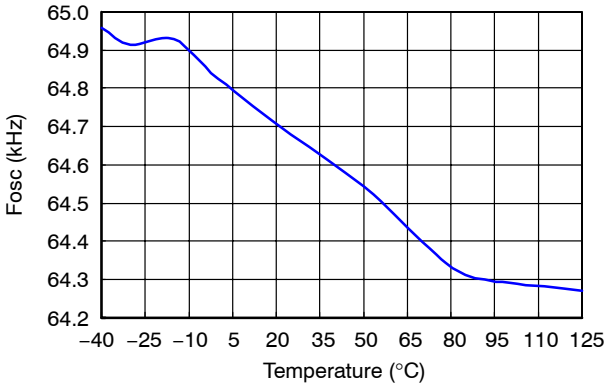


Figure 8. f_{osc} vs. Temperature

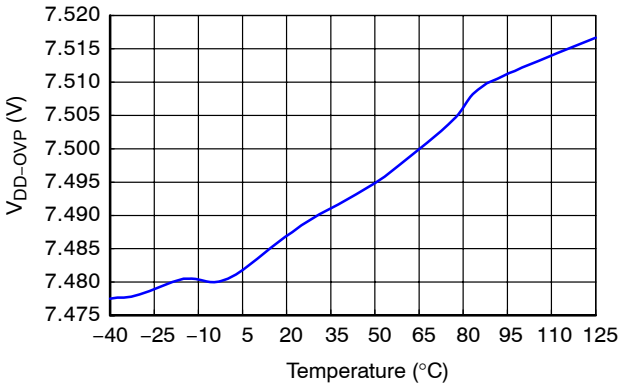


Figure 9. V_{VREF} vs. Temperature

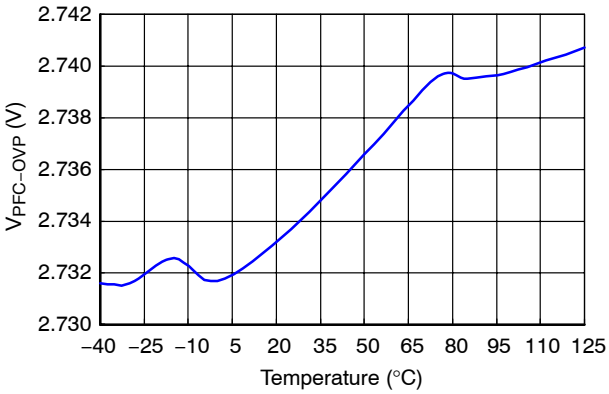


Figure 10. $V_{PFC-OVP}$ vs. Temperature

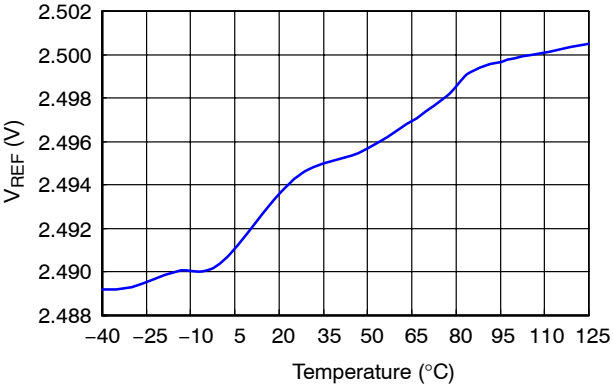


Figure 11. V_{REF} vs. Temperature

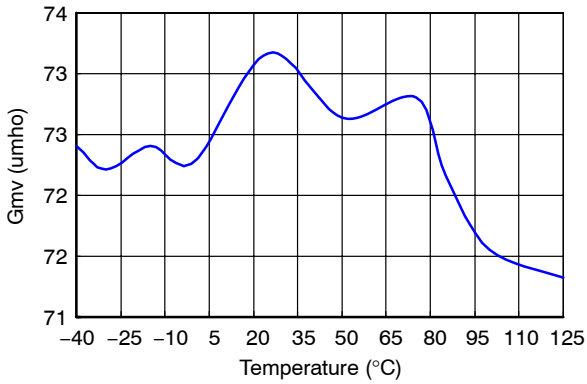


Figure 12. Gm_V vs. Temperature

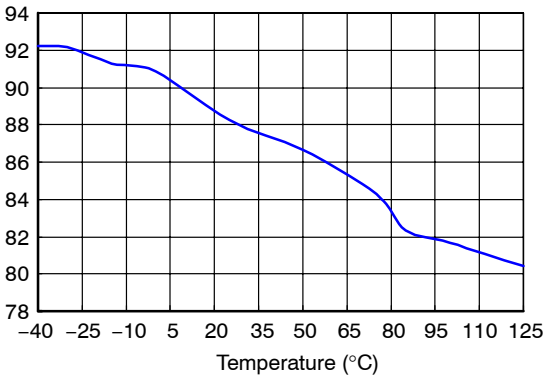


Figure 13. Gm_I vs. Temperature

TYPICAL CHARACTERISTICS (continued)

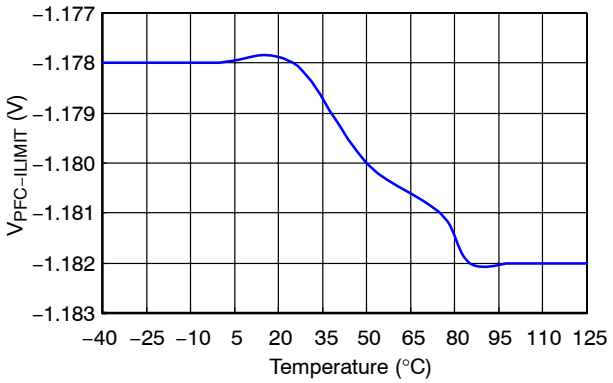


Figure 14. $V_{PFC-ILIMIT}$ vs. Temperature

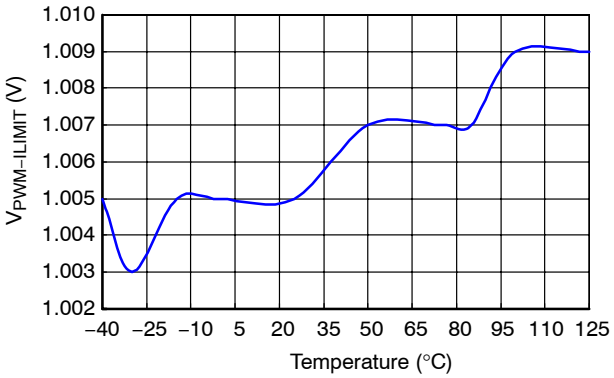


Figure 15. $V_{PWM-ILIMIT}$ vs. Temperature

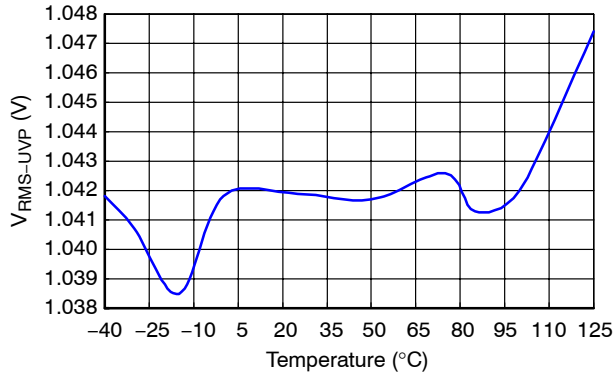


Figure 16. $V_{RMS-UVP}$ vs. Temperature

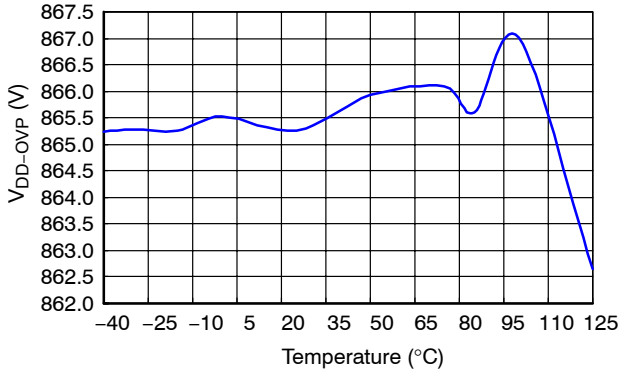


Figure 17. $\Delta V_{RMS-UVP}$ vs. Temperature

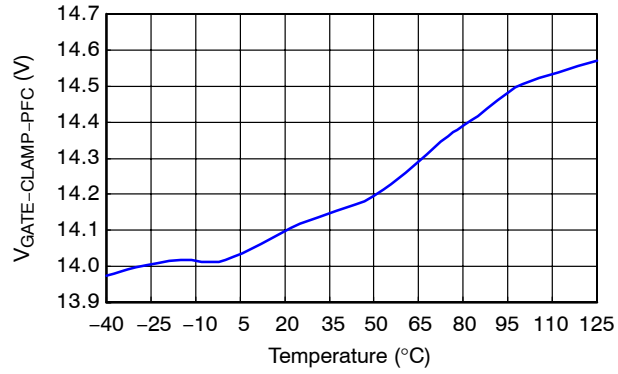


Figure 18. $V_{GATE-CLAMP-PFC}$ vs. Temperature

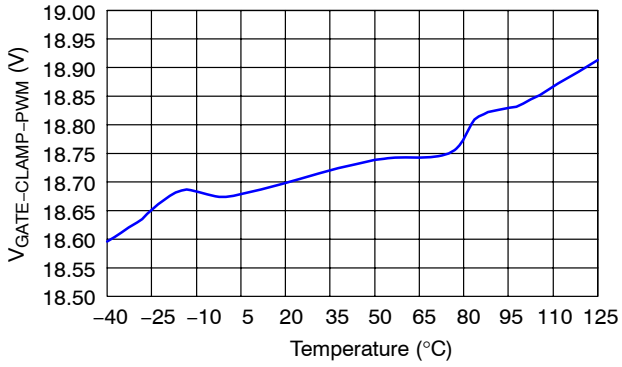


Figure 19. $V_{GATE-CLAMP-PWM}$ vs. Temperature

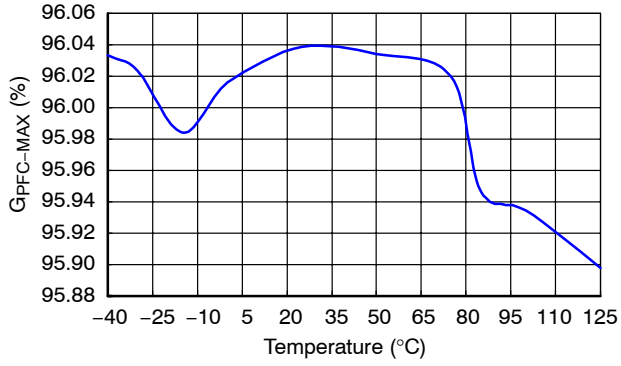


Figure 20. $D_{PFC-MAX}$ vs. Temperature

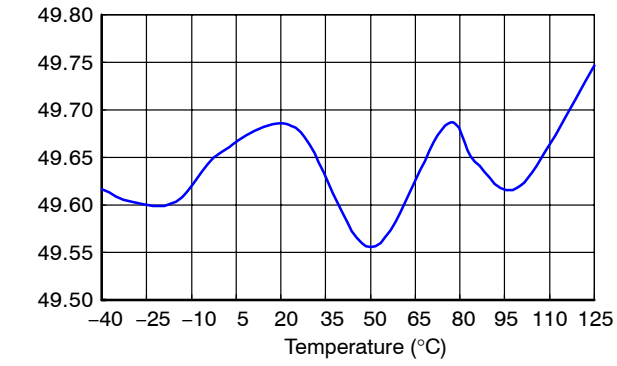


Figure 21. $D_{PWM-MAX}$ vs. Temperature

TYPICAL CHARACTERISTICS (continued)

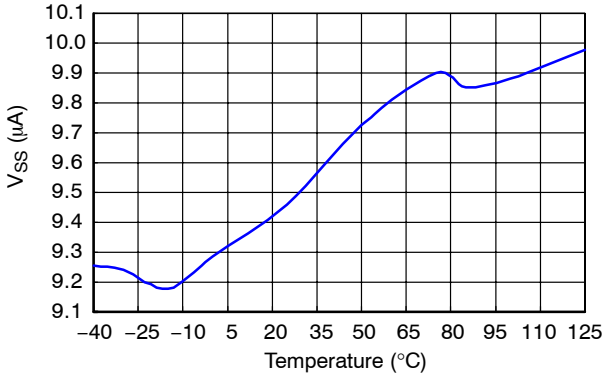


Figure 22. I_{SS} vs. Temperature

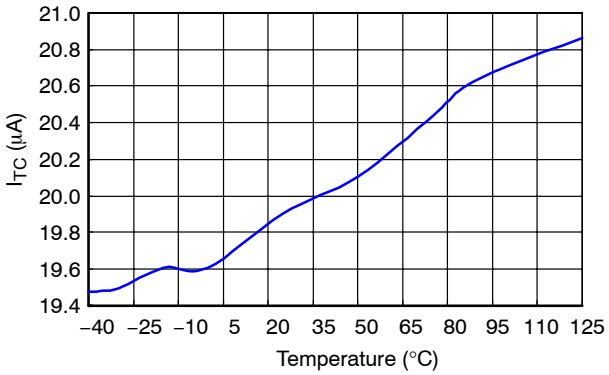


Figure 23. I_{TC} vs. Temperature

Functional Description

The FAN4800AS/CS/01S/02S consist of an average current controlled, continuous−boost, Power Factor Correction (PFC) front−end and a synchronized Pulse Width Modulator (PWM) back−end. The PWM can be used in current or voltage mode. In voltage mode, feedforward from the PFC output bus can help improve the line regulation of PWM. In either mode, the PWM stage uses conventional trailing−edge, duty−cycle modulation. This proprietary leading / trailing edge modulation results in a higher usable PFC error amplifier bandwidth and can significantly reduce the size of the PFC DC bus capacitor.

The synchronization of the PWM with the PFC simplifies the PWM compensation due to the controlled ripple on the PFC output capacitor (the PWM input capacitor).

In addition to power factor correction, a number of protection features are built into this series. They include soft−start, PFC over−voltage protection, peak current limiting, brownout protection, duty cycle limiting, and under−voltage lockout (UVLO).

Gain Modulator

The gain modulator is the heart of the PFC, as the circuit block controls the response of the current loop to line voltage waveform and frequency, RMS line voltage, and PFC output voltages. There are three inputs to the gain modulator:

1. A current representing the instantaneous input voltage (amplitude and wave shape) to the PFC. The rectified AC input sine wave is converted to a proportional current via a resistor and is fed into the gain modulator at IAC. Sampling current in this way minimizes ground noise, required in high−power, switching−power conversion environments. The gain modulator responds linearly to this current.
2. A voltage proportional to the long−term RMS AC line voltage, derived from the rectified line voltage after scaling and filtering. This signal is presented to the gain modulator at VRMS. The output of the gain modulator is inversely proportional to VRMS (except at unusually low values of VRMS, where special gain contouring takes over to limit power dissipation of the circuit components under brownout conditions).
3. The output of the voltage error amplifier, V_{EA}. The gain modulator responds linearly to variations in V_{VEA}.

The output of the gain modulator is a current signal, in the form of a full wave rectified sinusoid at twice the line frequency. This current is applied to the virtual ground (negative) input of the current error amplifier. In this way, the gain modulator forms the reference for the current error loop and ultimately controls the instantaneous current draw of the PFC from the power line. The general form of the output of the gain modulator is:

$$I_{GAINMOD} = \frac{I_{AC} \times (V_{EA} - 0.7)}{VRMS^2} \qquad \text{(eq. 1)}$$

Note that the output current of the gain modulator is limited around 159 μA and the maximum output voltage of the gain modulator is limited to 159 μA x 5.7 k = 0.906 V. This 0.906 V also determines the maximum input power. However, $I_{GAINMOD}$ cannot be measured directly from ISENSE. $I_{SENSE} = I_{GAINMOD} - I_{OFFSET}$ and I_{OFFSET} can only be measured when V_{VEA} is less than 0.5 V and $I_{GAINMOD}$ is 0 A. Typical I_{OFFSET} is around 31 μA ~ 48 μA.

Selecting R_{AC} for the IAC Pin

The IAC pin is the input of the gain modulator and also a current mirror input that requires current input. Selecting a proper resistor, R_{AC}, provides a good sine wave current derived from the line voltage and helps program the maximum input power and minimum input line voltage. $R_{AC} = V_{IN}$ peak x 56 kΩ. For example, if the minimum line voltage is 75 V_{AC}, the R_{AC}=75 x 1.414 x 56 kΩ = 6 MΩ.

Current Amplifier Error, IEA

The current error amplifier's output controls the PFC duty cycle to keep the average current through the boost inductor a linear function of the line voltage. At the inverting input to the current error amplifier, the output current of the gain modulator is summed with a current, which results in a negative voltage being impressed upon the ISENSE pin.

The negative voltage on ISENSE represents the sum of all currents flowing in the PFC circuit and is typically derived from a current−sense resistor in series with the negative terminal of the input bridge rectifier.

The inverting input of the current error amplifier is a virtual ground. Given this fact, and the arrangement of the duty cycle modulator polarities internal to the PFC, an increase in positive current from the gain modulator causes the output stage to increase its duty cycle until the voltage on ISENSE is adequately negative to cancel this increased current. Similarly, if the gain modulator's output decreases, the output duty cycle decreases to achieve a less negative voltage on the ISENSE pin.

PFC Cycle−By−Cycle Current Limiter

In addition to being a part of the current feedback loop, the ISENSE pin is a direct input to the cycle−by−cycle current limiter for the PFC section. If the input voltage at this pin is less than −1.15 V, the output of the PFC is disabled until the protection flip−flop is reset by the clock pulse at the start of the next PFC power cycle.

TriFault Detect™

To improve power supply reliability, reduce system component count, and simplify compliance to UL1950 safety standards; the FAN4800AS/CS/01S/02S includes TriFault Detect technology. This feature monitors FBPFC for certain PFC fault conditions.

In a feedback path failure, the output of the PFC could exceed safe operating limits. With such a failure, FBPFC exceeds its normal operating area. Should FBPFC go too

low, too high, or open; TriFault Detect senses the error and terminates the PFC output drive.

TriFault Detect is an entirely internal circuit. It requires no external components to serve its protective function.

PFC Over−Voltage Protection

In the FAN4800AS/CS/01S/02S, the PFC OVP comparator serves to protect the power circuit from being subjected to excessive voltages if the load changes suddenly. A resistor divider from the high−voltage DC output of the PFC is fed to FBPFC. When the voltage on FBPFC exceeds 2.75 V, the PFC output driver is shut down. The PWM section continues to operate. The OVP comparator has 250 mV of hysteresis and the PFC does not restart until the voltage at FBPFC drops below 2.5 V. V_{DD} OVP can also serve as a redundant PFC OVP protection. V_{DD} OVP threshold is 28 V with 1 V hysteresis.

Selecting PFC R_{sense}

R_{sense} is the sensing resistor of the PFC boost converter. During the steady state, line input current x R_{sense} equals $I_{GAINMOD}$ x 5.7 kΩ.

At full load, the average V_{VEA} needs to around 4.5 V and ripple on the VEA pin needs to be less than 400 mV. Choose the resistance of the sensing resistor:

$$R_{SENSE} = \frac{(4.5 - 0.7) \times 5.7\ k\Omega \times IAC \times Gain \times V_{IN} \times \sqrt{2}}{2 \times (5.6 - 0.7) \times Line\_Input\_Power} \quad \text{(eq. 2)}$$

where 5.6 is V_{VEA} maximum output voltage.

PFC Soft−Start

PFC startup is controlled by V_{VEA} level. Before the FBPFC voltage reaches 2.4 V, the V_{VEA} level is around 2.8 V. At 90 V_{AC}, the PFC soft−start time is 90 ms.

PFC Brownout

The AC UVP comparator monitors the AC input voltage. The PFC is disabled as AC input lowers, causing VRMS to be less than 1.05 V.

Error Amplifier Compensation

The PWM loading of the PFC can be modeled as a negative resistor because an increase in the input voltage to the PWM causes a decrease in the input current. This response dictates the proper compensation of the two transconductance error amplifiers. Figure 24 shows the types of compensation networks most commonly used for the voltage and current error amplifiers, along with their respective return points. The current−loop compensation is returned to VREF to produce a soft−start characteristic on the PFC. As the reference voltage increases from 0 V, it creates a differentiated voltage on IEA, which prevents the PFC from immediately demanding a full duty cycle on its boost converter. Complete design is discussed in application note AN−6078SC.

There is an RC filter between R_{sense} and ISENSE pin. There are two reasons to add a filter at the ISENSE pin:

1. Protection: During startup or inrush current conditions, there is a large voltage across R_{sense}, the sensing resistor of the PFC boost converter. It requires the I_{SENSE} filter to attenuate the energy.
2. To reduce inductance, L, the boost inductor. The I_{SENSE} filter also can reduce the boost inductor value since the I_{SENSE} filter behaves like an integrator before the ISENSE pin, which is the input of the current error amplifier, IEA.

The I_{SENSE} filter is an RC filter. The resistor value of the I_{SENSE} filter is between 100 Ω and 50 Ω because I_{OFFSET} x R_{FILTER} can generate a negative offset voltage of IEA. Selecting an R_{FILTER} equal to 50 Ω keeps the offset of the IEA less than 3 mV. Design the pole of the I_{SENSE} filter at $f_{PFC}/6$, one sixth of the PFC switching frequency, so the boost inductor can be reduced six times without disturbing the stability. The capacitor of the I_{SENSE} filter, C_{FILTER}, is approximately 100 nF.

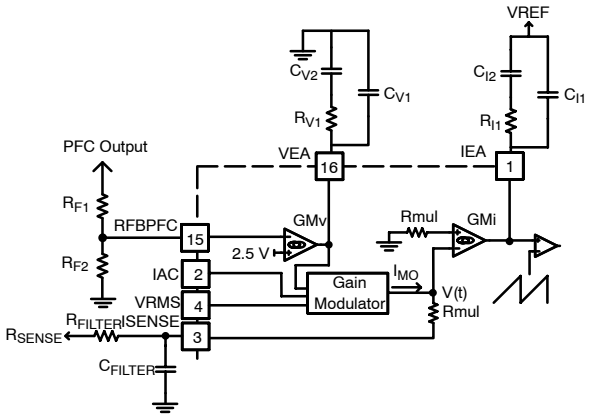


Figure 24. Compensation Network Connection for the Voltage and Current Error Amplifier

Two−Level PFC Function

To improve the efficiency, the system can reduce PFC switching loss at low line and light load by reducing the PFC output voltage. The two−level PFC output of the FAN4801S/02S can be programmable.

As Figure 25 shows, FAN4801S/02S detect the voltage of VEA and VRMS pins to determine if the system operates low line and light load. At the second−level PFC, there is a current of 20 μA through R_{F2} from the FBPFC pin. The second−level PFC output voltage can be calculated as.

$$Output = \frac{R_{F1} + R_{F2}}{R_{F2}} \times \left(2.5\ V - 20\ \mu A \times R_{F2}\right) \quad \text{(eq. 3)}$$

For example, if the second−level PFC output voltage is expected as 300 V and normal voltage is 387 V, according to the equation, R_{F2} is 28 kΩ R_{F1} is 4.3 MΩ.

The programmable range of second level PFC output voltage is 340 V ~ 300 V.

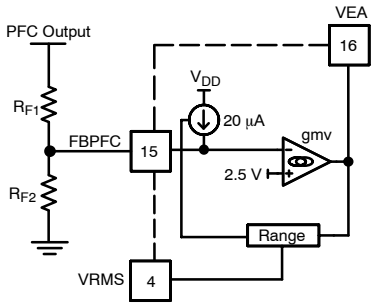


Figure 25. Two−Level PFC Scheme

Oscillator (RT/CT)

The oscillator frequency is determined by the values of R_T and C_T, which determine the ramp and off−time of the oscillator output clock:

$$f_{RTICT} = \frac{1}{t_{RTICT} + t_{DEAD}} \quad \text{(eq. 4)}$$

The dead time of the oscillator is derived from the following equation:

$$t_{RTICT} = C_T \times R_T \times \ln\left(\frac{VREF - 1}{VREF - 3.8}\right) \quad \text{(eq. 5)}$$

at V_{REF} = 7.5 V and $t_{RT/CT} = C_T$ x R_T x 0.56.

The dead time of the oscillator is determined using:

$$t_{DEAD} = \frac{2.8\ V}{7.78\ mA} \times C_T = 360 \times C_T \quad \text{(eq. 6)}$$

The dead time is so small ($t_{RT/CT} >> t_{DEAD}$) that the operating frequency can typically be approximated by:

$$f_{RTICT} = \frac{1}{t_{RTICT}} \quad \text{(eq. 7)}$$

Pulse Width Modulator (PWM)

The operation of the PWM section is straightforward, but there are several points that should be noted. Foremost among these is the inherent synchronization of PWM with the PFC section of the device, from which it also derives its basic timing. The PWM is capable of current−mode or voltage−mode operation. In current−mode applications, the PWM ramp (RAMP) is usually derived directly from a current−sensing resistor or current transformer in the primary side of the output stage. It is thereby representative of the current flowing in the converter's output stage. I_{LIMIT}, which provides cycle−by−cycle current limiting, is typically connected to RAMP in such applications. For voltage−mode operation and certain specialized applications, RAMP can be connected to a separate RC timing network to generate a voltage ramp against which FBPWM is compared. Under these conditions, the use of voltage feedforward from the PFC bus can assist in line regulation accuracy and response. As in current−mode operation, the I_{LIMIT} input is used for output stage over−current protection. No voltage error amplifier is included in the PWM stage, as this function is generally performed on the output side of the PWM's isolation boundary. To facilitate the design of opto−coupler feedback circuitry, an offset has been built into the PWM's RAMP input that allows FBPWM to command a 0% duty cycle for input voltages below typical 1.5 V.

PWM Cycle−by−Cycle Current Limiter

The ILIMIT pin is a direct input to the cycle−by−cycle current limiter for the PWM section. Should the input voltage at this pin exceed 1 V, the output flip−flop is reset by the clock pulse at the start of the next PWM power cycle. When the I_{LIMIT} triggers the cycle−by−cycle bi−cycle current, it limits the PWM duty cycle mode and the power dissipation is reduced during the dead−short condition.

V_{IN} OK Comparator

The V_{IN} OK comparator monitors the DC output of the PFC and inhibits the PWM if the voltage on FBPFC is less than its nominal 2.4 V. Once the voltage reaches 2.4 V, which corresponds to the PFC output capacitor being charged to its rated boost voltage, soft−start begins.

PWM Soft−Start (SS)

PWM startup is controlled by selection of the external capacitor at soft−start. A current source of 10 μA supplies the charging current for the capacitor and startup of the PWM begins at 1.5 V.

PWM Control (RAMP)

When the PWM section is used in current mode, RAMP is generally used as the sampling point for a voltage, representing the current in the primary of the PWM's output transformer. The voltage is derived either from a current−sensing resistor or a current transformer. In voltage mode, RAMP is the input for a ramp voltage generated by a second set of timing components (R_{RAMP}, C_{RAMP}) that have a minimum value of 0 V and a peak value of approximately 6 V. In voltage mode, feedforward from the PFC output bus is an excellent way to derive the timing ramp for the PWM stage.

Generating V_{DD}

After turning on the FAN4800AS/CS/01S/02S at 11 V, the operating voltage can vary from 9.3 V to 28 V. The threshold voltage of the V_{DD} OVP comparator is 28 V and its hysteresis is 1 V. When V_{DD} reaches 28 V, OPFC is LOW and the PWM section is not disturbed. There are two ways to generate V_{DD}: use auxiliary power supply around 15 V or use bootstrap winding to self−bias the FAN4800AS/CS/01S/02S system. The bootstrap winding can be taped from the PFC boost choke or the transformer of the DC−to−DC stage.

Leading/Trailing Edge Modulation

Conventional PWM techniques employ trailing−edge modulation, in which the switch turns on right after the trailing edge of the system clock. The error amplifier output

is then compared with the modulating ramp up. The effective duty cycle of the trailing−edge modulation is determined during the on−time of the switch.

In the case of leading−edge modulation, the switch is turned off exactly at the leading edge of the system clock. When the modulating ramp reaches the level of the error amplifier output voltage, the switch is turned on. The effective duty−cycle of the leading−edge modulation is determined during off−time of the switch.

Table 5. ORDERING INFORMATION

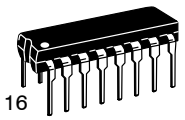
Part Number	Operating Temperature Range	Package	Packing Method
FAN4800ASNY	−40°C to 105°C	16−Pin Dual Inline Package (DIP)	Tube
FAN4800CSNY	−40°C to 105°C	16−Pin Dual Inline Package (DIP)	Tube
FAN4800CSMY	−40°C to 105°C	16−Pin Small Outline Package (SOP)	Tape & Reel
FAN4801SNY	−40°C to 105°C	16−Pin Dual Inline Package (DIP)	Tube
FAN4801SMY	−40°C to 105°C	16−Pin Small Outline Package (SOP)	Tape & Reel
FAN4802SNY	−40°C to 105°C	16−Pin Dual Inline Package (DIP)	Tube
FAN4802SMY	−40°C to 105°C	16−Pin Small Outline Package (SOP)	Tape & Reel

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

PDIP−16
CASE 648−08
ISSUE V

DATE 22 APR 2015



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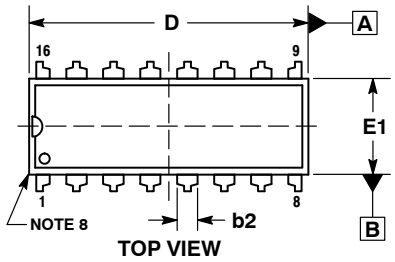
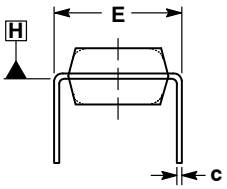
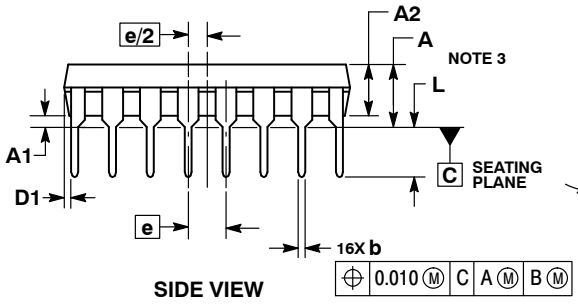


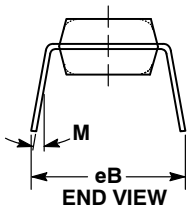
TOP VIEW



END VIEW
WITH LEADS CONSTRAINED
NOTE 5



SIDE VIEW



END VIEW
NOTE 6

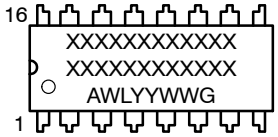
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS−3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	----	0.210	---	5.33
A1	0.015	----	0.38	---
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.735	0.775	18.67	19.69
D1	0.005	----	0.13	---
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	----	0.430	---	10.92
L	0.115	0.150	2.92	3.81
M	----	10°	---	10°

STYLE 1:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. CATHODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE
15. ANODE
16. ANODE

STYLE 2:
PIN 1. COMMON DRAIN
2. COMMON DRAIN
3. COMMON DRAIN
4. COMMON DRAIN
5. COMMON DRAIN
6. COMMON DRAIN
7. COMMON DRAIN
8. COMMON DRAIN
9. GATE
10. SOURCE
11. GATE
12. SOURCE
13. GATE
14. SOURCE
15. GATE
16. SOURCE

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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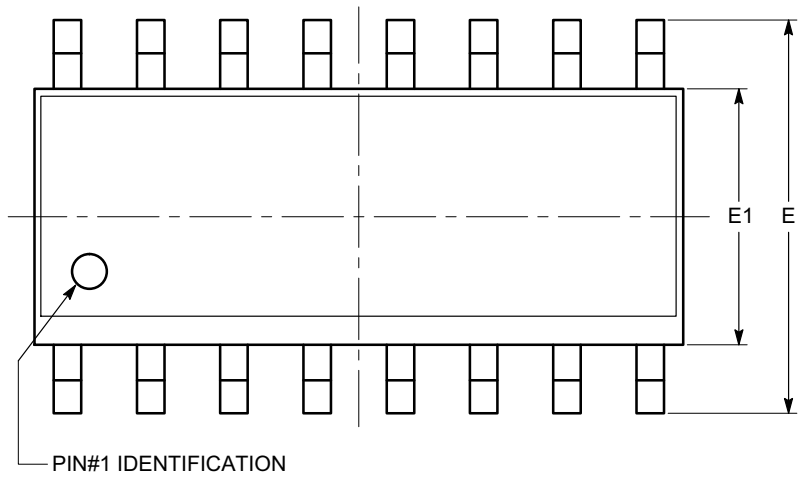
DESCRIPTION:	PDIP−16	PAGE 1 OF 1

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

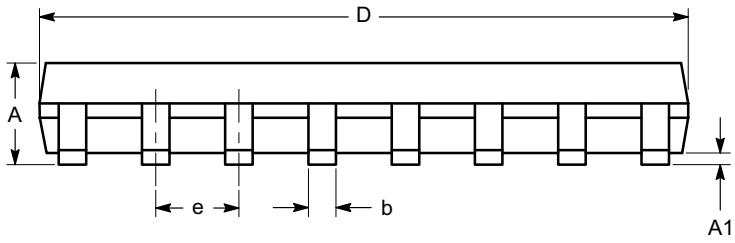
SOIC−16, 150 mils
CASE 751BG−01
ISSUE O

DATE 19 DEC 2008

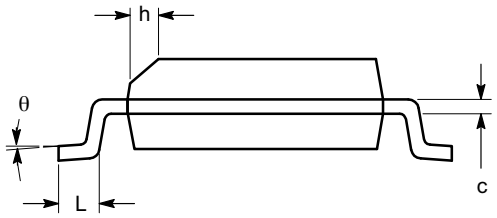


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27 BSC	
h	0.25		0.50
L	0.40		1.27
θ	0°		8°



SIDE VIEW



END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-012.

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