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# 500 mA, Very Low Dropout Bias Rail CMOS Voltage Regulator



ON Semiconductor™

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## NCP133

The NCP133 is a 500 mA VLDO equipped with NMOS pass transistor and a separate bias supply voltage ( $V_{BIAS}$ ). The device provides very stable, accurate output voltage with low noise suitable for space constrained, noise sensitive applications. In order to optimize performance for battery operated portable applications, the NCP133 features low  $I_Q$  consumption. The XDFN6 1.2 mm x 1.2 mm package is optimized for use in space constrained applications.

### Features

- Input Voltage Range: 0.8 V to 5.5 V
- Bias Voltage Range: 2.4 V to 5.5 V
- Adjustable and Fixed Voltage Versions Available
- Output Voltage Range: 0.8 V to 2.1 V (Fixed) and 0.8 V to 3.6 V (Adjustable)
- $\pm 1.5\%$  Accuracy over Temperature,  $0.5\% V_{OUT}$  @  $25^\circ\text{C}$
- Ultra-Low Dropout: Typ. 140 mV at 500 mA
- Very Low Bias Input Current of Typ.  $80 \mu\text{A}$
- Very Low Bias Input Current in Disable Mode: Typ.  $0.5 \mu\text{A}$
- Logic Level Enable Input for ON/OFF Control
- Output Active Discharge Option Available
- Stable with a  $2.2 \mu\text{F}$  Ceramic Capacitor
- Available in XDFN6 – 1.2 mm x 1.2 mm x 0.4 mm Package
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### Typical Applications

- Battery-powered Equipment
- Smartphones, Tablets
- Cameras, DVRs, STB and Camcorders



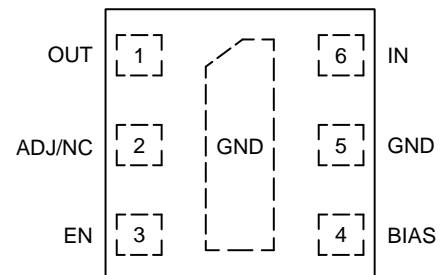
XDFN6  
CASE 711AT

### MARKING DIAGRAM



XX = Specific Device Code  
M = Date Code

### PIN CONNECTIONS



(Top View)

### ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

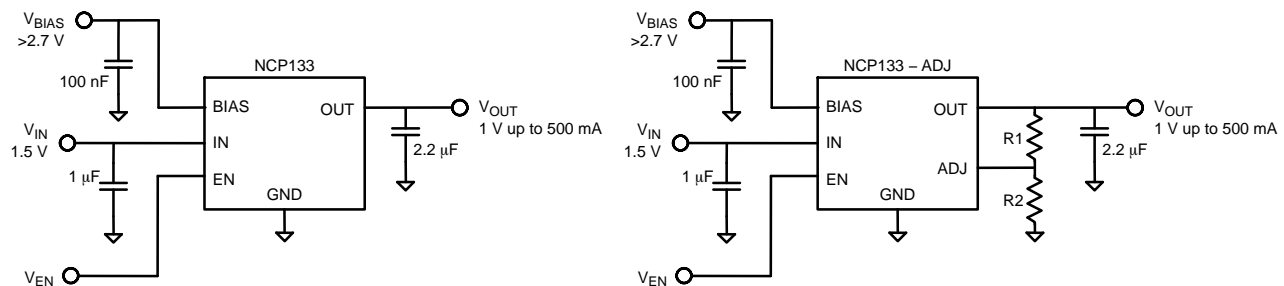


Figure 1. Typical Application Schematics



# NCP133

## PIN FUNCTION DESCRIPTION

Pin No. XDFN6	Pin Name	Description
1	OUT	Regulated Output Voltage pin
2 (Fixed)	N/C	Not internally connected (Note 1)
2 (Adj)	ADJ	Adjustable Regulator Feedback Input. Connect to output voltage resistor divider central node.
3	EN	Enable pin. Driving this pin high enables the regulator. Driving this pin low puts the regulator into shutdown mode.
4	BIAS	Bias voltage supply for internal control circuits. This pin is monitored by internal Under-Voltage Lockout Circuit.
5	GND	Ground
6	IN	Input Voltage Supply pin
Pad		Should be soldered to the ground plane for increased thermal performance.

1. True no connect. Printed circuit board traces are allowable

## ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage (Note 2)	$V_{IN}$	-0.3 to 6	V
Output Voltage	$V_{OUT}$	$-0.3 \text{ to } (V_{IN} + 0.3) \leq 6$	V
Chip Enable, Bias and Adj Input	$V_{EN}, V_{BIAS}, V_{ADJ}$	-0.3 to 6	V
Output Short Circuit Duration	$t_{SC}$	unlimited	s
Maximum Junction Temperature	$T_J$	150	°C
Storage Temperature	$T_{STG}$	-55 to 150	°C
ESD Capability, Human Body Model (Note 3)	$ESD_{HBM}$	2000	V
ESD Capability, Machine Model (Note 3)	$ESD_{MM}$	200	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.

3. This device series incorporates ESD protection (except OUT pin) and is tested by the following methods:

ESD Human Body Model tested per EIA/JESD22-A114

ESD Machine Model tested per EIA/JESD22-A115

Latchup Current Maximum Rating tested per JEDEC standard: JESD78.

## THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, XDFN6 1.2 mm x 1.2 mm Thermal Resistance, Junction-to-Air	$R_{\theta JA}$	170	°C/W

# NCP133

**ELECTRICAL CHARACTERISTICS**  $-40^{\circ}\text{C} \leq T_J \leq 85^{\circ}\text{C}$ ;  $V_{\text{BIAS}} = 2.7\text{ V}$  or  $(V_{\text{OUT}} + 1.6\text{ V})$ , whichever is greater,  $V_{\text{IN}} = V_{\text{OUT(NOM)}} + 0.3\text{ V}$ ,  $I_{\text{OUT}} = 1\text{ mA}$ ,  $V_{\text{EN}} = 1\text{ V}$ , unless otherwise noted.  $C_{\text{IN}} = 1\text{ }\mu\text{F}$ ,  $C_{\text{OUT}} = 2.2\text{ }\mu\text{F}$ . Typical values are at  $T_J = +25^{\circ}\text{C}$ . Min/Max values are for  $-40^{\circ}\text{C} \leq T_J \leq 85^{\circ}\text{C}$  unless otherwise noted. (Note 5)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Operating Input Voltage Range		$V_{\text{IN}}$	$V_{\text{OUT}} + V_{\text{DO}}$		5.5	V
Operating Bias Voltage Range		$V_{\text{BIAS}}$	$(V_{\text{OUT}} + 1.40) \geq 2.4$		5.5	V
Undervoltage Lock-out	$V_{\text{BIAS}}$ Rising Hysteresis	UVLO		1.6 0.2		V
Reference Voltage (Adj devices only)	$T_J = +25^{\circ}\text{C}$	$V_{\text{REF}}$		0.800		V
Output Voltage Accuracy	(Note 4)	$V_{\text{OUT}}$		$\pm 0.5$		%
Output Voltage Accuracy (Note 4)	$-40^{\circ}\text{C} \leq T_J \leq 85^{\circ}\text{C}$ , $V_{\text{OUT(NOM)}} + 0.3\text{ V} \leq V_{\text{IN}} \leq V_{\text{OUT(NOM)}} + 1.0\text{ V}$ , $2.7\text{ V}$ or $(V_{\text{OUT(NOM)}} + 1.6\text{ V})$ , whichever is greater $< V_{\text{BIAS}} < 5.5\text{ V}$ , $1\text{ mA} < I_{\text{OUT}} < 500\text{ mA}$	$V_{\text{OUT}}$	-1.5		+1.5	%
$V_{\text{IN}}$ Line Regulation	$V_{\text{OUT(NOM)}} + 0.3\text{ V} \leq V_{\text{IN}} \leq 5.0\text{ V}$	$\text{Line}_{\text{Reg}}$		0.01		%/V
$V_{\text{BIAS}}$ Line Regulation	$2.7\text{ V}$ or $(V_{\text{OUT(NOM)}} + 1.6\text{ V})$ , whichever is greater $< V_{\text{BIAS}} < 5.5\text{ V}$	$\text{Line}_{\text{Reg}}$		0.01		%/V
Load Regulation	$I_{\text{OUT}} = 1\text{ mA}$ to $500\text{ mA}$	$\text{Load}_{\text{Reg}}$		1.5		mV
$V_{\text{IN}}$ Dropout Voltage	$I_{\text{OUT}} = 150\text{ mA}$ (Note 6)	$V_{\text{DO}}$		37	75	mV
	$I_{\text{OUT}} = 500\text{ mA}$ (Note 6)	$V_{\text{DO}}$		140	250	
$V_{\text{BIAS}}$ Dropout Voltage	$I_{\text{OUT}} = 500\text{ mA}$ , $V_{\text{IN}} = V_{\text{BIAS}}$ (Notes 6, 7)	$V_{\text{DO}}$		1.1	1.5	V
Output Current Limit	$V_{\text{OUT}} = 90\% V_{\text{OUT(NOM)}}$	$I_{\text{CL}}$	550	800	1000	mA
ADJ Pin Operating Current (ADJ devices only)		$I_{\text{ADJ}}$		0.1	0.5	$\mu\text{A}$
Bias Pin Operating Current	$V_{\text{BIAS}} = 2.7\text{ V}$	$I_{\text{BIAS}}$		80	110	$\mu\text{A}$
Bias Pin Disable Current	$V_{\text{EN}} \leq 0.4\text{ V}$	$I_{\text{BIAS(DIS)}}$		0.5	1	$\mu\text{A}$
Vinpin Pin Disable Current	$V_{\text{EN}} \leq 0.4\text{ V}$	$I_{\text{VIN(DIS)}}$		0.5	1	$\mu\text{A}$
EN Pin Threshold Voltage	EN Input Voltage "H"	$V_{\text{EN(H)}}$	0.9			V
	EN Input Voltage "L"	$V_{\text{EN(L)}}$			0.4	
EN Pull Down Current	$V_{\text{EN}} = 5.5\text{ V}$	$I_{\text{EN}}$		0.3	1	$\mu\text{A}$
Turn-On Time	From assertion of $V_{\text{EN}}$ to $V_{\text{OUT}} = 98\% V_{\text{OUT(NOM)}}$ . $V_{\text{OUT(NOM)}} = 1.0\text{ V}$	$t_{\text{ON}}$		150		$\mu\text{s}$
Power Supply Rejection Ratio	$V_{\text{IN}}$ to $V_{\text{OUT}}$ , $f = 1\text{ kHz}$ , $I_{\text{OUT}} = 150\text{ mA}$ , $V_{\text{IN}} \geq V_{\text{OUT}} + 0.5\text{ V}$	$\text{PSRR}(V_{\text{IN}})$		70		dB
	$V_{\text{BIAS}}$ to $V_{\text{OUT}}$ , $f = 1\text{ kHz}$ , $I_{\text{OUT}} = 150\text{ mA}$ , $V_{\text{IN}} \geq V_{\text{OUT}} + 0.5\text{ V}$	$\text{PSRR}(V_{\text{BIAS}})$		80		
Output Noise Voltage (Fixed Volt.)	$V_{\text{IN}} = V_{\text{OUT}} + 0.5\text{ V}$ , $V_{\text{OUT(NOM)}} = 1\text{ V}$ , $f = 10\text{ Hz}$ to $100\text{ kHz}$	$V_{\text{N}}$		40		$\mu\text{V}_{\text{RMS}}$
Output Noise Voltage (Adj devices)	$V_{\text{IN}} = V_{\text{OUT}} + 0.5\text{ V}$ , $f = 10\text{ Hz}$ to $100\text{ kHz}$	$V_{\text{N}}$		$50 \times V_{\text{OUT}}$		$\mu\text{V}_{\text{RMS}}$
Thermal Shutdown Threshold	Temperature increasing			160		$^{\circ}\text{C}$
	Temperature decreasing			140		
Output Discharge Pull-Down	$V_{\text{EN}} \leq 0.4\text{ V}$ , $V_{\text{OUT}} = 0.5\text{ V}$ , NCP133A options only	$R_{\text{DISCH}}$		150		$\Omega$

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Adjustable devices tested at 0.8 V; external resistor tolerance is not taken into account.

5. Performance guaranteed over the indicated operating temperature range by design and/or characterization. Production tested at  $T_A = 25^{\circ}\text{C}$ . Low duty cycle pulse techniques are used during the testing to maintain the junction temperature as close to ambient as possible.

6. Dropout voltage is characterized when  $V_{\text{OUT}}$  falls 3% below  $V_{\text{OUT(NOM)}}$ .

7. For output voltages below 0.9 V,  $V_{\text{BIAS}}$  dropout voltage does not apply due to a minimum Bias operating voltage of 2.4 V.

TYPICAL CHARACTERISTICS

At  $T_J = +25^\circ\text{C}$ ,  $V_{IN} = V_{OUT(TYP)} + 0.3\text{ V}$ ,  $V_{BIAS} = 2.7\text{ V}$ ,  $V_{EN} = V_{BIAS}$ ,  $V_{OUT(NOM)} = 1.0\text{ V}$ ,  $I_{OUT} = 500\text{ mA}$ ,  $C_{IN} = 1\ \mu\text{F}$ ,  $C_{BIAS} = 0.1\ \mu\text{F}$ , and  $C_{OUT} = 2.2\ \mu\text{F}$  (effective capacitance), unless otherwise noted.

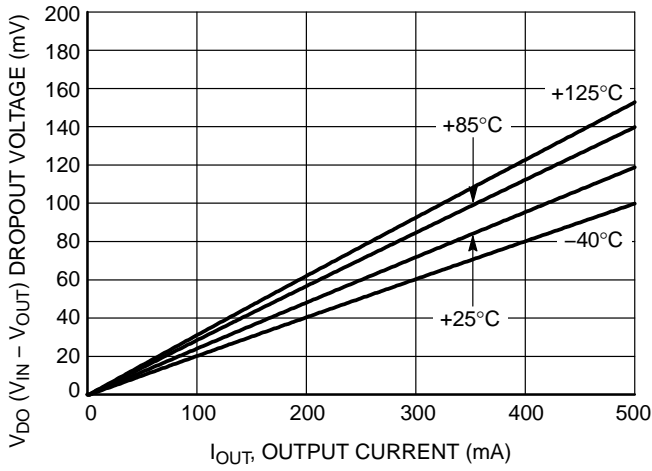


Figure 4.  $V_{IN}$  Dropout Voltage vs.  $I_{OUT}$  and Temperature  $T_J$

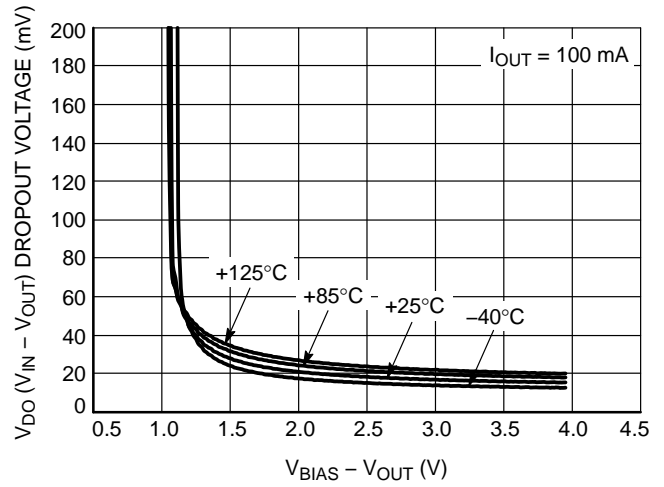


Figure 5.  $V_{IN}$  Dropout Voltage vs.  $(V_{BIAS} - V_{OUT})$  and Temperature  $T_J$

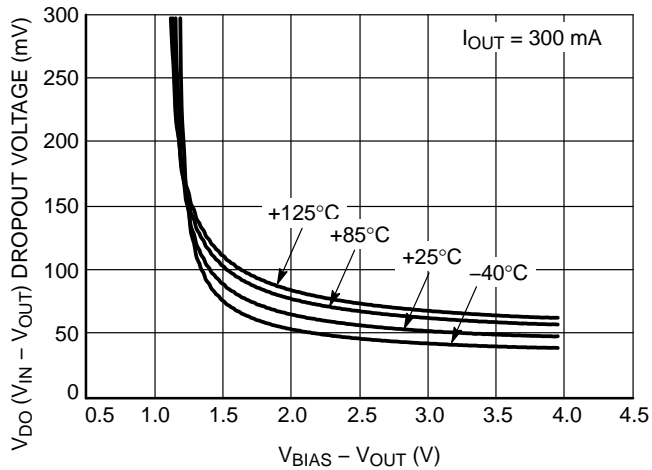


Figure 6.  $V_{IN}$  Dropout Voltage vs.  $(V_{BIAS} - V_{OUT})$  and Temperature  $T_J$

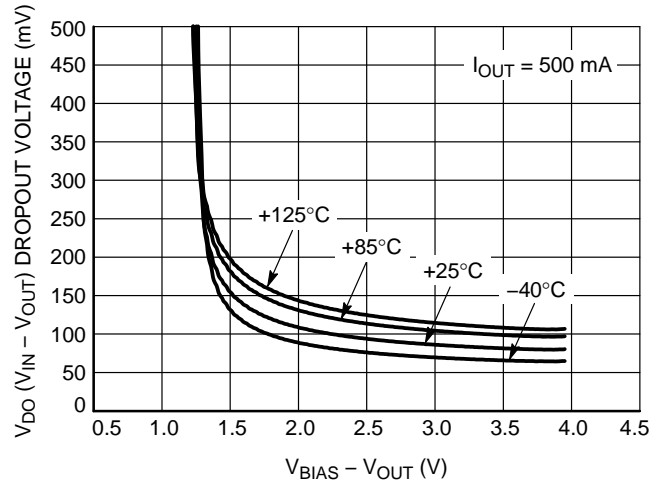


Figure 7.  $V_{IN}$  Dropout Voltage vs.  $(V_{BIAS} - V_{OUT})$  and Temperature  $T_J$

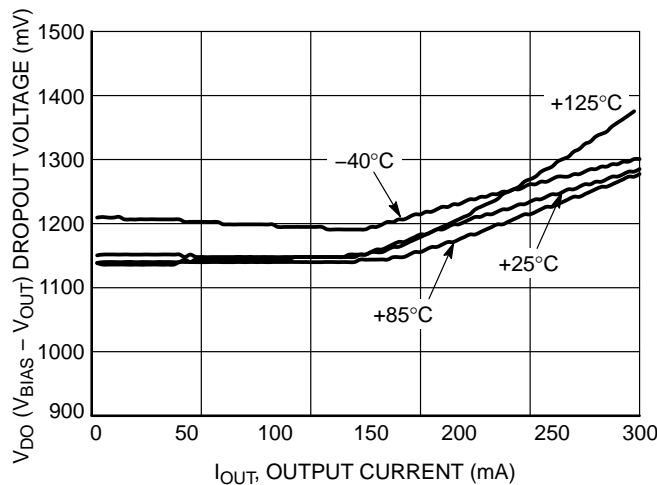


Figure 8.  $V_{BIAS}$  Dropout Voltage vs.  $I_{OUT}$  and Temperature  $T_J$

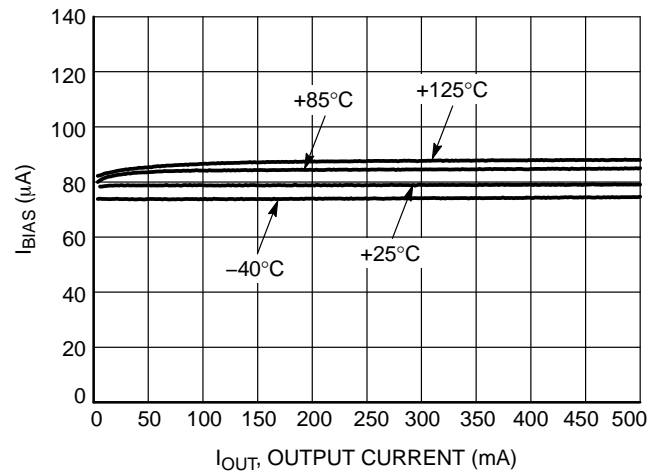
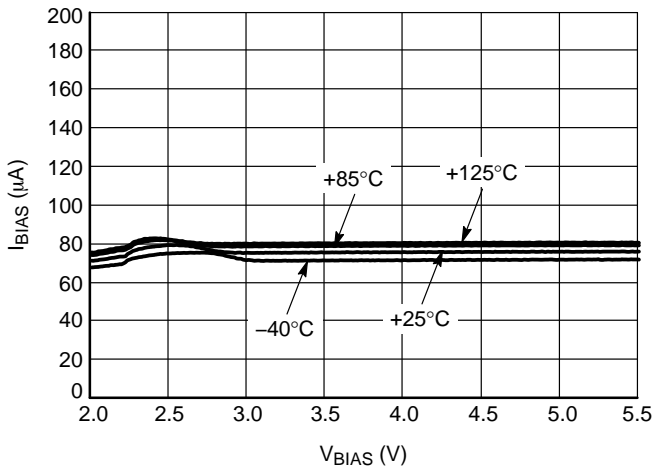


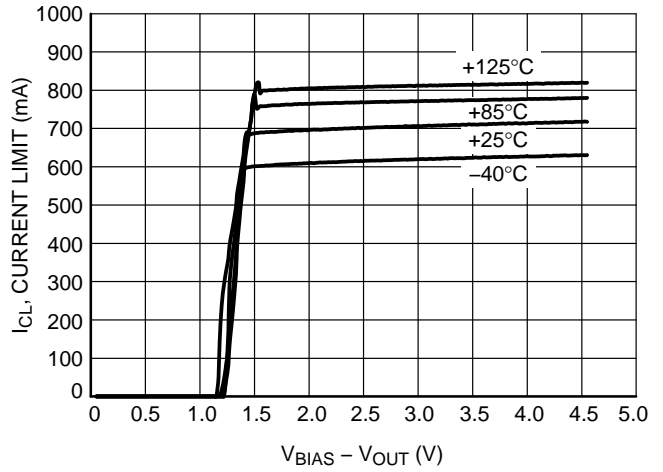
Figure 9. BIAS Pin Current vs.  $I_{OUT}$  and Temperature  $T_J$

**TYPICAL CHARACTERISTICS**

At  $T_J = +25^\circ\text{C}$ ,  $V_{IN} = V_{OUT(TYP)} + 0.3\text{ V}$ ,  $V_{BIAS} = 2.7\text{ V}$ ,  $V_{EN} = V_{BIAS}$ ,  $V_{OUT(NOM)} = 1.0\text{ V}$ ,  $I_{OUT} = 500\text{ mA}$ ,  
 $C_{IN} = 1\text{ }\mu\text{F}$ ,  $C_{BIAS} = 0.1\text{ }\mu\text{F}$ , and  $C_{OUT} = 2.2\text{ }\mu\text{F}$  (effective capacitance), unless otherwise noted.



**Figure 10. BIAS Pin Current vs.  $V_{BIAS}$  and Temperature  $T_J$**



**Figure 11. Current Limit vs.  $(V_{BIAS} - V_{OUT})$**

APPLICATIONS INFORMATION

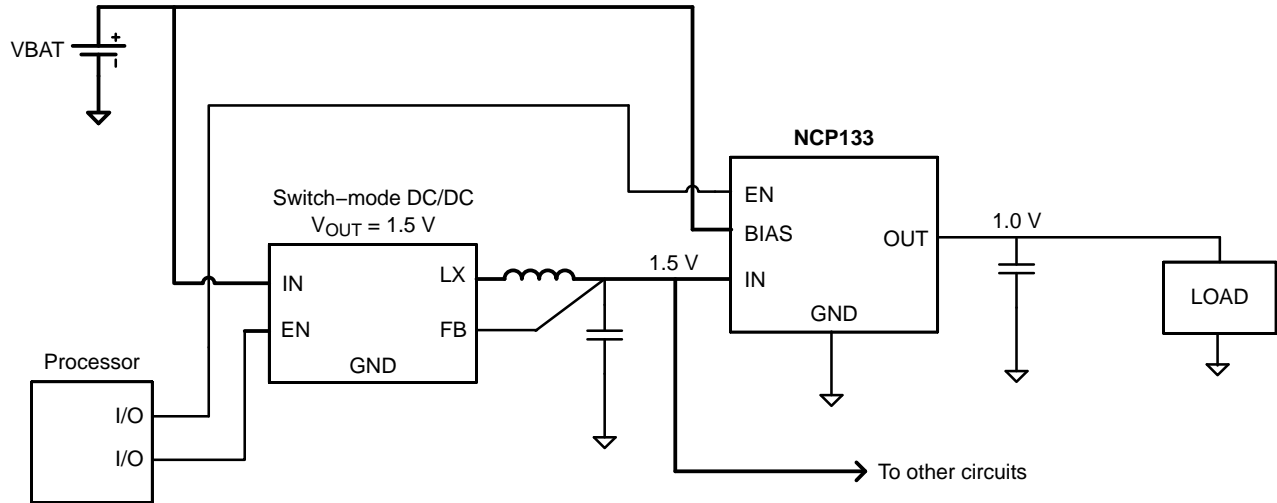


Figure 12. Typical Application: Low-Voltage DC/DC Post-Regulator with ON/OFF Functionality

The NCP133 dual-rail very low dropout voltage regulator is using NMOS pass transistor for output voltage regulation from  $V_{IN}$  voltage. All the low current internal control circuitry is powered from the  $V_{BIAS}$  voltage.

The use of an NMOS pass transistor offers several advantages in applications. Unlike PMOS topology devices, the output capacitor has reduced impact on loop stability.  $V_{in}$  to  $V_{out}$  operating voltage difference can be very low compared with standard PMOS regulators in very low  $V_{in}$  applications.

The NCP133 offers smooth monotonic start-up. The controlled voltage rising limits the inrush current.

The Enable (EN) input is equipped with internal hysteresis. NCP133 Voltage linear regulator Fixed and Adjustable version is available.

**Output Voltage Adjust**

The required output voltage of Adjustable devices can be adjusted from 0.8 V to 3.6 V using two external resistors.

Typical application schematics is shown in Figure 13.

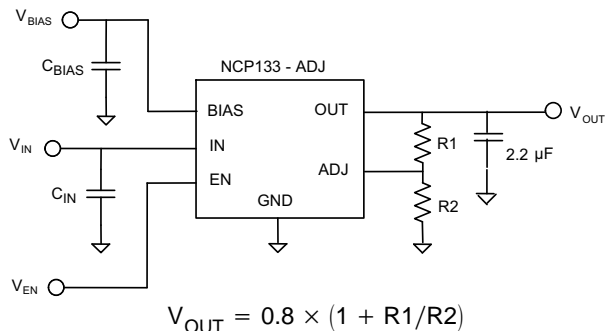


Figure 13. Typical Application Schematics

It is recommended to keep the total serial resistance of resistors ( $R1 + R2$ ) no greater than 100 kΩ.

Recommended resistor values for programming the frequently used voltages can be found in the Table 1.

**Dropout Voltage**

Because of two power supply inputs  $V_{IN}$  and  $V_{BIAS}$  and one  $V_{OUT}$  regulator output, there are two Dropout voltages specified.

The first, the  $V_{IN}$  Dropout voltage is the voltage difference ( $V_{IN} - V_{OUT}$ ) when  $V_{OUT}$  starts to decrease by percent specified in the Electrical Characteristics table.  $V_{BIAS}$  is high enough; specific value is published in the Electrical Characteristics table.

The second,  $V_{BIAS}$  dropout voltage is the voltage difference ( $V_{BIAS} - V_{OUT}$ ) when  $V_{IN}$  and  $V_{BIAS}$  pins are joined together and  $V_{OUT}$  starts to decrease.

**Input and Output Capacitors**

The device is designed to be stable for ceramic output capacitors with Effective capacitance in the range from 2.2 μF to 10 μF. The device is also stable with multiple capacitors in parallel, having the total effective capacitance in the specified range.

In applications where no low input supplies impedance available (PCB inductance in  $V_{IN}$  and/or  $V_{BIAS}$  inputs as example), the recommended  $C_{IN} = 1 \mu F$  and  $C_{BIAS} = 0.1 \mu F$  or greater. Ceramic capacitors are recommended. For the best performance all the capacitors should be connected to the NCP133 respective pins directly in the device PCB copper layer, not through vias having not negligible impedance.

When using small ceramic capacitor, their capacitance is not constant but varies with applied DC biasing voltage, temperature and tolerance. The effective capacitance can be much lower than their nominal capacitance value, most importantly in negative temperatures and higher LDO output voltages. That is why the recommended Output capacitor capacitance value is specified as Effective value in the specific application conditions.



# NCP133

## Enable Operation

The enable pin will turn the regulator on or off. The threshold limits are covered in the electrical characteristics table in this data sheet. If the enable function is not to be used then the pin should be connected to  $V_{IN}$  or  $V_{BIAS}$ .

## Current Limitation

The internal Current Limitation circuitry allows the device to supply the full nominal current and surges but protects the device against Current Overload or Short.

## Thermal Protection

Internal thermal shutdown (TSD) circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When TSD activated, the regulator output turns off. When cooling down under the low temperature threshold, device output is activated again. This TSD feature is provided to prevent failures from accidental overheating.

Activation of the thermal protection circuit indicates excessive power dissipation or inadequate heatsinking. For reliable operation, junction temperature should be limited to +125°C maximum.

**Table 1. RESISTOR VALUES FOR PROGRAMMING THE OUTPUT VOLTAGE**

$V_{OUT}$ (V)	$R_1$ (k $\Omega$ )	$R_2$ (k $\Omega$ )
0.8	Short	Open
0.9	10.0	80.6
1.0	19.6	78.7
1.05	24.3	78.7
1.1	24.9	66.5
1.2	33.2	66.5
1.5	43.2	49.9
1.8	41.2	33.2
2.5	42.2	20.0
3.3	61.9	20.0

NOTE:  $V_{OUT} = 0.8 \times (1 + R_1/R_2)$   
Resistors in the table are standard 1% types

## ORDERING INFORMATION

Device	Nominal Output Voltage	Marking	Marking Rotation	Option	Package	Shipping†
NCP133AMX090TAG	0.90 V	D	90°	Output Active Discharge Output Active Discharge	XDFN6 (Pb-Free) XDFN6 (Pb-Free)	3000 / Tape & Reel
NCP133AMX090TCG	0.90 V	D	90°			
NCP133AMX100TCG	1.00 V	3	0°			
NCP133AMX105TCG	1.05 V	4	0°			
NCP133AMX110TCG	1.10 V	5	0°			
NCP133AMX115TCG	1.15 V	T	90°			
NCP133AMX120TCG	1.20 V	6	0°			
NCP133AMX125TCG	1.25 V	E	90°			
NCP133AMX130TCG	1.30 V	F	90°			
NCP133AMX150TCG	1.50 V	J	90°			
NCP133AMX180TCG	1.80 V	Q	90°			
NCP133AMXADJTCG	ADJ	K	90°			
NCP133BMXADJTCG	ADJ	P	90°	Non-Active Discharge		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

To order other package and voltage variants, please contact your ON Semiconductor sales representative

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

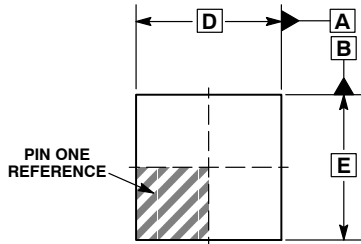
ON Semiconductor®



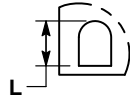
SCALE 4:1

XDFN6 1.20x1.20, 0.40P  
CASE 711AT  
ISSUE C

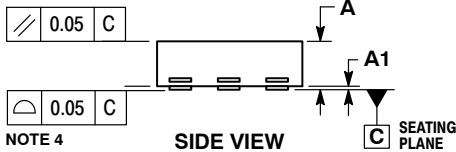
DATE 04 DEC 2015



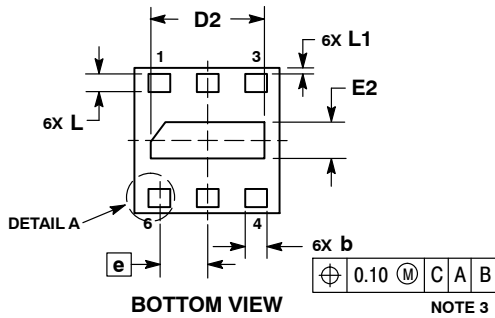
TOP VIEW



DETAIL A  
OPTIONAL  
CONSTRUCTION



SIDE VIEW



BOTTOM VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO THE PLATED TERMINALS.
4. COPLANARITY APPLIES TO THE PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS		
	MIN	TYP	MAX
A	0.30	0.37	0.45
A1	0.00	0.03	0.05
b	0.13	0.18	0.23
D	1.15	1.20	1.25
D2	0.84	0.94	1.04
E	1.15	1.20	1.25
E2	0.20	0.30	0.40
e	0.40 BSC		
L	0.15	0.20	0.25
L1	0.00	0.05	0.10

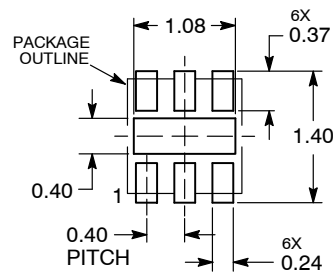
GENERIC MARKING DIAGRAM\*



XX = Specific Device Code  
M = Date Code

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

RECOMMENDED MOUNTING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	XDFN6, 1.20 X 1.20, 0.40P	PAGE 1 OF 1

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