TS4956

Stereo audio amplifier system with I²C bus interface

Features

- Operating from V_{CC} = 2.7 V to 5.5 V
- I²C bus control interface
- 38 mW output power at V_{CC} = 3.3 V, THD = 1%, F = 1 kHz, with 16 Ω load
- Ultra low consumption in standby mode: 0.5 µA
- Digital volume control range from +12 dB to -34 dB
- 32-step digital volume control
- Stereo loudspeaker option by I²C
- 8 different output mode selections
- Pop and click reduction circuitry
- Flip-chip package, 18 bumps with 300 µm diameter
- Lead-free flip chip package
- Output power limitation on headphone for eardrum damage consideration

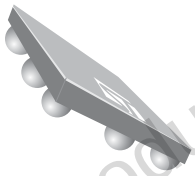
Applications

- Mobile phones (cellular/cordless)
- PDAs
- Laptop / notebook computers
- Portable audio devices

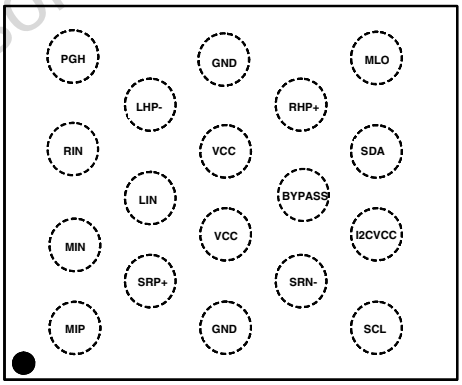
Description

The TS4956 is a complete audio system device with three dedicated outputs, one stereo headphone, one loudspeaker drive and one mono line for a hands-free set. The stereo headphone is capable of delivering more than 25 mW per channel of continuous average power into 16 Ω single-ended loads with 0.3% THD+N from a 5 V power supply. The device functions are controlled via an I²C bus, which minimizes the number of external components needed.

TS4956 - flip-chip 18



Pin connections (top view)



The overall gain and the different output modes of the TS4956 are controlled digitally by the control registers which are programmed via the I²C interface. It has also an internal thermal shutdown protection mechanism.

Contents

1 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage (1)	6	V
V_i	Input voltage (2)	G_{ND} to V_{CC}	V
T_{oper}	Operating free air temperature range	-40 to + 85	°C
T_{stg}	Storage temperature	-65 to +150	°C
T_j	Maximum junction temperature	150	°C
R_{thja}	Thermal resistance junction to ambient (3)	200	°C/W
P_{diss}	Power dissipation	Internally limited(4)	
ESD	Susceptibility - human body model(5)	2	kV
	Susceptibility - machine model	150	V
Latch-up	Latch-up immunity	200	mA
	Lead temperature (soldering, 10sec)	260	°C

1. All voltage values are measured with respect to the ground pin.
2. The magnitude of input signal must never exceed V_{CC} + 0.3 V / GND - 0.3 V
3. Device is protected in case of over temperature by a thermal shutdown activated at 150°C.
4. Exceeding the power derating curves during a long period may involve abnormal operating conditions.
5. Human body model, 100 pF discharged through a 1.5 kΩ resistor, into pin to V_{CC} device

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}(1)	Supply voltage	2.7 to 5.5 V	V
R_L	Load resistor Speaker/BTL output (modes 1,2,7) Headphone, MLO output (modes 3,4,5,6,)	 ≥8 ≥16	Ω
C_L	Load capacitor R_L = 8 Ω to 100 Ω (speaker/BTL output - modes 1,2,7) R_L = 16 Ω to 100 Ω (headphone, MLO output - modes 3,4,5,6) R_L > 100 Ω	 500 400 100	pF
R_{thja}	Flip-chip thermal resistance junction to ambient	90(2)	°C/W

1. For proper functionality of I2C bus, V_{CC} pins must not be grounded. ESD protection diodes ground data and clock wires and cause dysfunction of I^2C bus in this condition.
2. With heat sink surface 120 mm^2.

Table 3. I^2C electrical characteristics

Symbol	Parameter	Value	Unit
I^2CV_{CC}	I2C supply voltage(1)	2.7 to 5.5 V	V
V_{ILI}	Maximum low level input voltage on pins SDA, SCL	0.3 I2CVCC	V
V_{IH}	Minimum high level input voltage	0.7 I2CVCC	V
I_{IN}	Maximum input current (pins SDA, SCL), 0.4 V < V_{in} < 4.5 V	10	µA
F_{SCL}	SCL maximum clock frequency	400	kHz
V_{ol}	Max low level output voltage, SDA pin, I_{sink} = 3 mA	0.4	V

1. Must be less than or equal to the power supply voltage V_{CC} of the device.

2 Typical application schematic

Table 4. Description of external components

Components	Functional description
C_{s1}, C_{s2}	Supply bypass capacitors which provide power supply filtering.
C_b	Bypass capacitor which provides half-supply filtering.
C_{in1} to C_{in4}	Input capacitors which form together with input impedance Z_{in} first-order high pass filter to block DC voltage on inputs
C_{out}	Output capacitor which forms with output load R_L first-order high pass filter to block half-supply voltage on single-ended output.
R_1	Resistor to keep C_{out} charged for better pop performance on single-ended output.

Figure 1. Typical application for the TS4956 (modes 1, 2, 3, 4, 5 and 6)

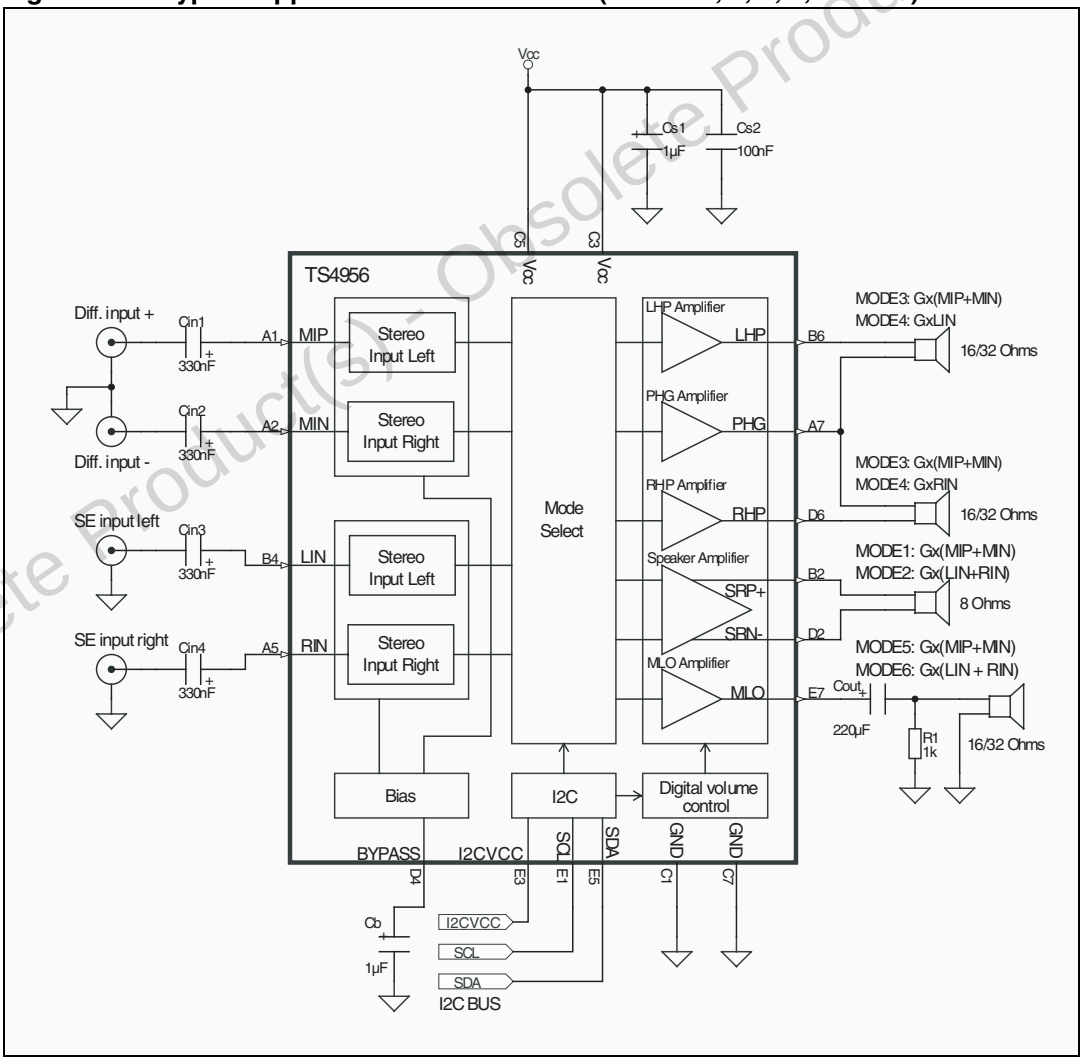
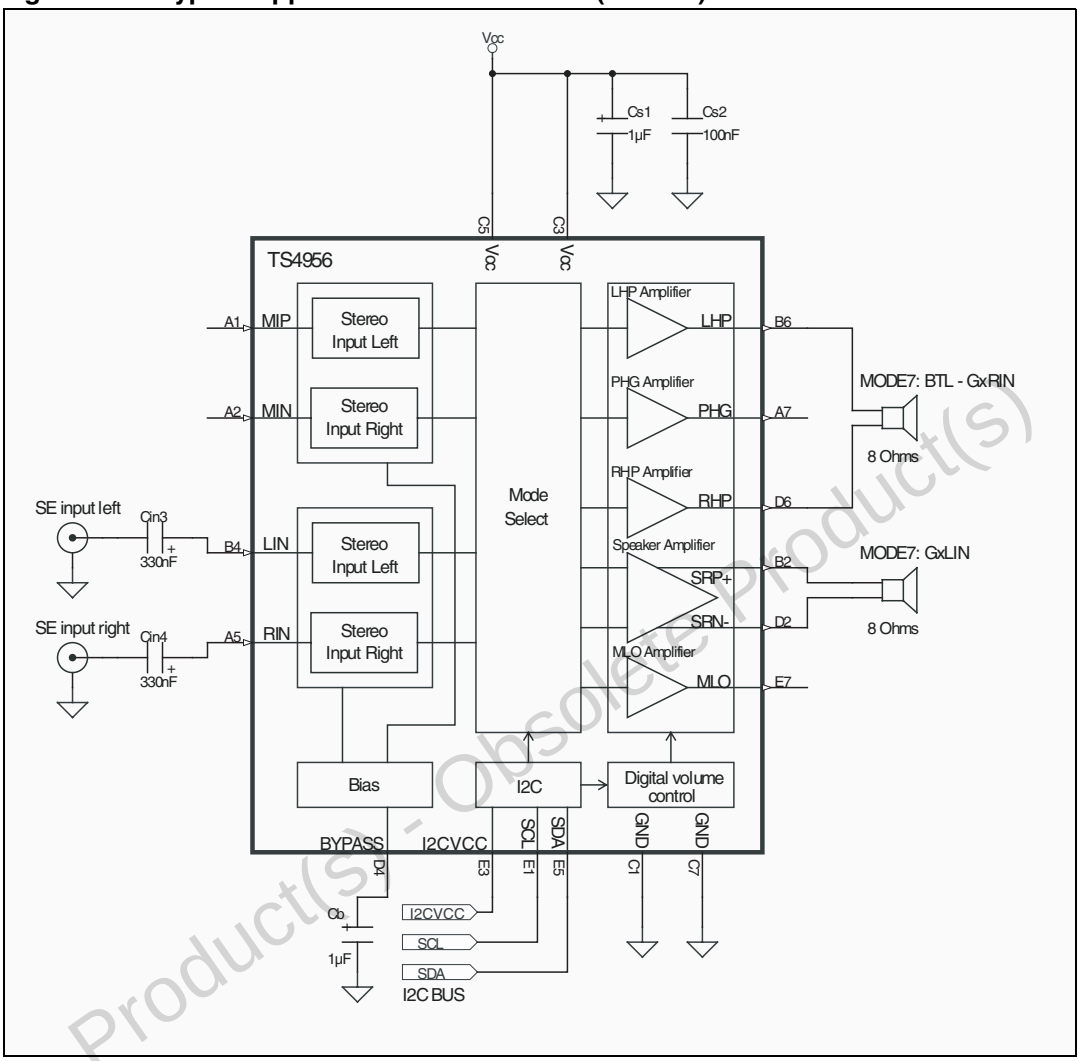


Figure 2. Typical application for the TS4956 (mode 7)



2.1 I²C interface

The TS4956 uses a serial bus, which conforms to the I²C protocol (the TS4956 must be powered when it is connected to the I²C bus), to control the chip's functions via two wires: clock and data.

The clock and data lines are bidirectional (open-collector) with an external chip pull-up resistor (typically 10 kΩ). The maximum clock frequency in fast-mode specified by the I²C standard is 400 kHz, and this frequency is supported by the TS4956. In this application, the TS4956 is always the slave device and the controlling MCU is the master device.

The I2CVCC pin determines the power supply of the TS4956's I²C interface. The voltage connected to this pin must be equal to or less than the TS4956 power supply voltage V_{CC}. The minimum value of the I2CVCC voltage is 2.7 V.

When the I2CVCC pin is connected to an I²C voltage, the TS4956 is ready to communicate via the I²C bus.

When the I2CVCC pin is connected to the ground, the TS4956 is in total standby mode, with an ultra-low standby current on the order of a few nanoamperes. In this condition the TS4956 cannot receive I²C commands from the I²C bus.

In both cases, pins SDA and SCL must respect logic HI or logic LOW thresholds (not floating) presented in *Table 3 on page 4*, in order for the circuit to function properly.

Table 5 summarizes the pin descriptions for the I²C bus interface.

Table 5. I²C bus interface: pin descriptions

Pin	Functional description
SDA	Serial data pin
SCL	Clock input pin
I2CVCC	I²C interface power supply

2.1.1 I²C operation description

The host MCU can write into the TS4946 control register to control the TS4956 and read from the control register to get the current configuration of the TS4956. The TS4956 is addressed by a single byte consisting of a 7-bit slave address and an R/W bit. The TS4956 control register address is $5Dh.

Table 6. First byte after the START message for addressing the device

A6	A5	A4	A3	A2	A1	A0	Rw
1	0	1	1	1	0	1	X

In order to write data into the TS4956 control register, after the "start" message the MCU must send the following data:

- send byte with the I²C 7-bit slave address and with the R/W bit set low.
- send the data (control register setting).

All bytes are sent with the MSB bit first. The transfer of written data ends with a "stop" message. When transmitting several bits of data, the data can be written without having to repeat the "start" message or address byte with the slave address.

In order to read data from the TS4956, after the "start" message, the MCU must send and receive the following data:

- send byte with the I²C 7-bit slave address and with the R/W bit set high.
- receive the data (control register value).

All bytes are read with the MSB bit first. The transfer of read data is ended with a "stop" message. When transmitting several bits of data, the data can be read with having to repeat the "start" message and the byte with slave address. In this case the value of the control register is read repeatedly.

Figure 3. I²C read/write operation

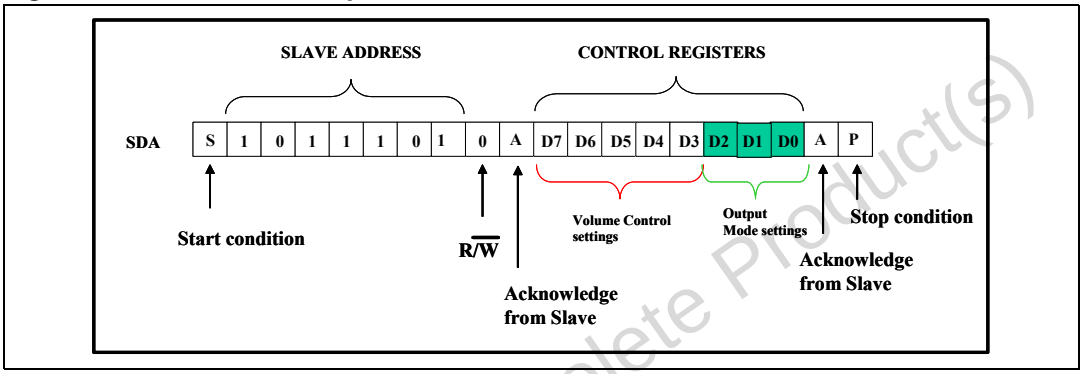


Table 7. Output mode selection: G from -34.5 dB to + 12 dB (by steps of 1.5 dB)(1)

Output mode #	RHP	LHP	Speaker P/N	Mono L/O
0	SD	SD	SD	SD
1	SD	SD	Gx (MIP + MIN)	SD
2	SD	SD	GX (RIN + LIN)	SD
3	GX (MIP + MIN)	GX (MIP + MIN)	SD	SD
4	G x RIN	G x LIN	SD	SD
5	SD	SD	SD	GX (MIP + MIN)
6	SD	SD	SD	GX (RIN + LIN)
7	BTL: G x RIN	BTL: G x RIN	G x LIN	SD

1. SD = shutdown mode
G = audio gain
MIP = mono input positive
MIN = mono input negative
RIN = stereo input right
LIN = stereo input left

2.1.2 Gain and mode setting operations

The gain of the TS4956 ranges from -34.5 dB to +12 dB. At power-up, the output channels are set to standby mode.

Table 8. Gain settings truth table

G: Gain (dB) #	D7 (MSB)	D6	D5	D4	D3
-34.5	0	0	0	0	0
-33	0	0	0	0	1
-31.5	0	0	0	1	0
-30	0	0	0	1	1
-28.5	0	0	1	0	0
-27	0	0	1	0	1
-25.5	0	0	1	1	0
-24	0	0	1	1	1
-22.5	0	1	0	0	0
-21	0	1	0	0	1
-19.5	0	1	0	1	0
-18	0	1	0	1	1
-16.5	0	1	1	0	0
-15	0	1	1	0	1
-13.5	0	1	1	1	0
-12	0	1	1	1	1
-10.5	1	0	0	0	0
-9	1	0	0	0	1
-7.5	1	0	0	1	0
-6	1	0	0	1	1
-4.5	1	0	1	0	0
-3	1	0	1	0	1
-1.5	1	0	1	1	0
0	1	0	1	1	1
+1.5	1	1	0	0	0
+3	1	1	0	0	1
+4.5	1	1	0	1	0
+6	1	1	0	1	1
+7.5	1	1	1	0	0
+9	1	1	1	0	1
+10.5	1	1	1	1	0
+12	1	1	1	1	1

Table 9. Output mode settings truth table

D2	D1	D0	Comments
0	0	0	OUTPUT MODE 0
0	0	1	OUTPUT MODE 1
0	1	0	OUTPUT MODE 2
0	1	1	OUTPUT MODE3
1	0	0	OUTPUT MODE 4
1	0	1	OUTPUT MODE 5
1	1	0	OUTPUT MODE 6
1	1	1	OUTPUT MODE 7

2.1.3 Acknowledge bit

The number of data bytes transferred between the start and the stop conditions from the CPU master to the TS4956 slave is unlimited. Each byte of eight bits is followed by one acknowledge bit.

The addressed TS4956 generates an acknowledge after receiving each byte that has been clocked out.

3 Electrical characteristics

Table 10. V_{CC} = +2.7 V, GND = 0 V, T_{amb} = 25° C (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{CC}	Supply current	Mode 1, 2, no input signal, no load		3.4	4.4	mA
		Mode 3, no input signal, no load		4.6	6	
		Mode 4, no input signal, no load		4.4	5.7	
		Mode 5, 6, no input signal, no load		1.75	2.3	
		Mode 7, no input signal, no load		5.7	7.4	
I_{STBY}	Standby current	No input signal		0.5	2	µA
V_{OO}	Output offset voltage	No input signal Modes 1, 2 speaker output, RL = 8 Ω Mode 3 headphone outputs, RL = 16 Ω Mode 4 headphone outputs, RL = 16 Ω Mode 7 BTL, speaker output, R_L = 8 Ω		 5 5 5 5	 50 50 20 20	mV
P_{out}	Headphone output power (phantom ground mode)	Modes 3, 4 THD+N = 1% max, F = 1 kHz, R_L = 16 Ω THD+N = 1% max, F = 1 kHz, R_L = 32 Ω	 30 20	 35 25		mW
	BTL, speaker output power	Modes 1, 2, 7 THD+N = 1% max, F = 1 kHz, R_L = 8 Ω	270	285		
	MLO output power	Modes 5, 6 THD+N = 1% max, F = 1 kHz, R_L = 16 Ω THD+N = 1% max, F = 1 kHz, R_L = 32 Ω	 35 20	 42 25		
THD+N	Total harmonic distortion + noise	G = +1.5 dB, 20 Hz < F < 20 kHz Modes 1, 2, 7, RL = 8 Ω, Pout = 200 mW Modes 3, 4, RL = 16 Ω, Pout = 15 mW Modes 5, 6, R_L = 16 Ω, P_{out} = 30 mW		 0.5 0.5 0.5		%
PSRR	Power supply rejection ratio(1)	F = 217Hz, G = +1.5 dB, V_{ripple} = 200 mVpp, Inputs grounded, C_b = 1 µF Mode 1, speaker output, RL = 8 Ω Mode 2, speaker output, RL = 8 Ω Mode 3, headphone outputs, RL = 16 Ω Mode 4, headphone outputs, RL = 16 Ω Mode 5, MLO output, RL = 16 Ω Mode 6, MLO output, RL = 16 Ω Mode 7, BTL, speaker outputs, RL = 8 Ω		 60 55 61 75 62 57 73	 	dB

Table 10. V_{CC} = +2.7 V, GND = 0 V, T_{amb} = 25° C (unless otherwise specified) (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Crosstalk	Channel separation	Mode 4 F = 1 kHz, R_L = 16 Ω, P_{out} = 15 mW F = 20 Hz to 20 kHz, R_L = 16 Ω, P_{out} = 15 mW Mode 7 F = 1 kHz, R_L = 8 Ω, P_{out} = 200 mW F = 20 Hz to 20 kHz, R_L = 8 Ω, P_{out} = 200 mW		 50 50 80 60		dB
SNR	Signal-to-noise ratio	A-weighted, G = +1.5 dB, THD+N < 0.5%, 20 Hz < F < 20 kHz Mode 1 - speaker output, RL = 8 Ω Mode 2 - speaker output, RL = 8 Ω Mode 3 - headphone output, RL = 16 Ω Mode 4 - headphone output, RL = 16 Ω Mode 5 - MLO output, RL = 16 Ω Mode 6 - MLO output, R = 16 Ω Mode 7 - BTL, speaker output, R_L = 8 Ω, G = +10.5 dB		 91 90 84 90 85 85 92		dB
G	Digital gain range		-34.5		+12	dB
	Digital gain stepsize			1.5		dB
	Stepsize error		0.1		0.6	dB
Z_{in}	Input impedance, all gain setting	Differential input Differential input impedance (MIP to MIN) MIP input impedance referenced to ground MIN input impedance referenced to ground Stereo input RIN input impedance LIN input impedance	 48 24 36 24 24	 60 30 45 30 30	 72 36 54 36 36	kΩ
t_{WU}	Wake-up time			70	90	ms
t_{STBY}	Standby time			1		µs

1. Dynamic measurements - 20*log(rms(V_{out})/rms(V_{ripple})). V_{ripple} is an added sinus signal to V_{CC} at f = 217 Hz.

Table 11. V_{CC} = +3.3 V, GND = 0 V, T_{amb} = 25° C (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{CC}	Supply current	Mode 1, 2, no input signal, no load		3.6	4.7	mA
		Mode 3, no input signal, no load		4.8	6.2	
		Mode 4, no input signal, no load		4.6	6	
		Modes 5, 6, no input signal, no load		1.8	2.4	
		Mode 7, no input signal, no load		6	7.8	
I_{STBY}	Standby current	No input signal		0.5	2	µA
V_{OO}	Output offset voltage	No input signal Modes 1, 2 speaker output, RL = 8 Ω Mode 3 headphone outputs, RL = 16 Ω Mode 4 headphone outputs, RL = 16 Ω Mode 7 BTL, speaker output, R_L = 8 Ω		 5 5 5 5	 50 50 20 20	mV
P_{out}	Headphone output power (phantom ground mode)	Modes 3, 4 THD+N = 1% max, F = 1 kHz, RL = 16 Ω THD+N = 1% max, F = 1 kHz, RL = 32 Ω	 32 30	 38(1) 36(1)		mW
	BTL, speaker output power	Modes 1, 2, 7 THD+N = 1% max, F = 1 kHz, RL = 8 Ω	430	450		
	MLO output power	Modes 5, 6 THD+N = 1% max, F = 1 kHz, RL = 16 Ω THD+N = 1% max, F = 1 kHz, RL = 32 Ω	 58 32	 65 38		
THD+N	Total harmonic distortion + noise	G = +1.5 dB, 20 Hz < F < 20 kHz Modes 1, 2, 7, RL = 8 Ω, Pout = 300 mW Modes 3, 4, RL = 16 Ω, Pout = 15 mW Modes 5, 6, RL = 16 Ω, Pout = 50 mW		 0.5 0.5 0.5		%
PSRR	Power supply rejection ratio(2)	F = 217Hz, G = +1.5 dB, Vripple = 200 mVpp, inputs grounded, Cb = 1 µF Mode 1, speaker output, RL = 8 Ω Mode 2, speaker output, RL = 8 Ω Mode 3, headphone outputs, RL = 16 Ω Mode 4, headphone outputs, RL = 16 Ω Mode 5, MLO output, RL = 16 Ω Mode 6, MLO output, RL = 16 Ω Mode 7, BTL, speaker outputs, RL = 8 Ω		 63 57 63 77 64 58 74		dB

Table 11. V_{CC} = +3.3 V, GND = 0 V, T_{amb} = 25° C (unless otherwise specified) (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Crosstalk	Channel separation	Mode 4 F = 1 kHz, RL = 16 Ω, Pout = 15 mW F = 20 Hz to 20 kHz, RL = 16 Ω, Pout = 15 mW Mode 7 F = 1 kHz, RL = 8 Ω, Pout = 300 mW F = 20 Hz to 20 kHz, RL = 8 Ω, Pout = 300 mW		 50 50 80 60		dB
SNR	Signal-to-noise ratio	A-weighted, G = +1.5 dB, THD+N < 0.5%, 20 Hz < F < 20 kHz Mode 1 - speaker output, RL = 8 Ω Mode 2 - speaker output, RL = 8 Ω Mode 3 - headphone output, RL = 16 Ω Mode 4 - headphone output, RL = 16 Ω Mode 5 - MLO output, RL = 16 Ω Mode 6 - MLO output, R = 16 Ω Mode 7 - BTL, speaker output, RL = 8 Ω, G = +10.5 dB		 93 92 85 91 87 87 95		dB
G	Digital gain range		-34.5		+12	dB
	Digital gain stepsize			1.5		dB
	Stepsize error		0.1		0.6	dB
Z_{in}	Input impedance, all gain setting	Differential input Differential input impedance (MIP to MIN) MIP input impedance referenced to ground MIN input impedance referenced to ground Stereo input RIN input impedance LIN input impedance	 48 24 36 24 24	 60 30 45 30 30	 72 36 54 36 36	kΩ
t_{WU}	Wake-up time			70	90	ms
t_{STBY}	Standby time			1		µs

1. Internal power limitation on headphone outputs (see application information).
2. Dynamic measurements - 20*log(rms(V_{out})/rms(V_{ripple})). V_{ripple} is an added sinus signal to V_{CC} at F = 217 Hz.

Table 12. V_{CC} = +5 V, GND = 0 V, T_{amb} = 25° C (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{CC}	Supply current	Mode 1, 2, no input signal, no load		4	5.2	mA
		Mode 3, no input signal, no load		5.3	6.9	
		Mode 4, no input signal, no load		5.2	6.8	
		Modes 5, 6, no input signal, no load		1.9	2.5	
		Mode 7, no input signal, no load		6.7	8.7	
I_{STBY}	Standby current	No input signal		0.5	2	µA
V_{OO}	Output offset voltage	No input signal Modes 1, 2 speaker output, RL = 8 Ω Mode 3 headphone outputs, RL = 16 Ω Mode 4 headphone outputs, RL = 16 Ω Mode 7 BTL, speaker output, RL = 8 Ω		 5 5 5 5	 50 50 20 20	mV
P_{out}	Headphone output power (phantom ground mode)	Modes 3, 4 THD+N = 1% max, F = 1 kHz, RL = 16 Ω THD+N = 1% max, F = 1 kHz, RL = 32 Ω	 32 35	 39(1) 43(1)		mW
	BTL, speaker output power	Modes 1, 2, 7 THD+N = 1% max, F = 1 kHz, RL = 8 Ω	1000	1055		
	MLO output power	Modes 5, 6 THD+N = 1% max, F = 1 kHz, RL = 16 Ω THD+N = 1% max, F = 1 kHz, RL = 32 Ω	140 80	150 88		
THD+N	Total harmonic distortion + noise	G = +1.5 dB, 20 Hz < F < 20 kHz Modes 1, 2, 7, RL = 8 Ω, Pout = 700 mW Modes 3, 4, RL = 16 Ω, Pout = 15 mW Modes 5, 6, RL = 16 Ω, Pout = 100 mW		 0.5 0.5 0.5		%
PSRR	Power supply rejection ratio(2)	F = 217Hz, G = +1.5 dB, Vripple = 200 mVpp, inputs grounded, Cb = 1 µF Mode 1, speaker output, RL = 8 Ω Mode 2, speaker output, RL = 8 Ω Mode 3, headphone outputs, RL = 16 Ω Mode 4, headphone outputs, RL = 16 Ω Mode 5, MLO output, RL = 16 Ω Mode 6, MLO output, RL = 16 Ω Mode 7, BTL, speaker outputs, RL = 8 Ω		 66 60 65 78 66 61 75		dB

Table 12. V_{CC} = +5 V, GND = 0 V, T_{amb} = 25° C (unless otherwise specified) (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Crosstalk	Channel separation	Mode 4 F = 1 kHz, RL = 16 Ω, Pout = 15 mW F = 20 Hz to 20 kHz, RL = 16 Ω, Pout = 15 mW Mode 7 F = 1 kHz, RL = 8 Ω, Pout = 700 mW F = 20 Hz to 20 kHz, RL = 8 Ω, Pout = 700 mW		 50 50 80 60		dB
SNR	Signal-to-noise ratio	A-weighted, G = +1.5 dB, THD+N < 0.5%, 20 Hz < F < 20 kHz Mode 1 - speaker output, RL = 8 Ω Mode 2 - speaker output, RL = 8 Ω Mode 3 - headphone output, RL = 16 Ω Mode 4 - headphone output, RL = 16 Ω Mode 5 - MLO output, RL = 16 Ω Mode 6 - MLO output, R = 16 Ω Mode 7 - BTL, Speaker output, RL = 8 Ω, G = +10.5 dB		 96 96 85 91 90 90 98		dB
G	Digital gain range		-34.5		+12	dB
	Digital gain stepsize			1.5		dB
	Stepsize error		0.1		0.6	dB
Z_{in}	Input impedance, all gain setting	Differential input Differential input impedance (MIP to MIN) MIP input impedance referenced to ground MIN input impedance referenced to ground Stereo input RIN input impedance LIN input impedance	 48 24 36 24 24	 60 30 45 30 30	 72 36 54 36 36	kΩ
t_{WU}	Wake-up time			70	90	ms
t_{STBY}	Standby time			1		µs

1. Internal power limitation on headphone outputs (see application information).
2. Dynamic measurements - 20*log(rms(V_{out})/rms(V_{ripple})). V_{ripple} is an added sinus signal to V_{CC} at F = 217 Hz.

Table 13. Output noise V_{CC} = 2.7 V to 5.5 V (all inputs grounded)

	G = +12 dB		G = +10.5 dB		G = +1.5 dB	
	A-weighted filter	Unweighted filter (20Hz - 20kHz)	A-weighted filter	Unweighted filter (20Hz - 20kHz)	A-weighted filter	Unweighted filter (20Hz - 20kHz)
	V_{out} (µV)	V_{out} (µV)	V_{out} (µV)	V_{out} (µV)	V_{out} (µV)	V_{out} (µV)
Mode 1 - SPK out	54	80	67	100	45	66
Mode 2 - SPK out	67	99	75	111	45	69
Mode 3 - LHP, RHP	55	80	68	100	45	67
Mode 4 - LHP, RHP	29	43	35	52	23	34
Mode 5 - MLO	53	80	66	97	45	66
Mode 6 - MLO	65	96	73	106	45	67
Mode 7 - BTL, SPK out	29	42	35	52	23	34

Figure 4. THD+N vs. output power

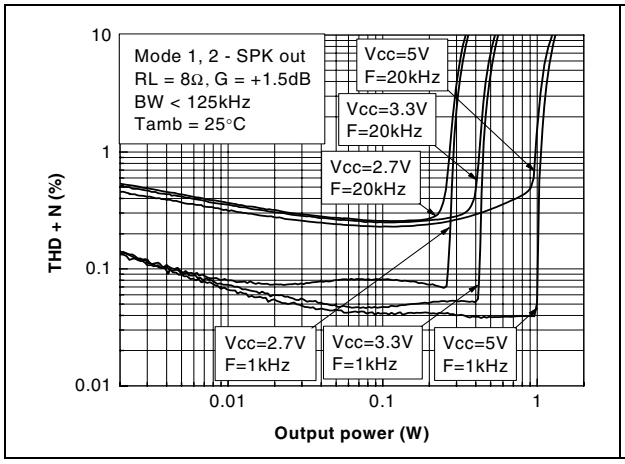


Figure 5. THD+N vs. output power

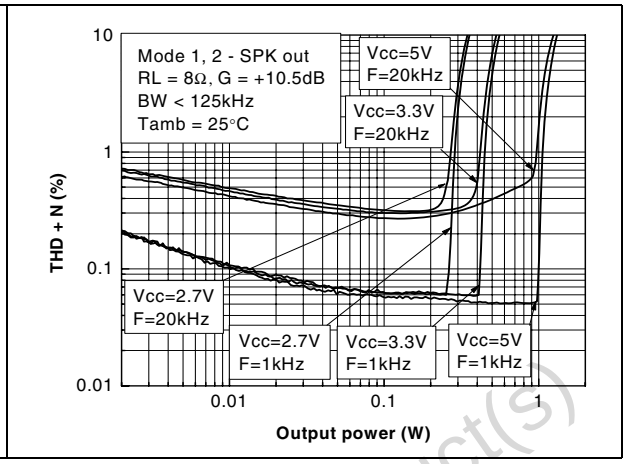


Figure 6. THD+N vs. output power

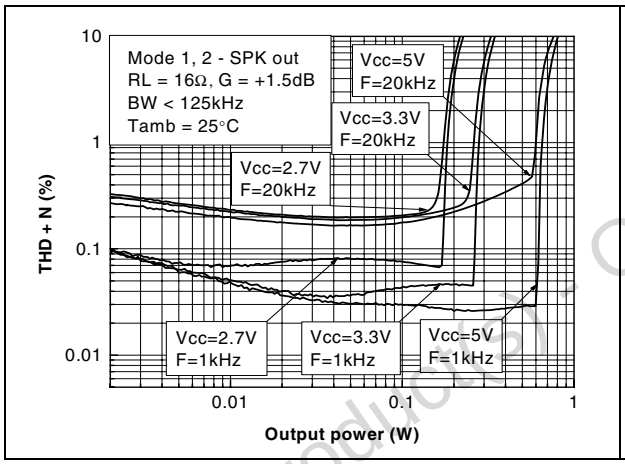


Figure 7. THD+N vs. output power

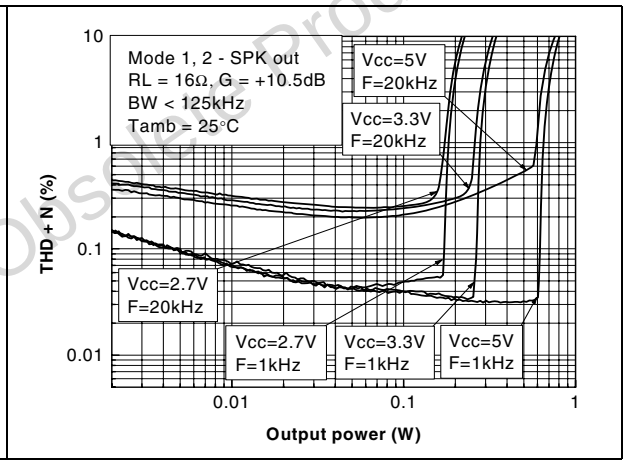


Figure 8. THD+N vs. output power

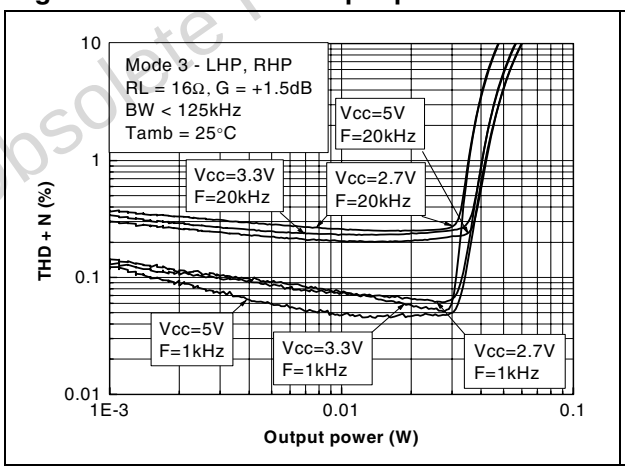


Figure 9. THD+N vs. output power

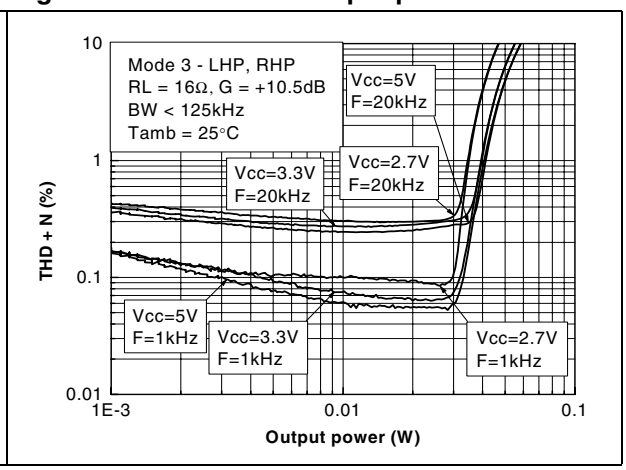


Figure 10. THD+N vs. output power

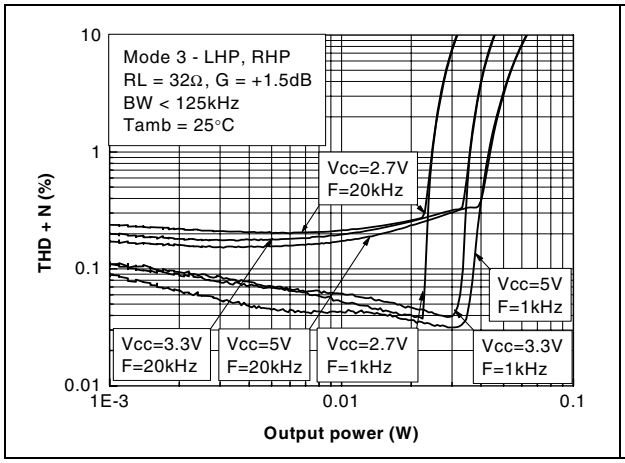


Figure 11. THD+N vs. output power

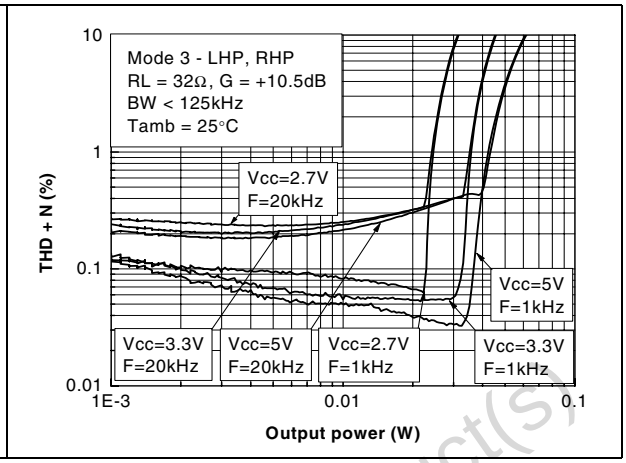


Figure 12. THD+N vs. output power

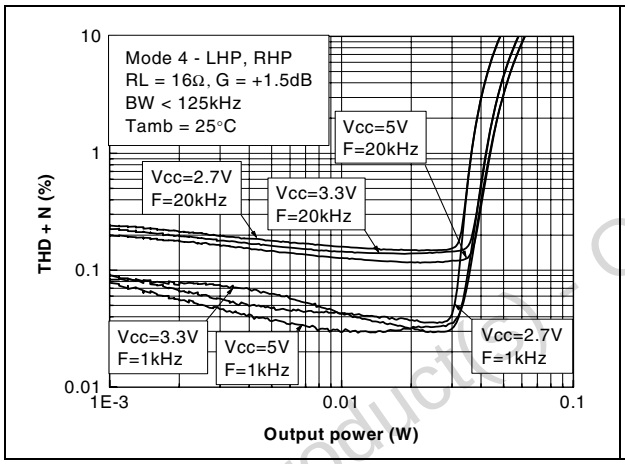


Figure 13. THD+N vs. output power

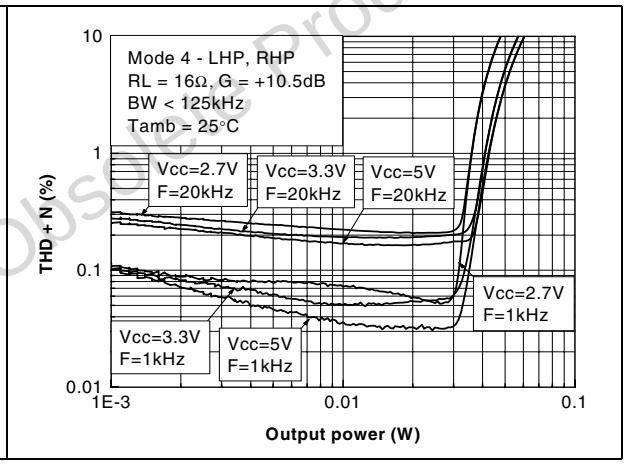


Figure 14. THD+N vs. output power

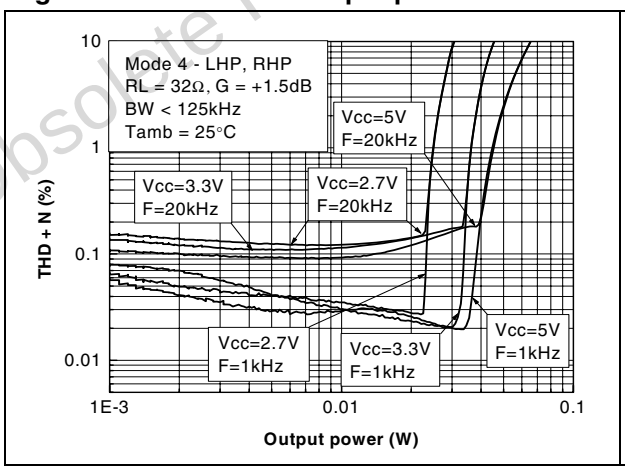


Figure 15. THD+N vs. output power

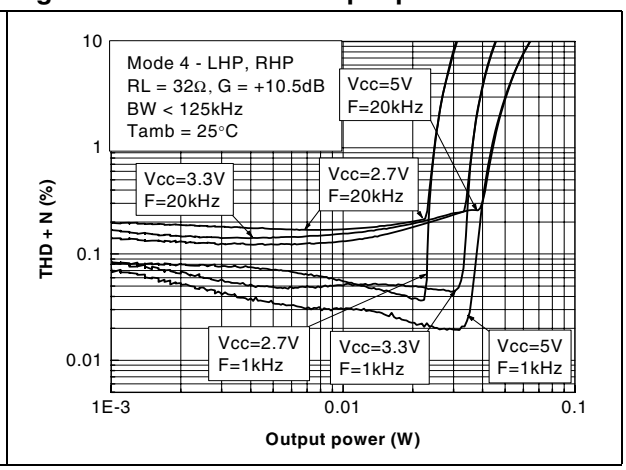


Figure 16. THD+N vs. output power

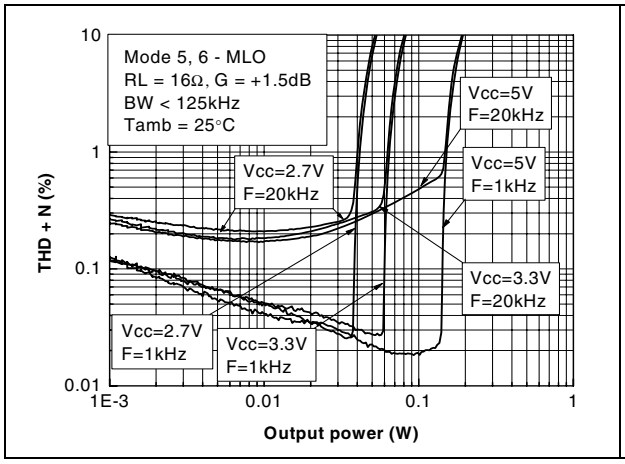


Figure 17. THD+N vs. output power

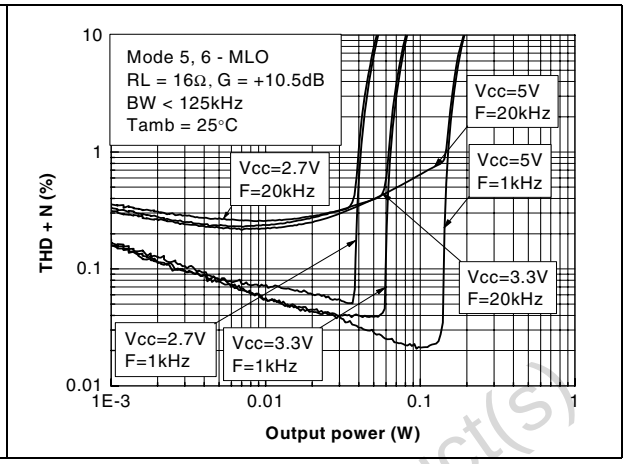


Figure 18. THD+N vs. output power

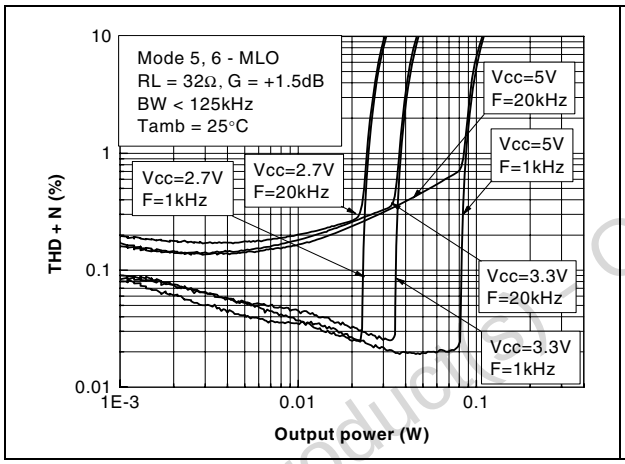


Figure 19. THD+N vs. output power

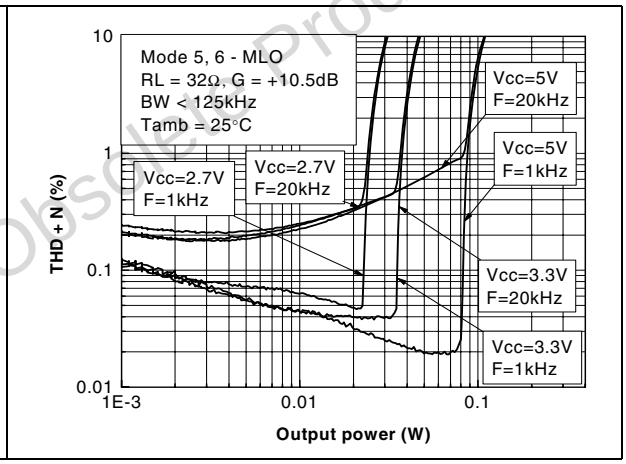


Figure 20. THD+N vs. output power

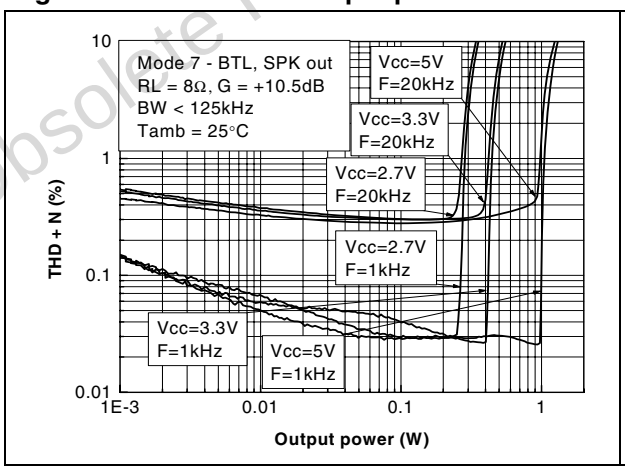


Figure 21. THD+N vs. output power

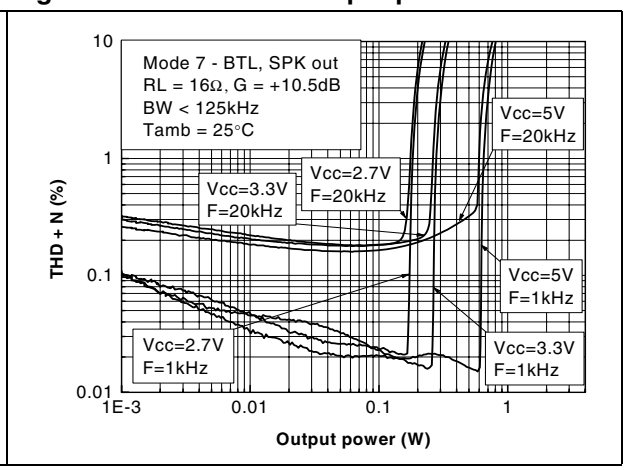


Figure 22. THD+N vs. frequency

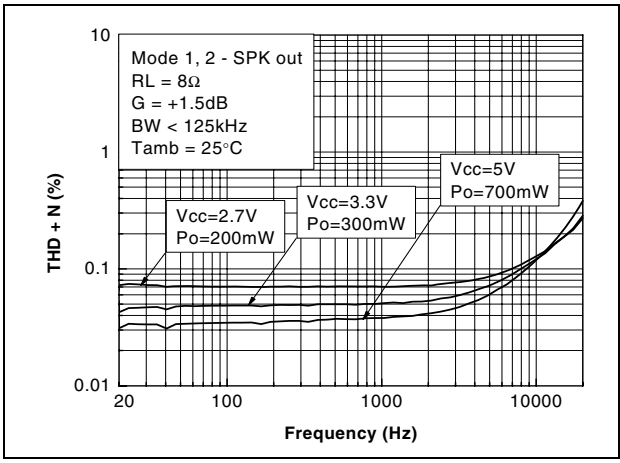


Figure 23. THD+N vs. frequency

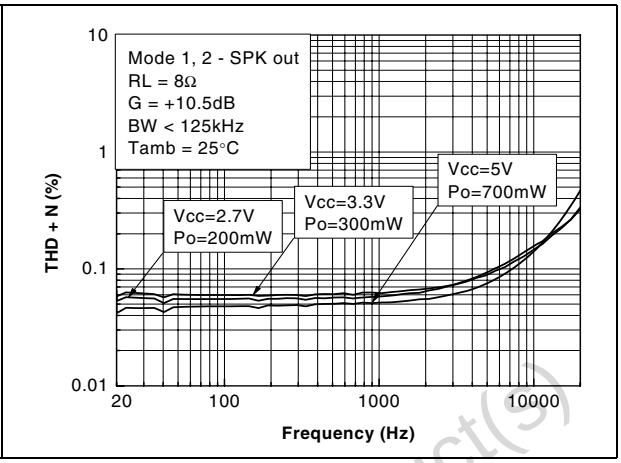


Figure 24. THD+N vs. frequency

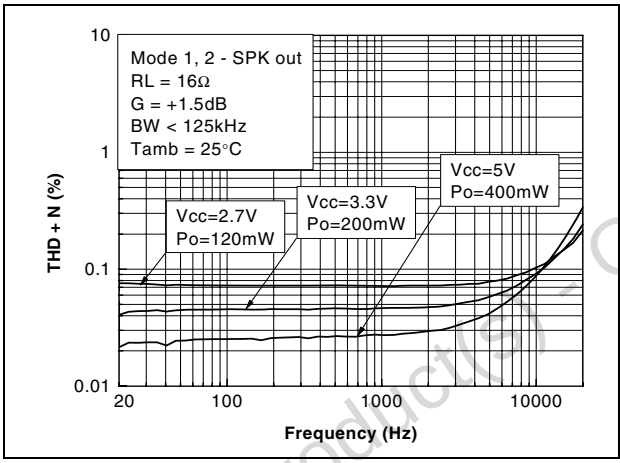


Figure 25. THD+N vs. frequency

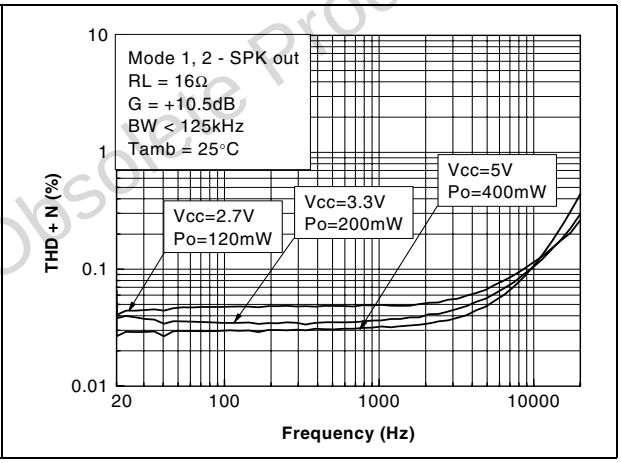


Figure 26. THD+N vs. frequency

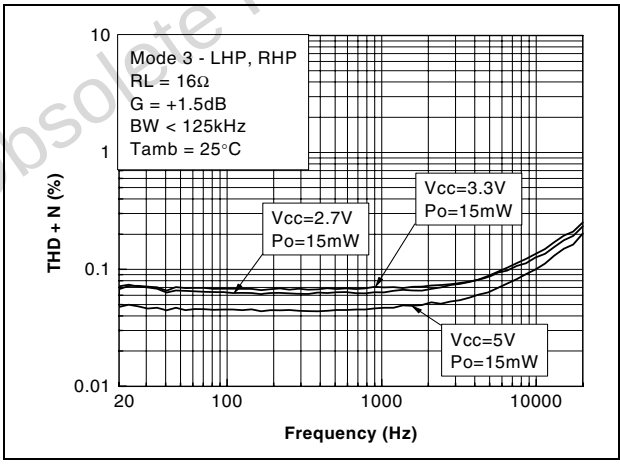


Figure 27. THD+N vs. frequency

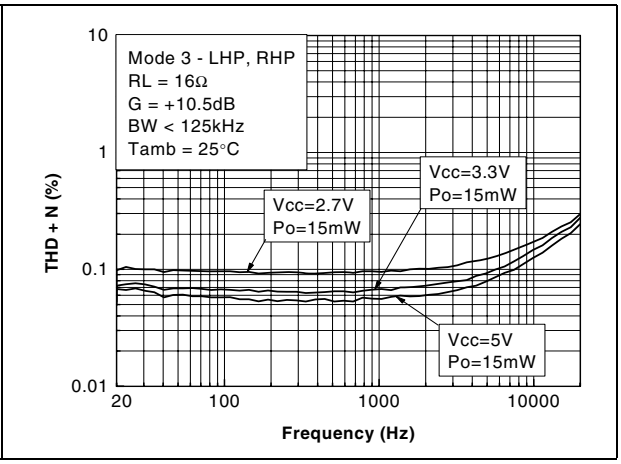


Figure 28. THD+N vs. frequency

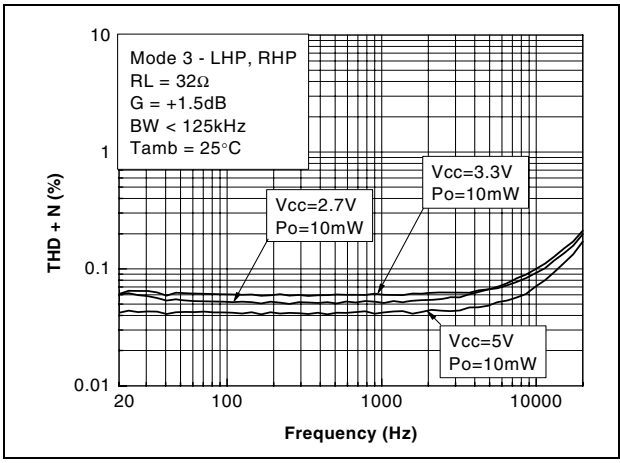


Figure 29. THD+N vs. frequency

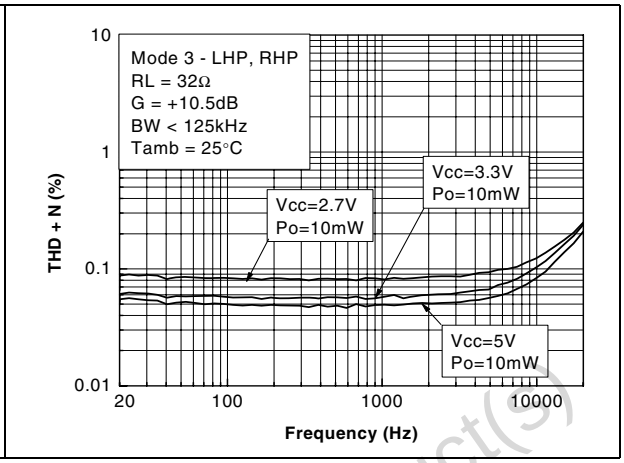


Figure 30. THD+N vs. frequency

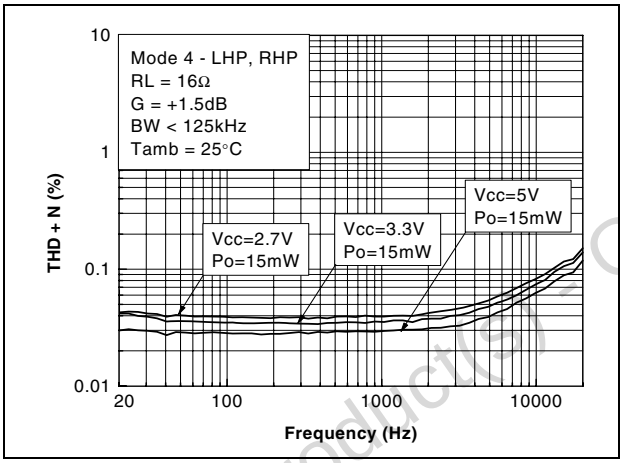


Figure 31. THD+N vs. frequency

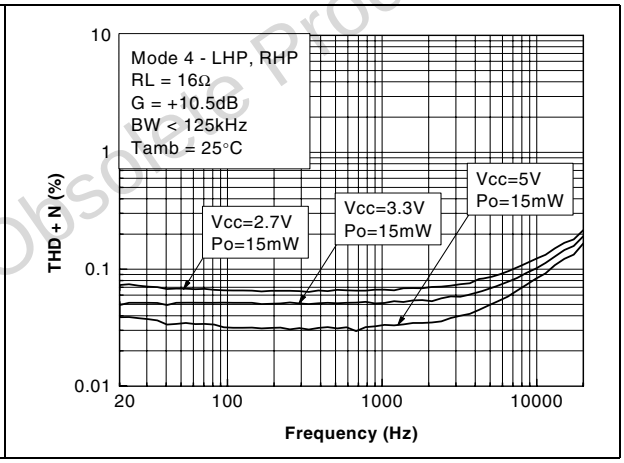


Figure 32. THD+N vs. frequency

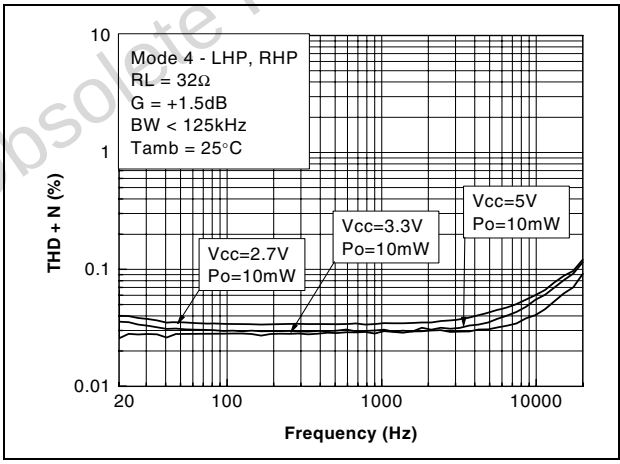


Figure 33. THD+N vs. frequency

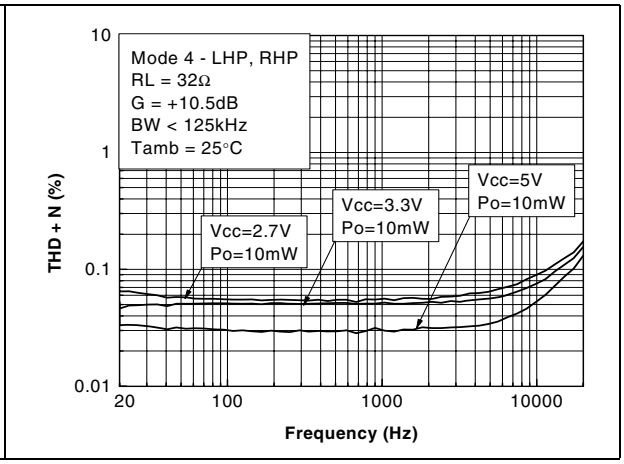


Figure 34. THD+N vs. frequency

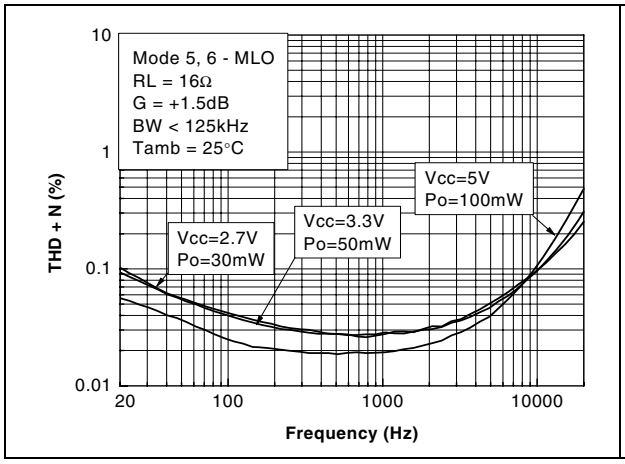


Figure 35. THD+N vs. frequency

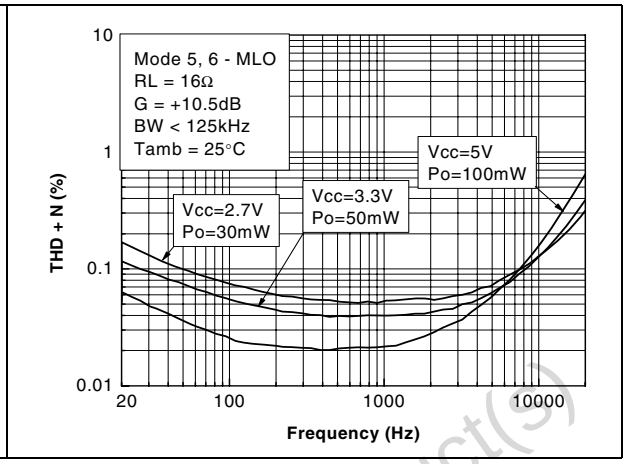


Figure 36. THD+N vs. frequency

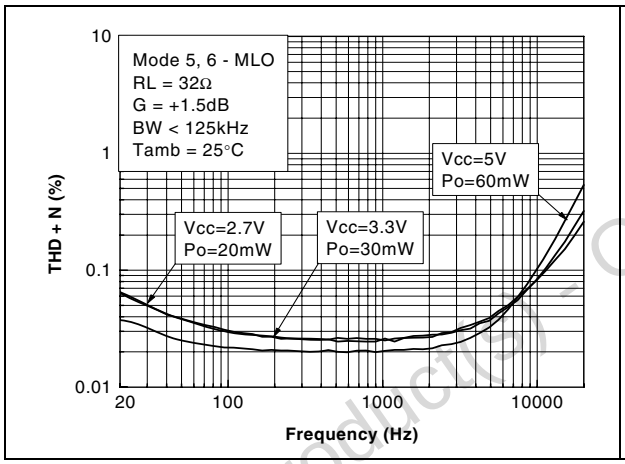


Figure 37. THD+N vs. frequency

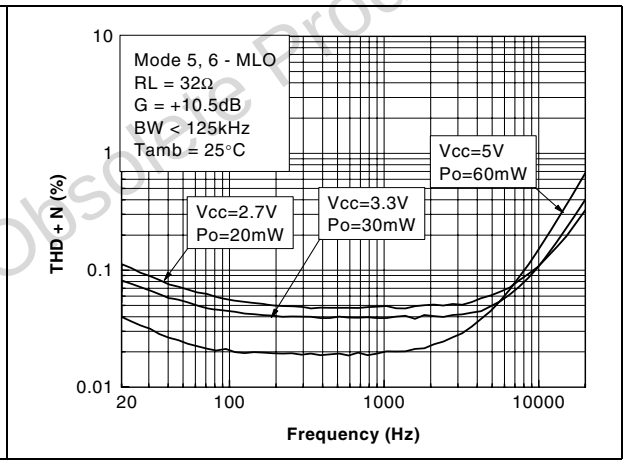


Figure 38. THD+N vs. frequency

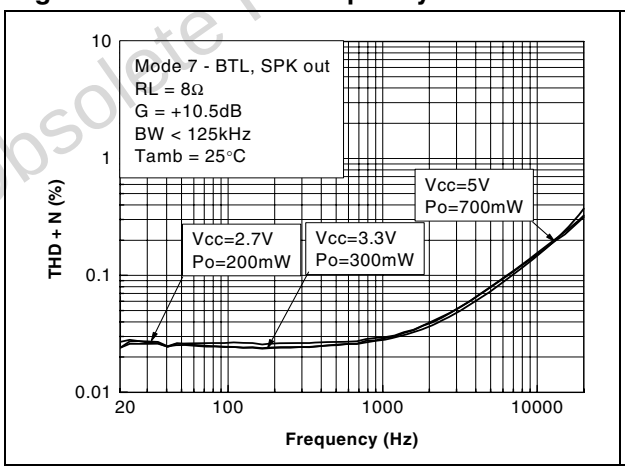


Figure 39. THD+N vs. frequency

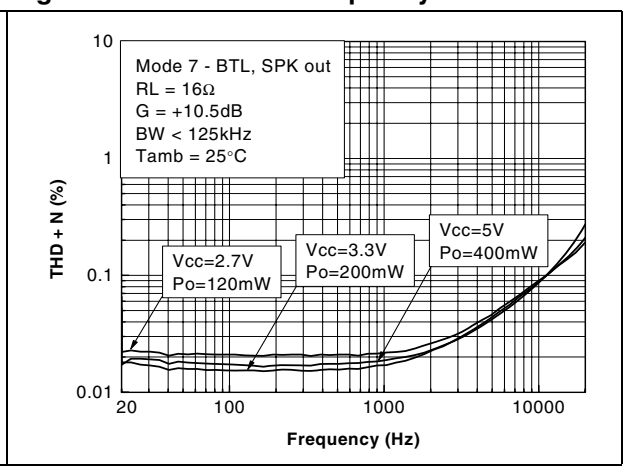


Figure 40. Output power vs. power supply voltage

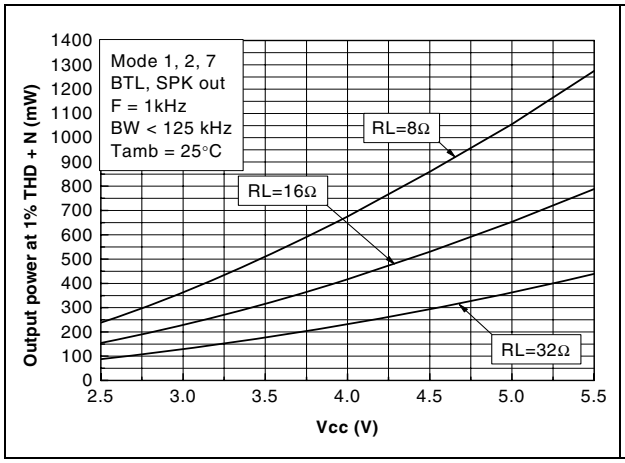


Figure 41. Output power vs. power supply voltage

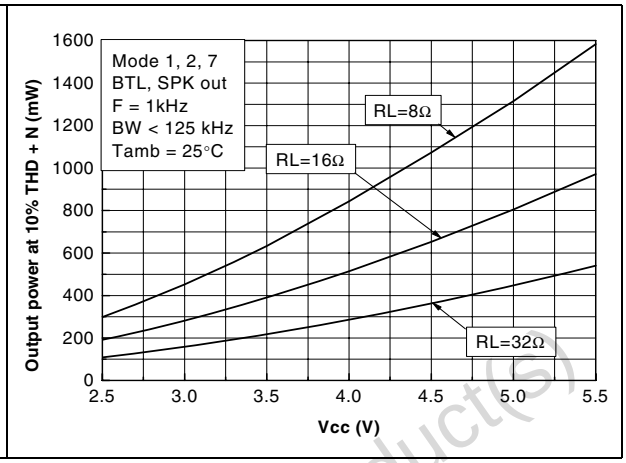


Figure 42. Output power vs. power supply voltage

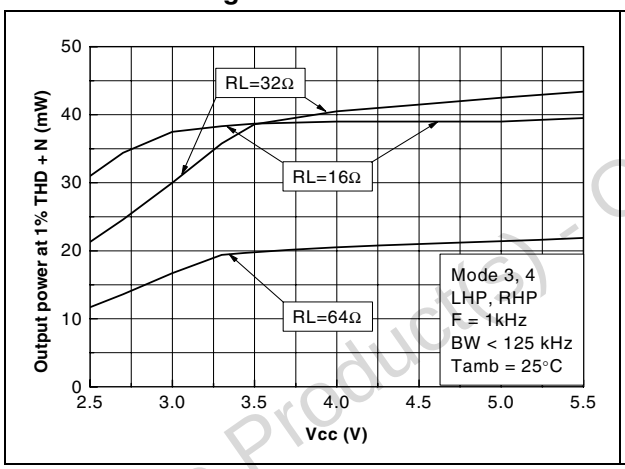


Figure 43. Output power vs. power supply voltage

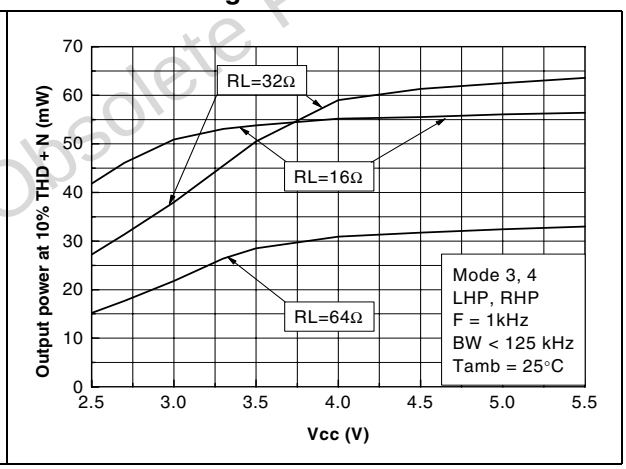


Figure 44. Output power vs. power supply voltage

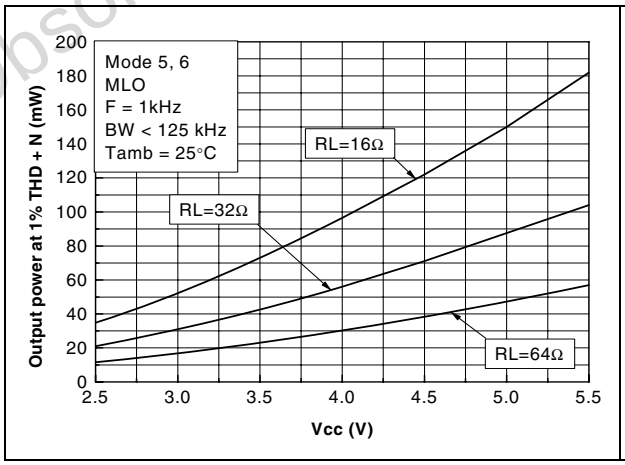


Figure 45. Output power vs. power supply voltage

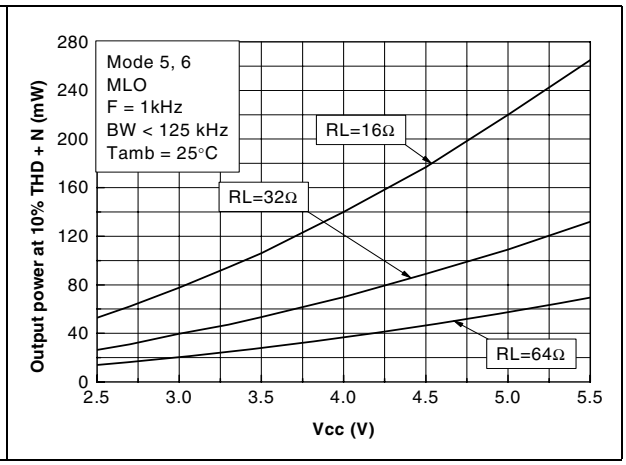


Figure 46. Output power vs. load resistance

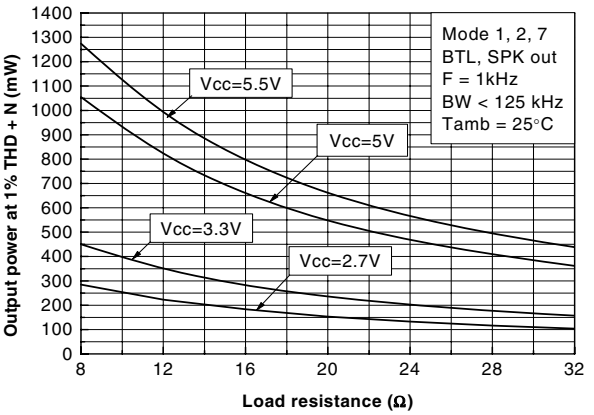


Figure 47. Output power vs. load resistance

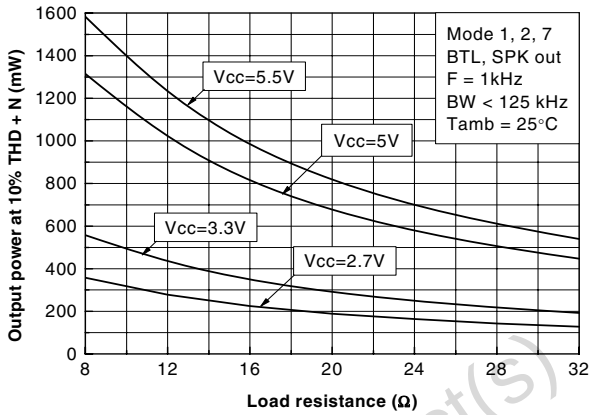


Figure 48. Output power vs. load resistance

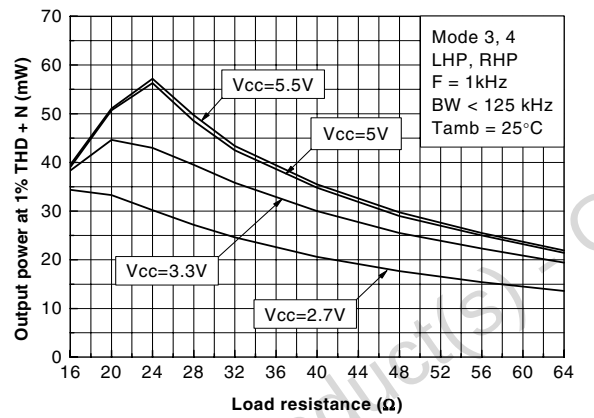


Figure 49. Output power vs. load resistance

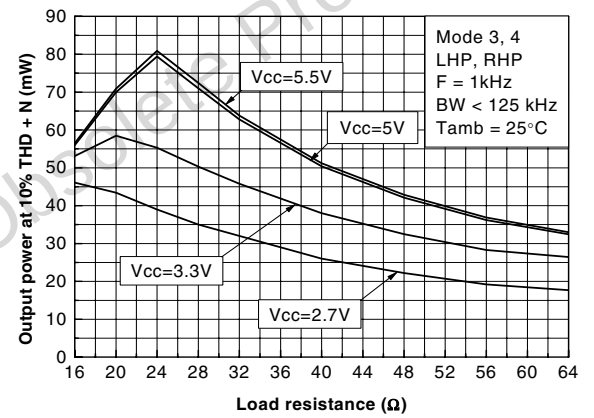


Figure 50. Output power vs. load resistance

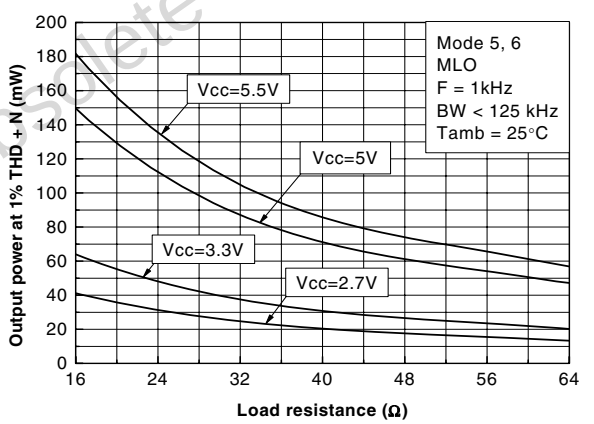


Figure 51. Output power vs. load resistance

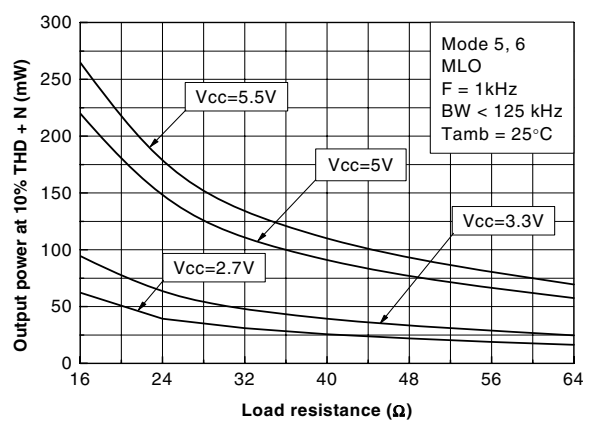


Figure 52. PSRR vs. frequency

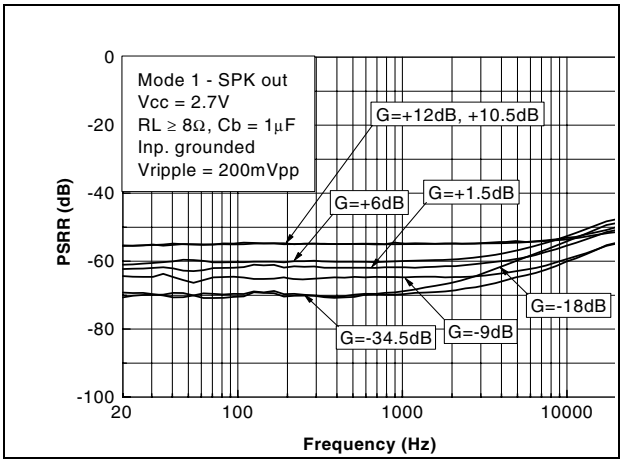


Figure 53. PSRR vs. frequency

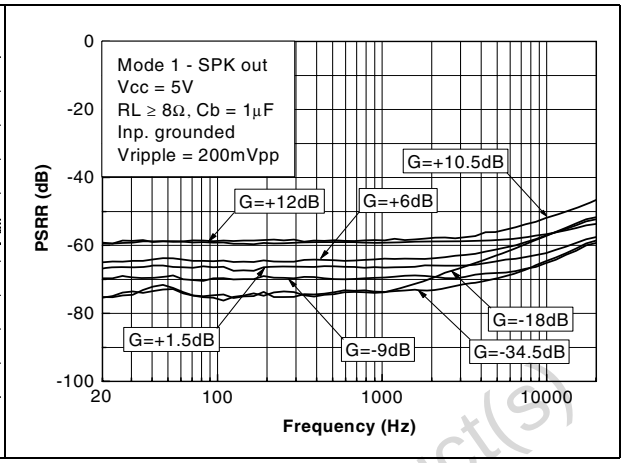


Figure 54. PSRR vs. frequency

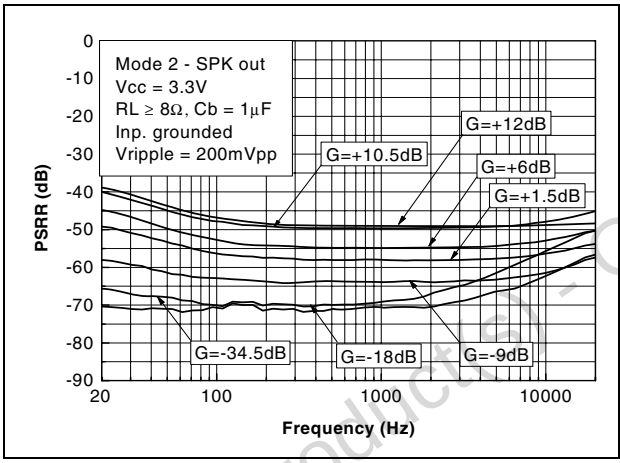


Figure 55. PSRR vs. frequency

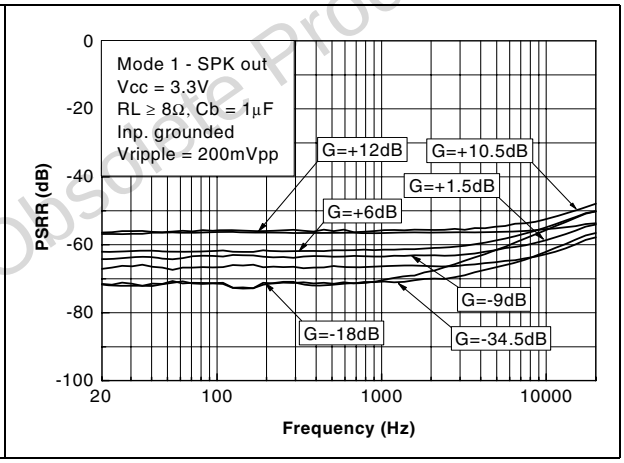


Figure 56. PSRR vs. frequency

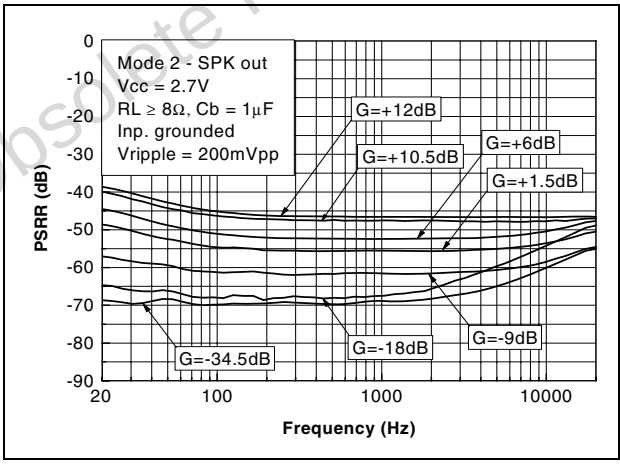


Figure 57. PSRR vs. frequency

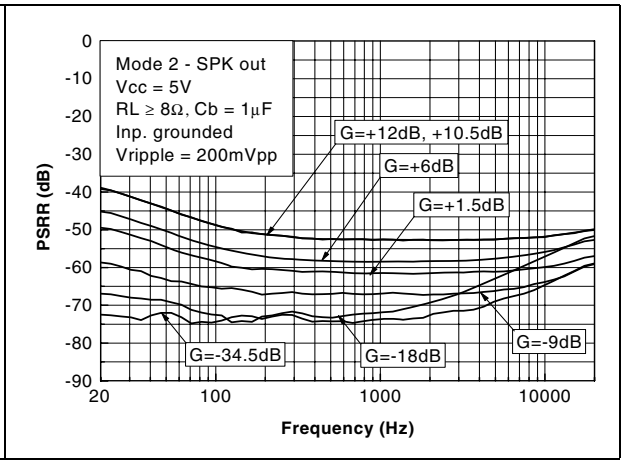


Figure 58. PSRR vs. frequency

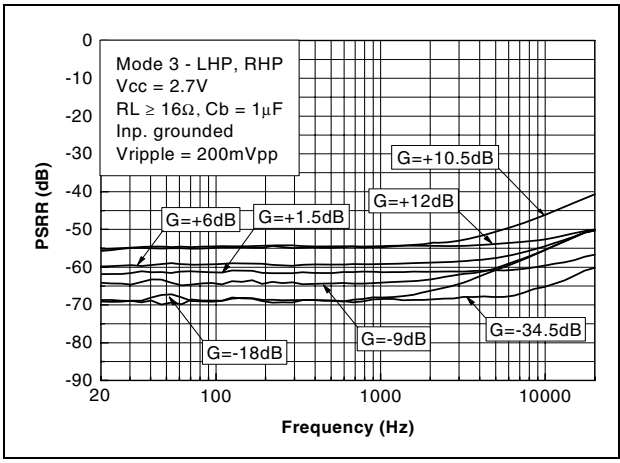


Figure 59. PSRR vs. frequency

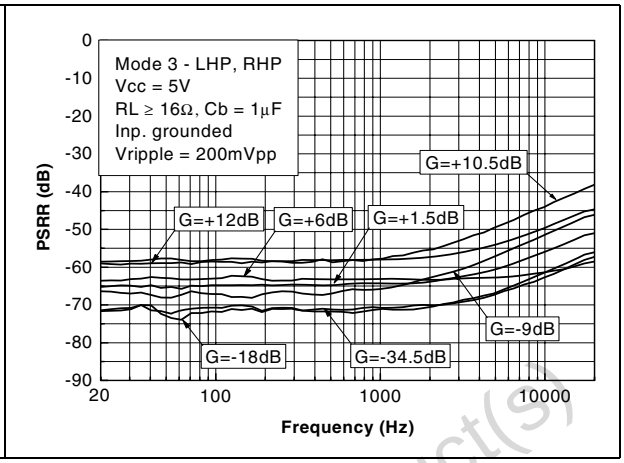


Figure 60. PSRR vs. frequency

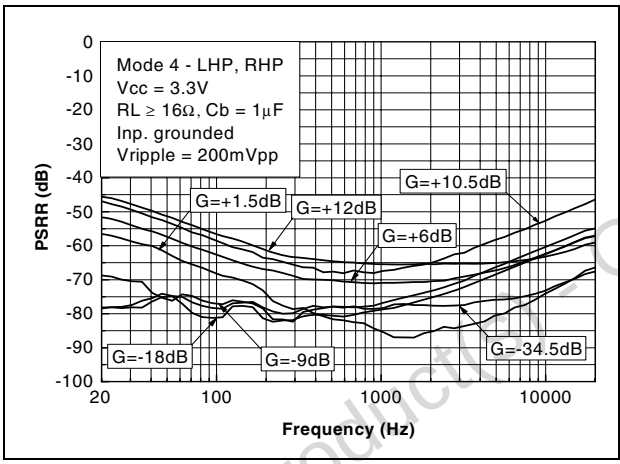


Figure 61. PSRR vs. frequency

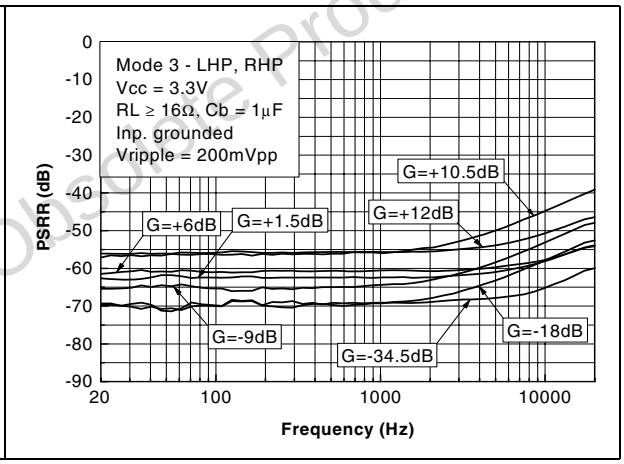


Figure 62. PSRR vs. frequency

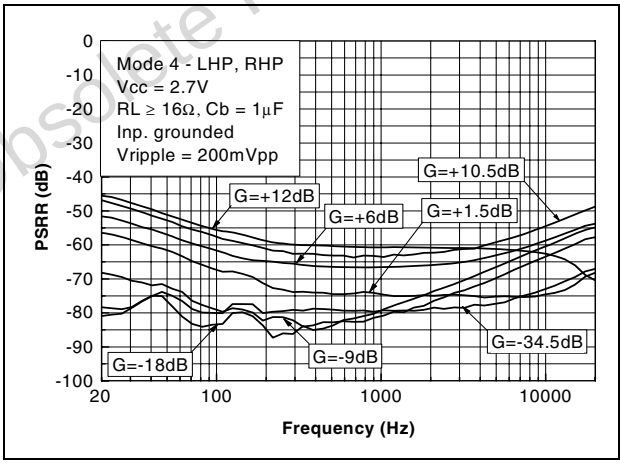


Figure 63. PSRR vs. frequency

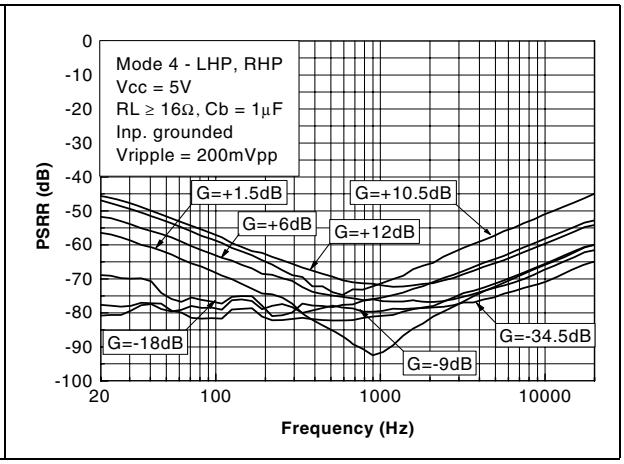


Figure 64. PSRR vs. frequency

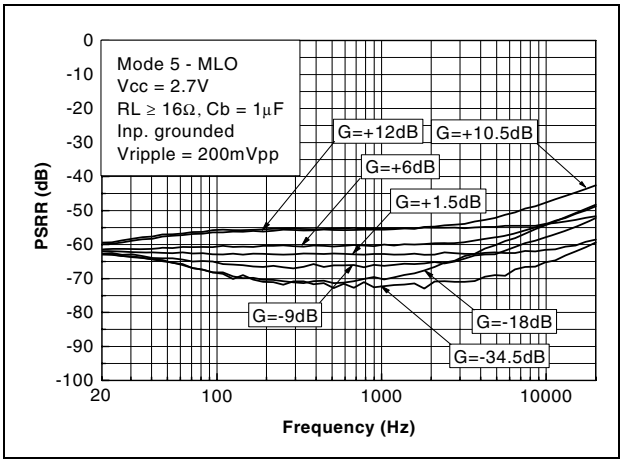


Figure 65. PSRR vs. frequency

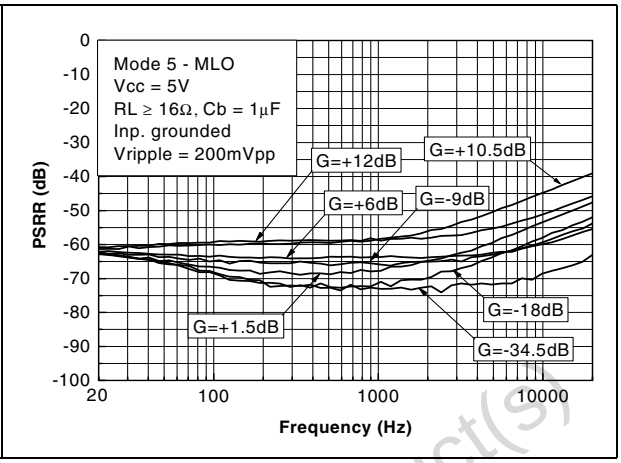


Figure 66. PSRR vs. frequency

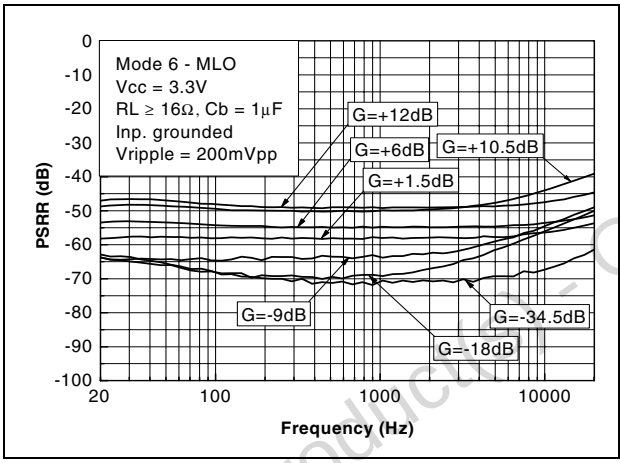


Figure 67. PSRR vs. frequency

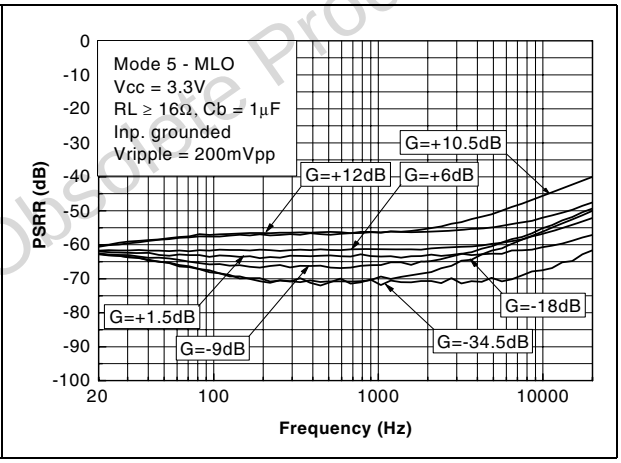


Figure 68. PSRR vs. frequency

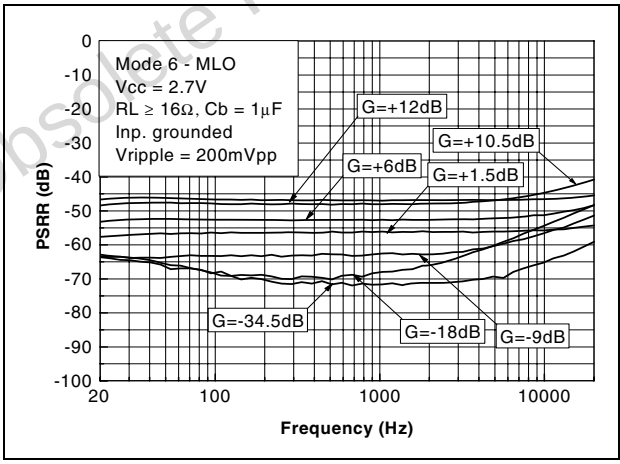


Figure 69. PSRR vs. frequency

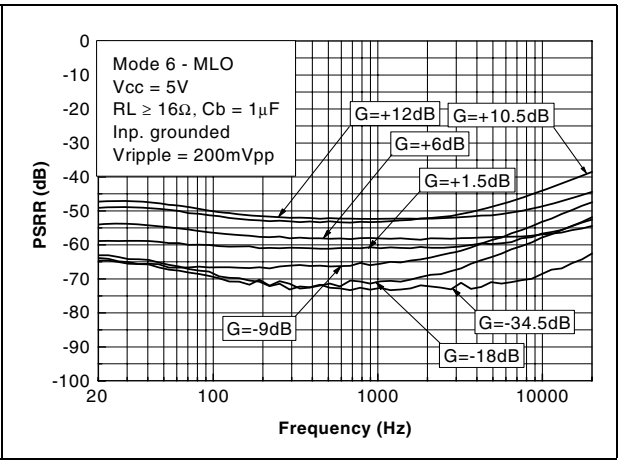


Figure 70. PSRR vs. frequency

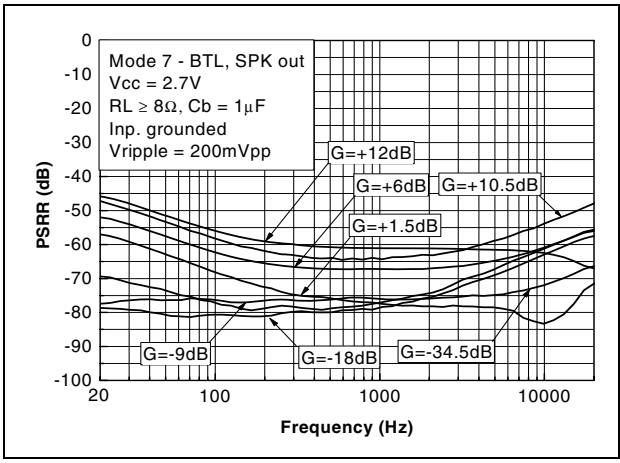


Figure 71. PSRR vs. frequency

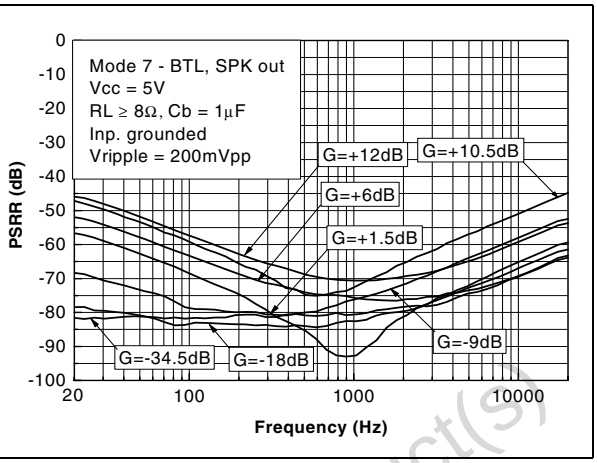


Figure 72. PSRR vs. frequency

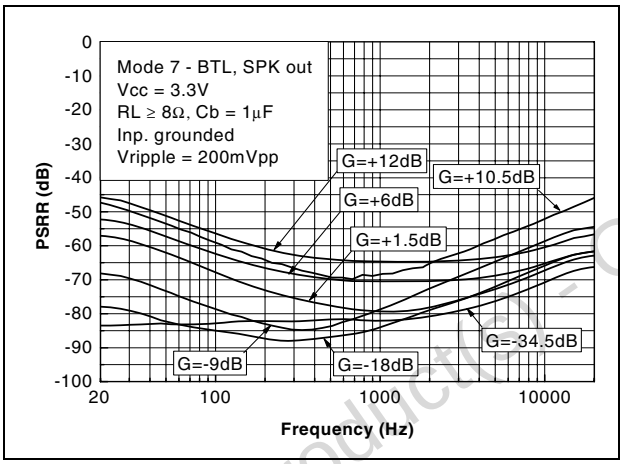


Figure 73. CMRR vs. frequency

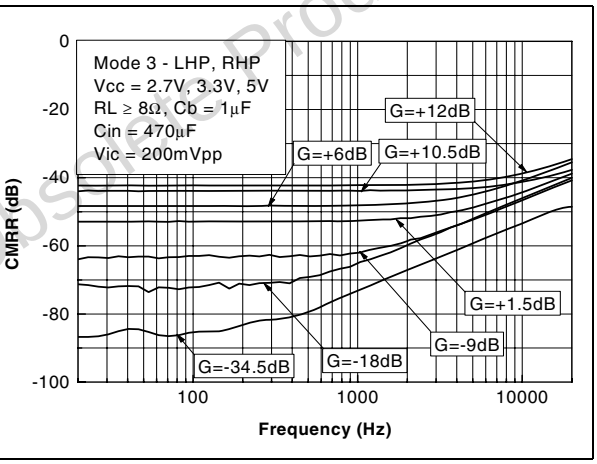


Figure 74. CMRR vs. frequency

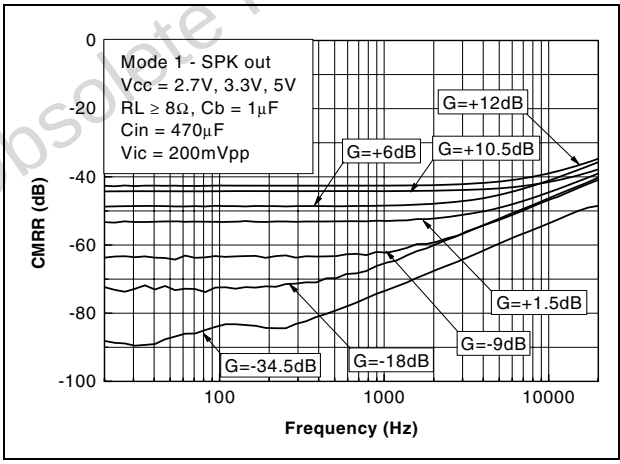


Figure 75. CMRR vs. frequency

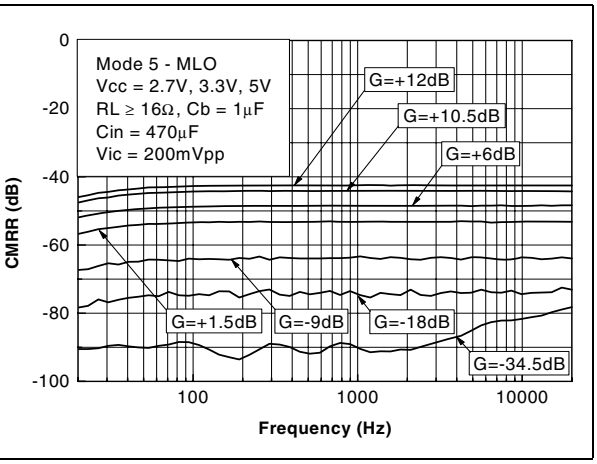


Figure 76. SNR vs. power supply voltage

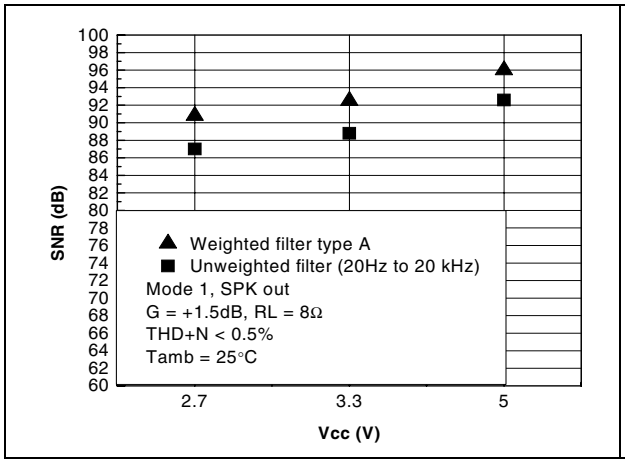


Figure 77. SNR vs. power supply voltage

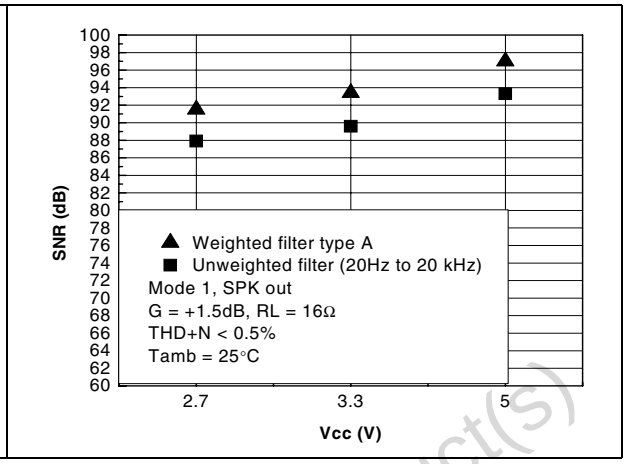


Figure 78. SNR vs. power supply voltage

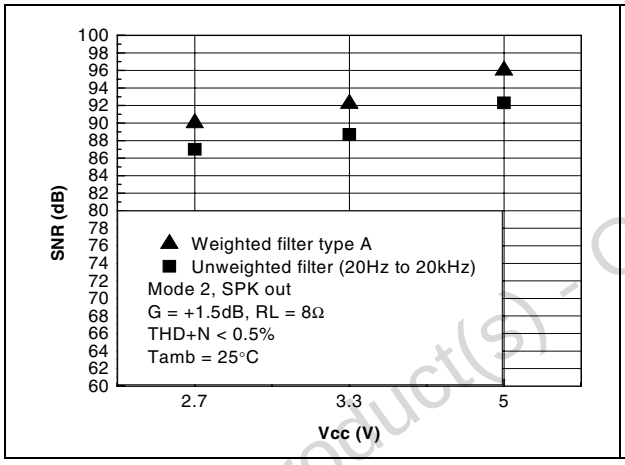


Figure 79. SNR vs. power supply voltage

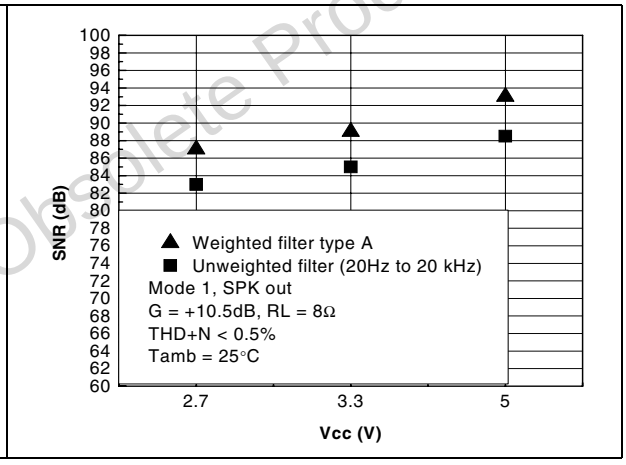


Figure 80. SNR vs. power supply voltage

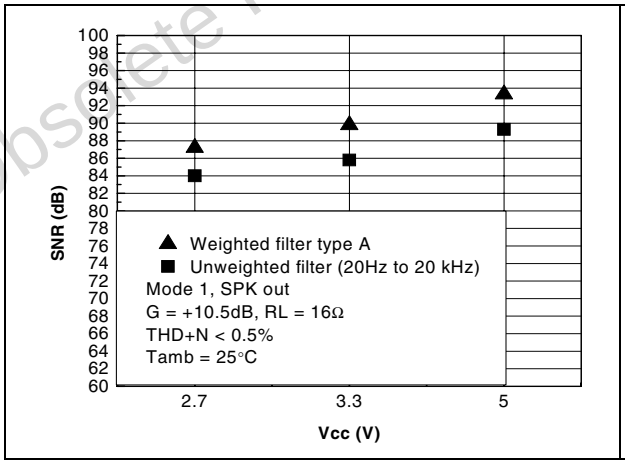


Figure 81. SNR vs. power supply voltage

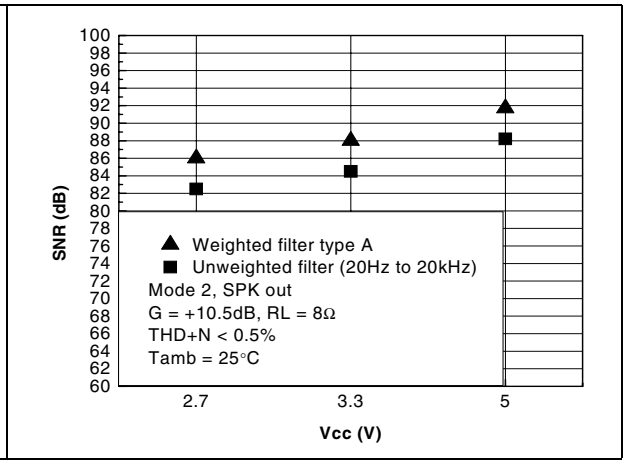


Figure 82. SNR vs. power supply voltage

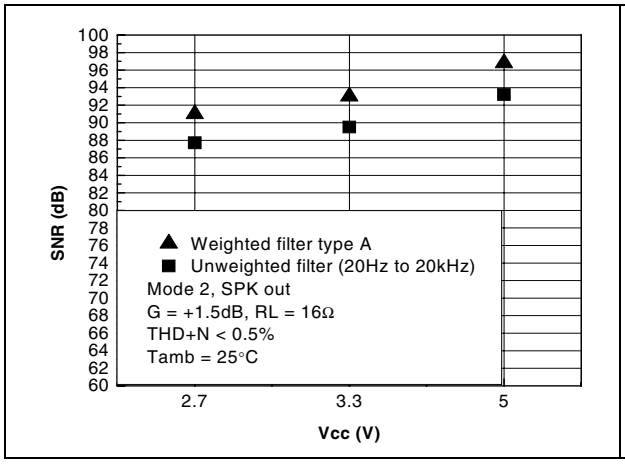


Figure 83. SNR vs. power supply voltage

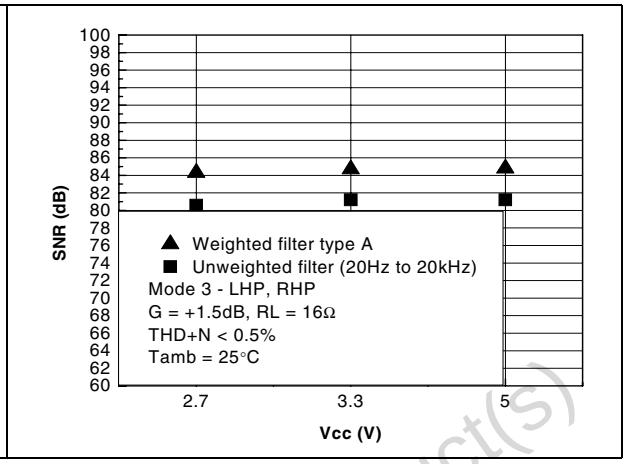


Figure 84. SNR vs. power supply voltage

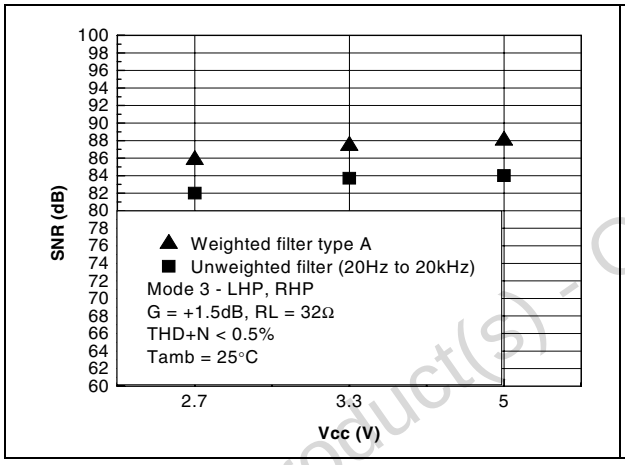


Figure 85. SNR vs. power supply voltage

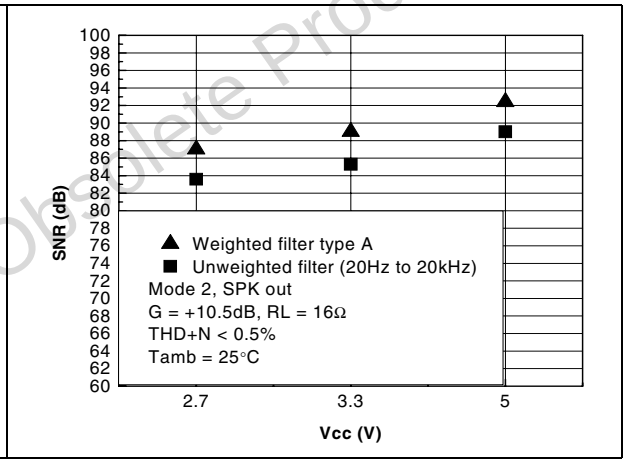


Figure 86. SNR vs. power supply voltage

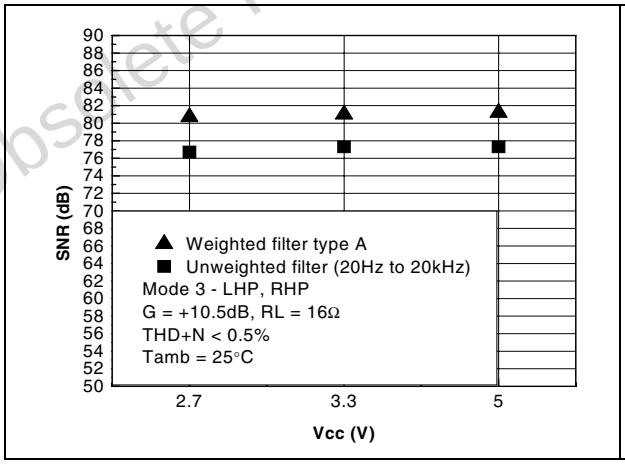


Figure 87. SNR vs. power supply voltage

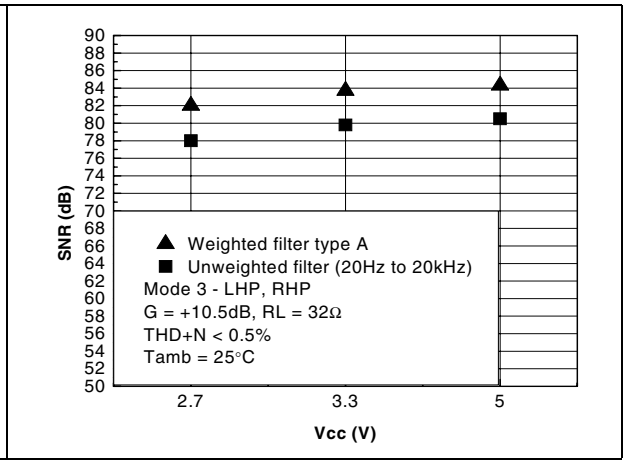


Figure 88. SNR vs. power supply voltage

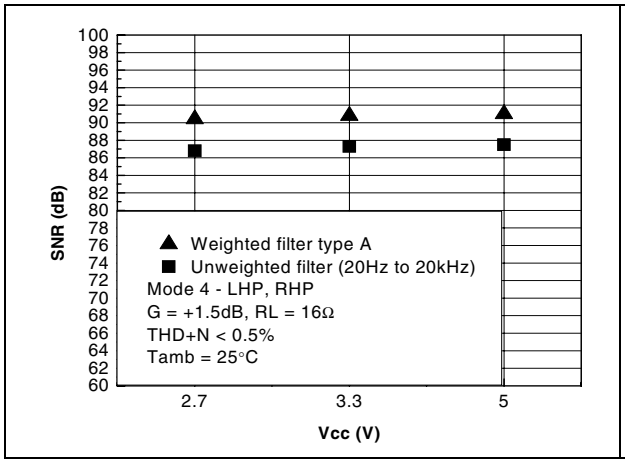


Figure 89. SNR vs. power supply voltage

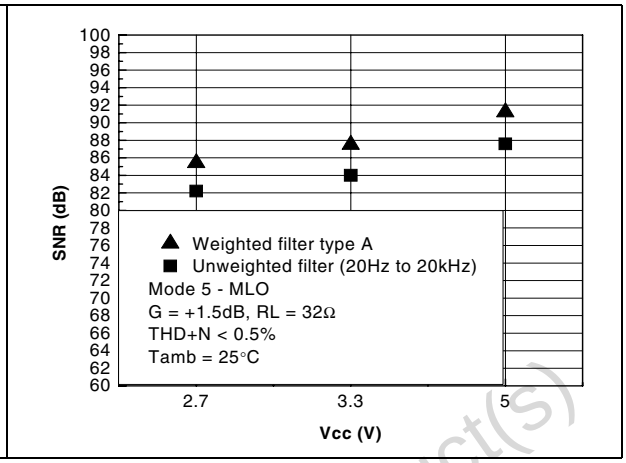


Figure 90. SNR vs. power supply voltage

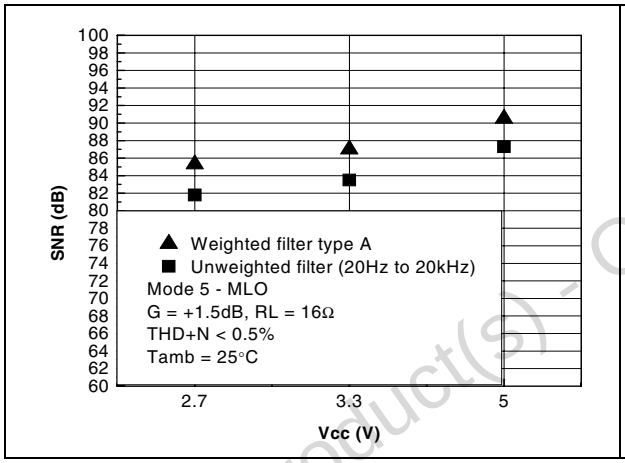


Figure 91. SNR vs. power supply voltage

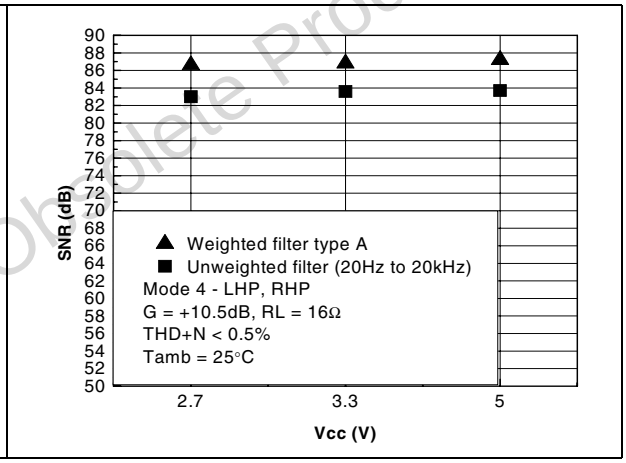


Figure 92. SNR vs. power supply voltage

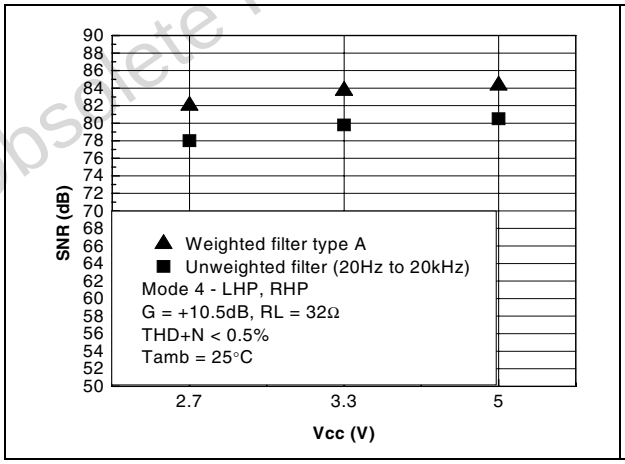


Figure 93. SNR vs. power supply voltage

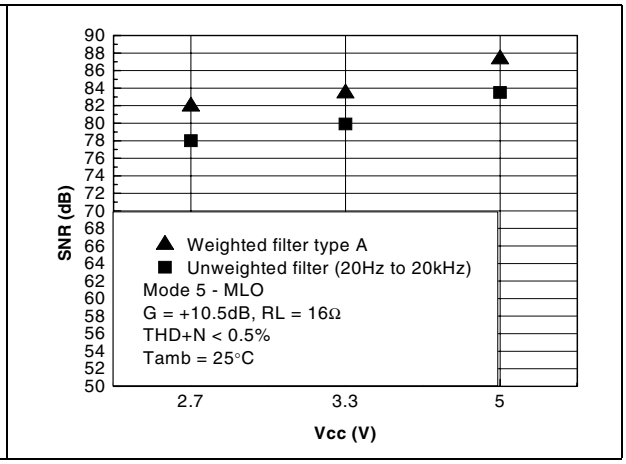


Figure 94. SNR vs. power supply voltage

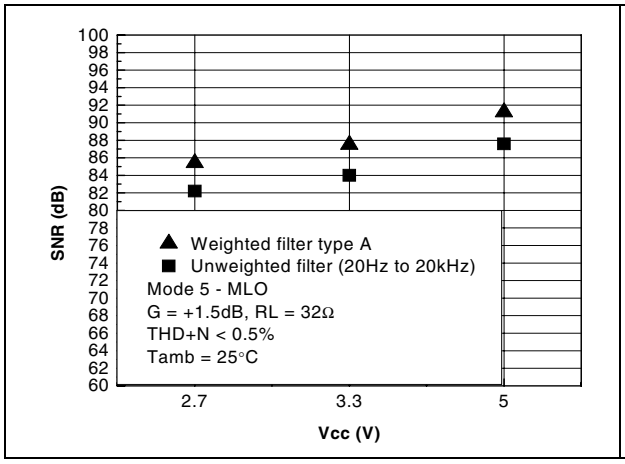


Figure 95. SNR vs. power supply voltage

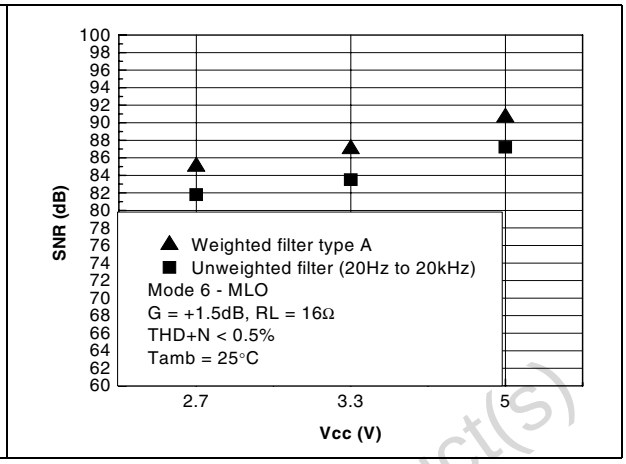


Figure 96. SNR vs. power supply voltage

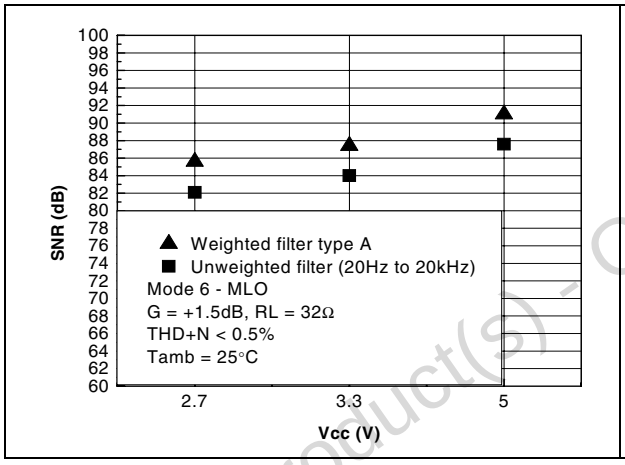


Figure 97. SNR vs. power supply voltage

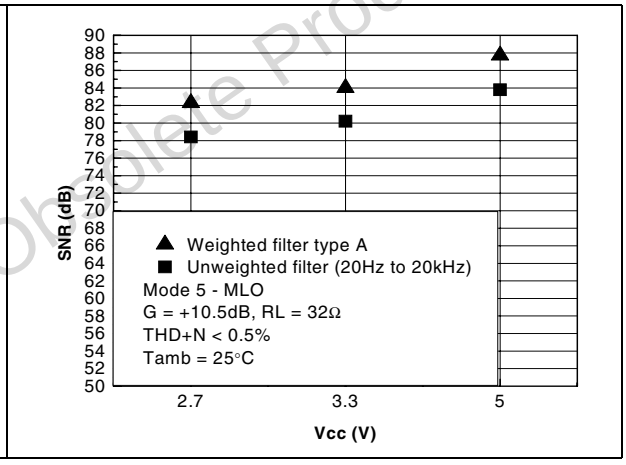


Figure 98. SNR vs. power supply voltage

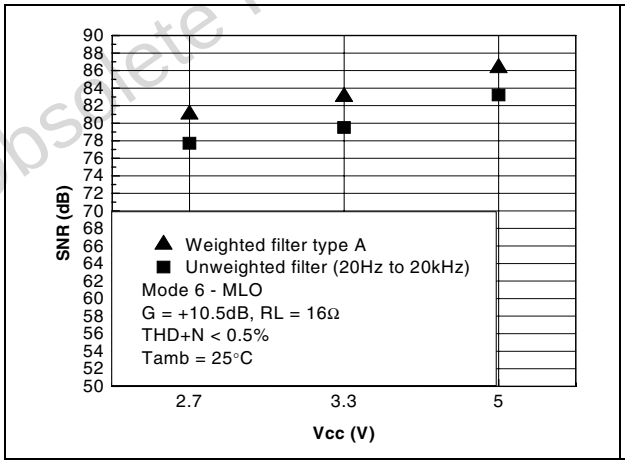


Figure 99. SNR vs. power supply voltage

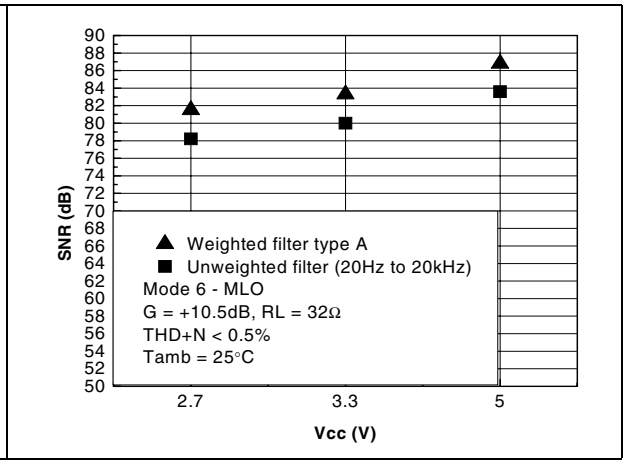


Figure 100. SNR vs. power supply voltage

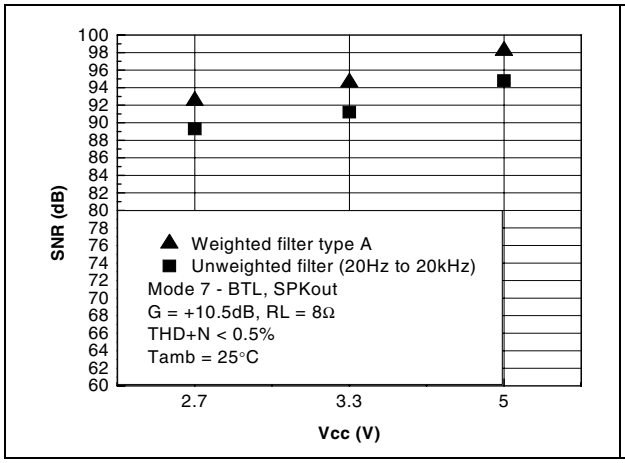


Figure 101. SNR vs. power supply voltage

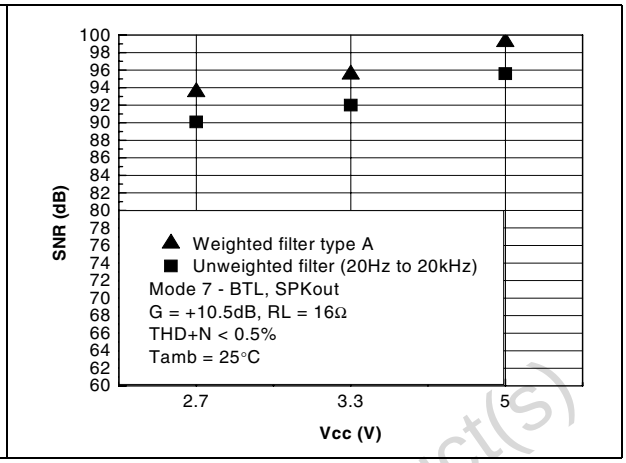


Figure 102. Current consumption vs. power supply voltage

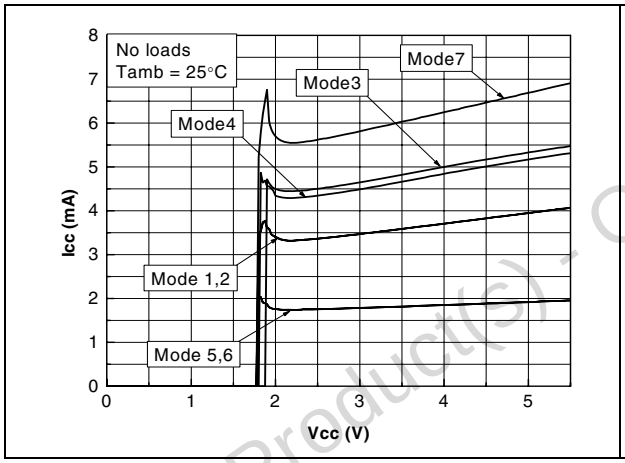


Figure 103. Frequency response modes 1, 2, 7

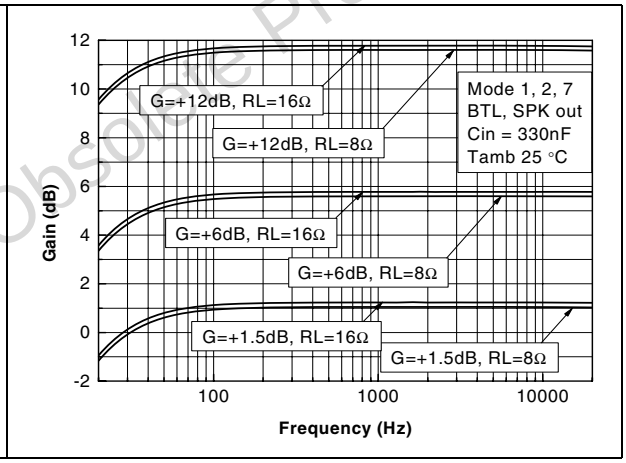


Figure 104. Frequency response modes 3, 4

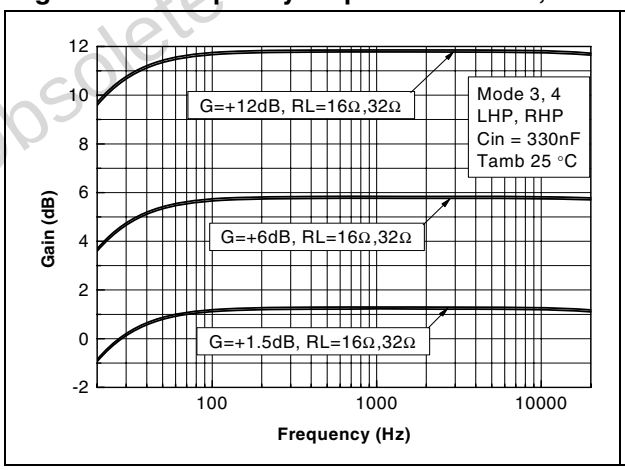


Figure 105. Frequency response modes 5, 6

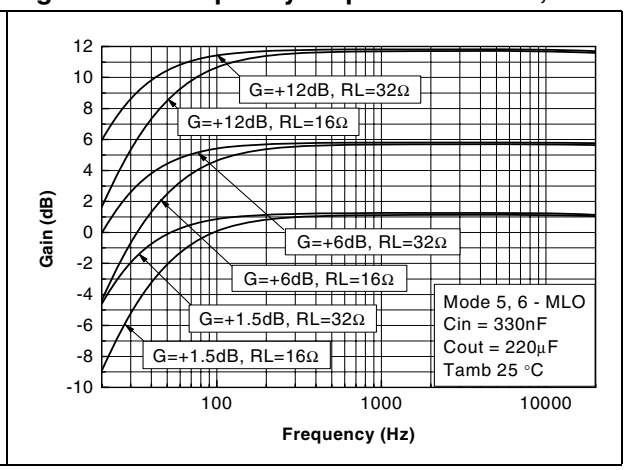


Figure 106. Frequency response modes 5, 6

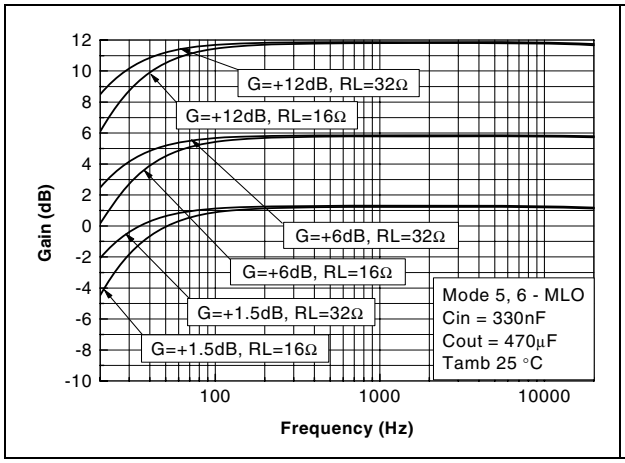


Figure 107. Standby current consumption vs. power supply voltage

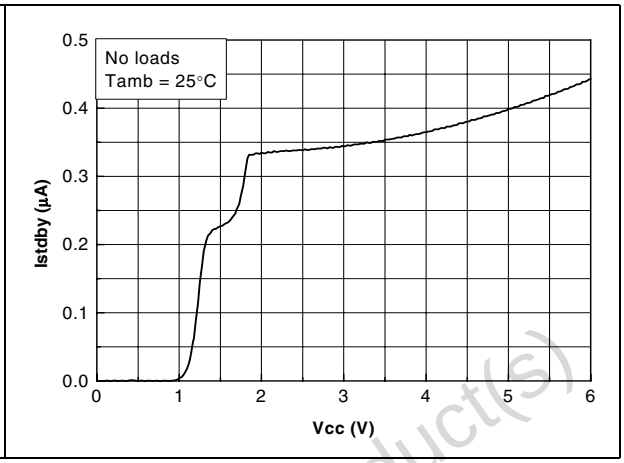


Figure 108. Power dissipation vs. output power (per channel)

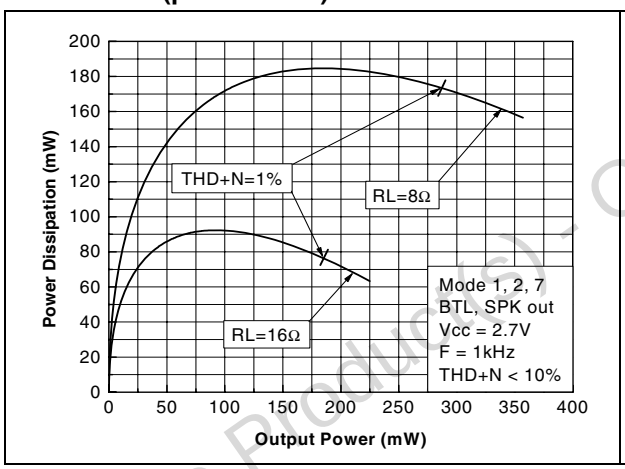


Figure 109. Power dissipation vs. output power (per channel)

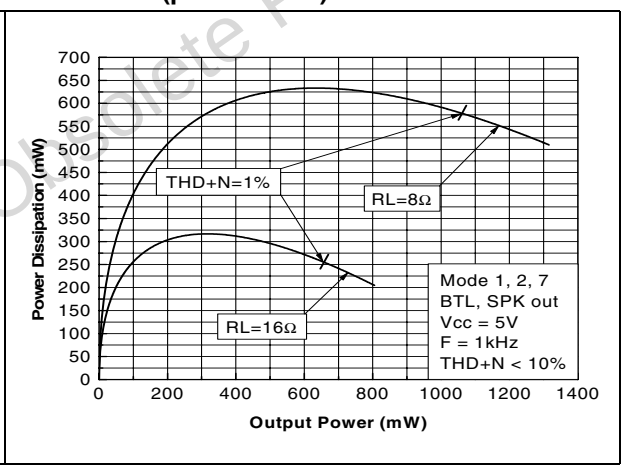


Figure 110. Power dissipation vs. output power (per channel)

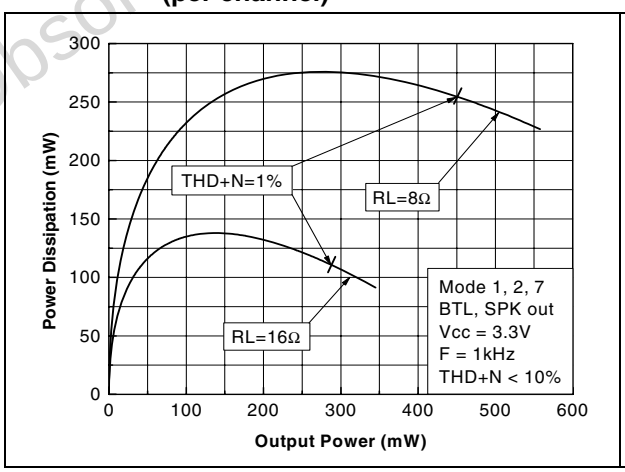


Figure 111. Power dissipation vs. output power (per channel)

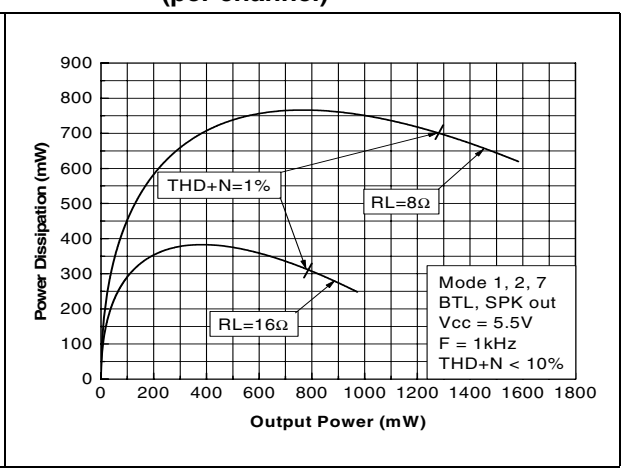


Figure 112. Power dissipation vs. output power (per channel)

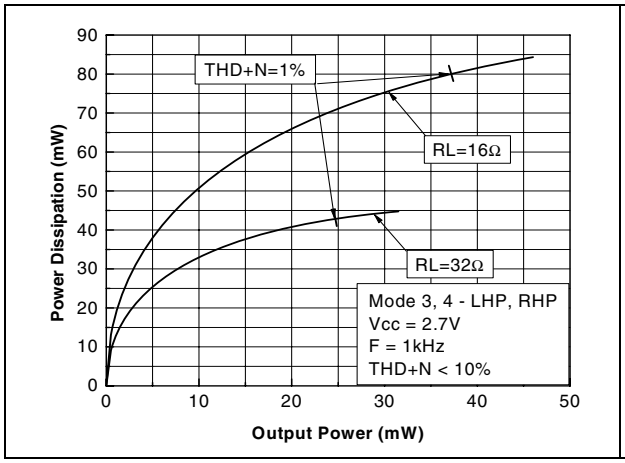


Figure 113. Power dissipation vs. output power (per channel)

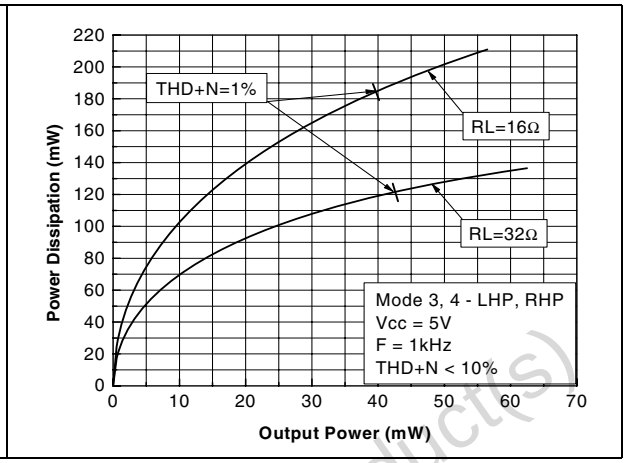


Figure 114. Power dissipation vs. output power (per channel)

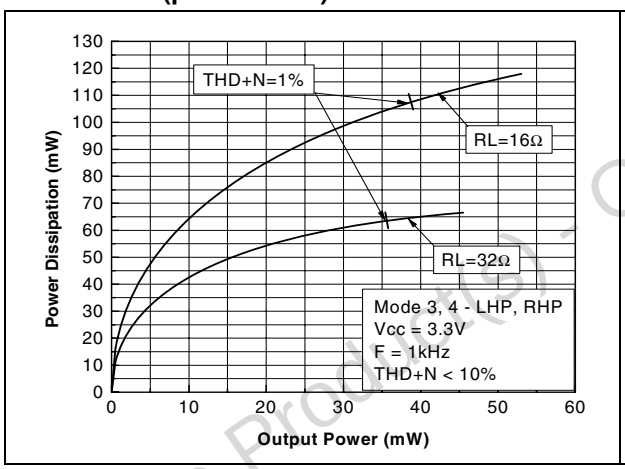


Figure 115. Power dissipation vs. output power (per channel)

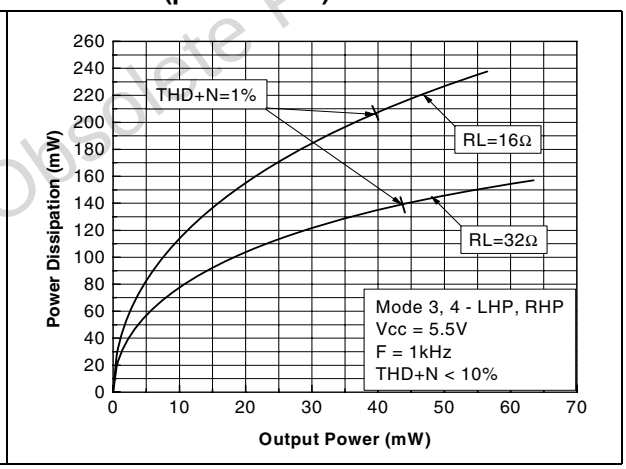


Figure 116. Power dissipation vs. output power

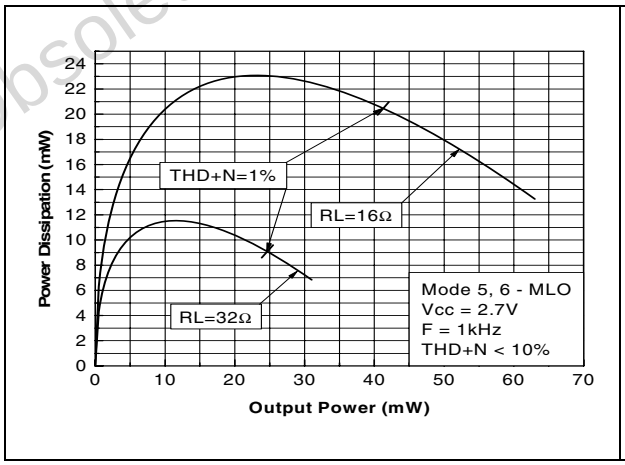


Figure 117. Power dissipation vs. output power

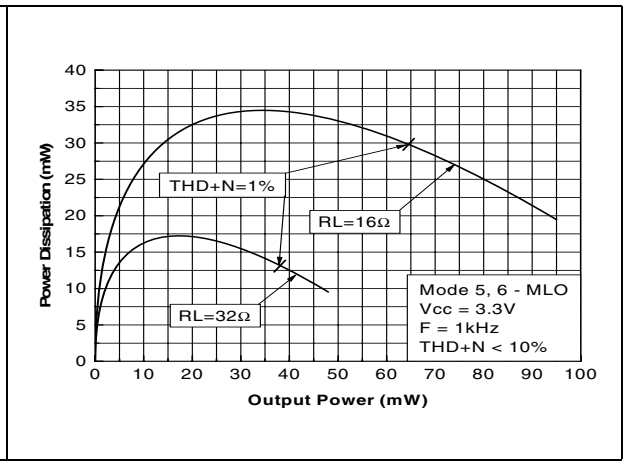


Figure 118. Power dissipation vs. output power

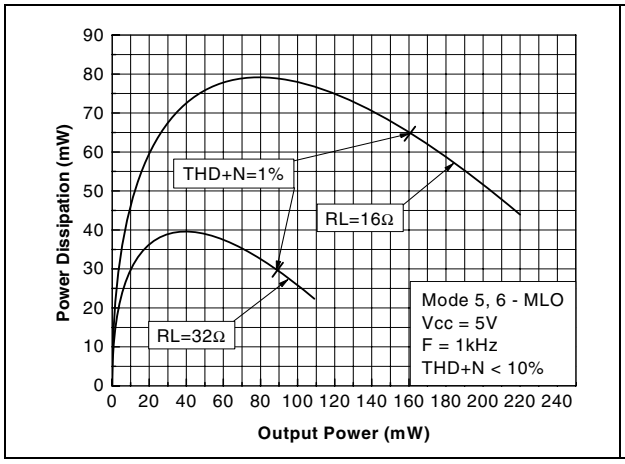


Figure 119. Power dissipation vs. output power

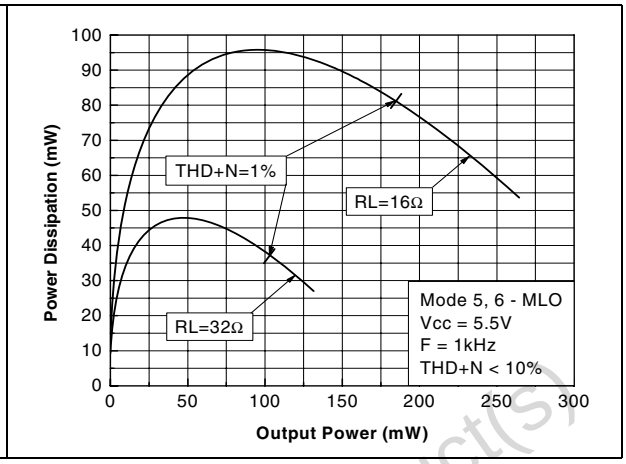


Figure 120. Power derating curves

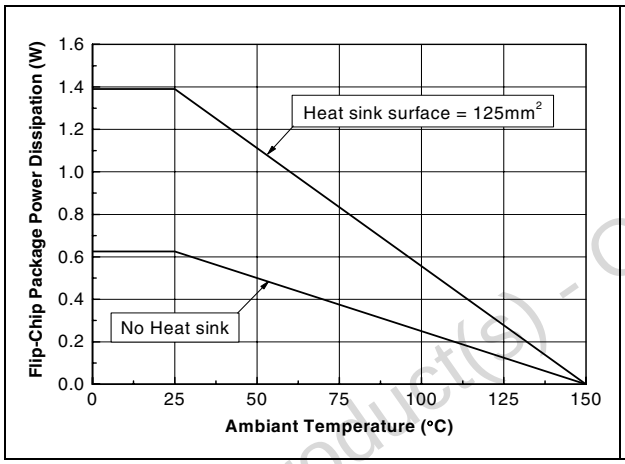


Figure 121. Crosstalk vs. frequency

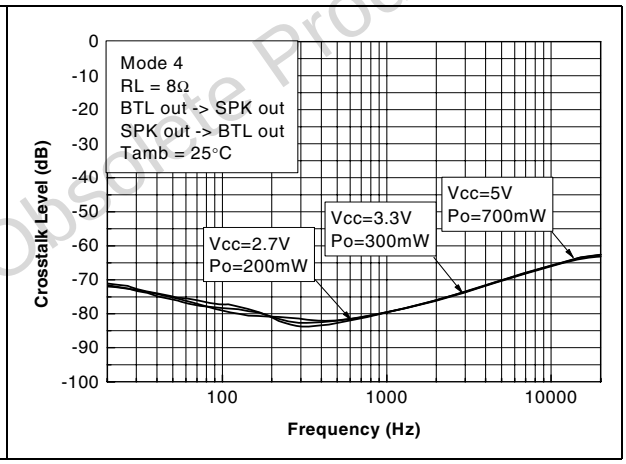
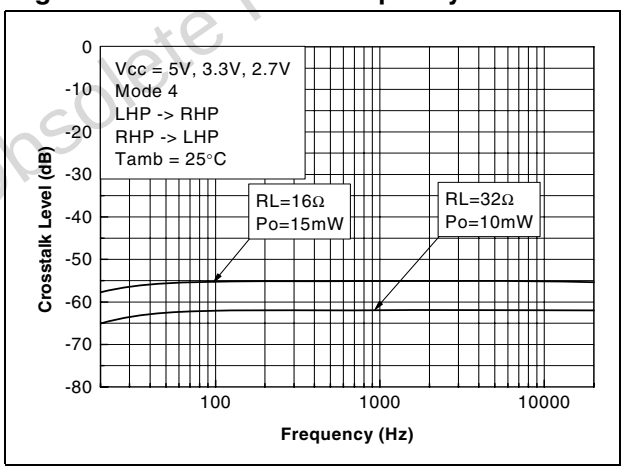


Figure 122. Crosstalk vs. frequency



4 Application information

The TS4956 integrates four monolithic power amplifiers and has one differential input and two single-ended inputs. The output amplifiers can be configured in 7 different modes as one SE (single-ended) capacitively-coupled output, two phantom ground headphone outputs and two BTL outputs. *Figure 1 on page 5* and *Figure 2 on page 6* show these configuration schemes and *Table 7 on page 8* describes these configurations in different modes.

This chapter gives information on how to configure the TS4956 in an application.

4.1 Output configurations

4.1.1 Shutdown

When the device is in shutdown mode, all of the device's outputs are in a high impedance state.

4.1.2 Single-ended output configuration (modes 5 and 6)

When the device is woken-up via the I²C interface, output amplifier on output MLO is biased to the $V_{CC}/2$ voltage. In this configuration an output capacitor, C_{out}, on the single-ended output is needed to block the $V_{CC}/2$ voltage and couples the audio signal to the load.

$V_{CC}/2$ voltage is present on this output in all modes (modes 1 to 7) to keep the output capacitor C_{out} charged and to improve pop performance on this output during the switching between any given mode to mode 5 or 6.

When the device is in mode 5 or 6 where the single-ended output MLO is active, all other outputs are in a high impedance state.

4.1.3 Phantom ground output configuration (modes 3 and 4)

In a phantom ground output configuration (modes 3 and 4) the internal buffer is connected to the PHG pin and biased to the $V_{CC}/2$ voltage. Output amplifiers (pins LHP and RHP) are also biased to the $V_{CC}/2$ voltage. One end of the load is connected to output amplifier and one to the PHG buffer. Therefore, no output capacitors are needed. The advantage of the PHG output configuration is that there are fewer external components compared to an SE configuration. However, note that in this configuration, the device has a higher power dissipation (see *Section 4.3: Power dissipation and efficiency on page 40*).

All other inactive outputs are in the high impedance state except for the MLO output, which is biased to $V_{CC}/2$ voltage.

To achieve better crosstalk results in this case, each speaker should be connected with a separate PHG wire (two speakers connected with four wires) as shown in *Figure 1 on page 5* (instead of using only one common PHG wire for both speakers, that is, two speakers connected with three wires).

4.1.4 BTL output configuration (modes 1, 2, 7)

In a BTL (bridge tied load) output configuration (modes 1, 2 and 4), active outputs are biased to the $V_{CC}/2$ voltage. All other inactive outputs are in the high impedance state except for the MLO output, which is biased to $V_{CC}/2$ voltage.

BTL means that each end of the load is connected to two single-ended output amplifiers.

Therefore we have:

single-ended output 1 = $V_{out1} = V_{out}$ (V)

single-ended output 2 = $V_{out2} = -V_{out}$ (V)

and

$V_{out1} - V_{out2} = 2V_{out}$ (V)

For the same power supply voltage, the output voltage amplitude is twice as high as the output voltage in the single-ended or phantom ground configurations and the output power is four times higher than the output power in the single-ended or phantom ground configurations.

4.2 Power limitation in the phantom ground configuration

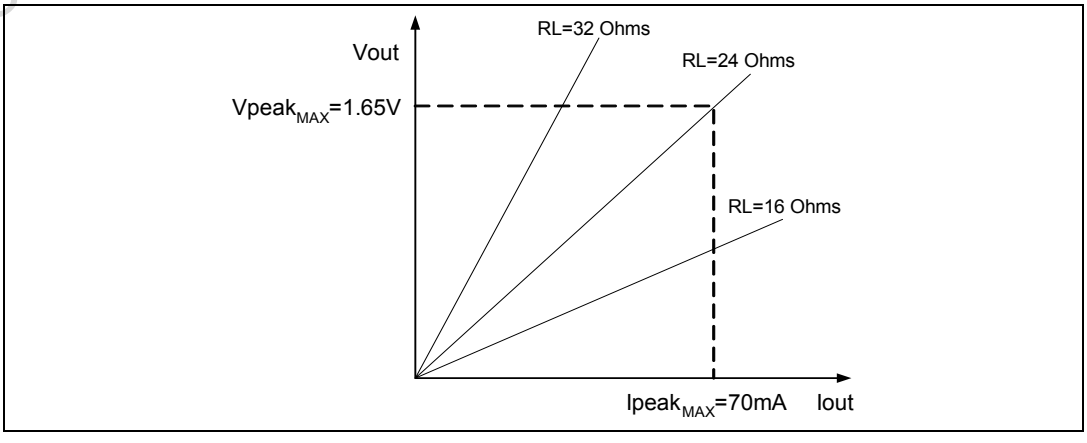
A power limitation is imposed on the headphones in mode 3 and 4. Limitation of output power is achieved by limiting the output voltage and output current on each amplifier.

The maximum value of the output voltage, $V_{out\ max}$, is set to a value of 1.65 V in order to reach a maximum output power of the sinusoidal signal of around 40 mW per channel with a 32 Ω load resistance and THD+N<1%.

The maximum value of output current $I_{out\ max}$ is set to value 70 mA in order to reach a maximum output power of the sinusoidal signal of around 40 mW per channel with a 16 Ω load resistance and THD+N<1%. *Figure 48 on page 25* shows the functionality of the power limitation with different load resistances.

The maximum output power with these voltage and current limitations is reached with load values above 16 Ω and below 32 Ω as explained by *Figure 123*.

Figure 123. Voltage and current limitation on headphones



4.3 Power dissipation and efficiency

Hypotheses:

- The voltage and current in the load are sinusoidal (V_{out} and I_{out}).
- The supply voltage is a pure DC source (V_{CC}).

Regarding the load we have:

$$V_{out} = V_{PEAK}\sin\omega t(V)$$

and

$$I_{out} = \frac{V_{out}}{R_L}(A)$$

and

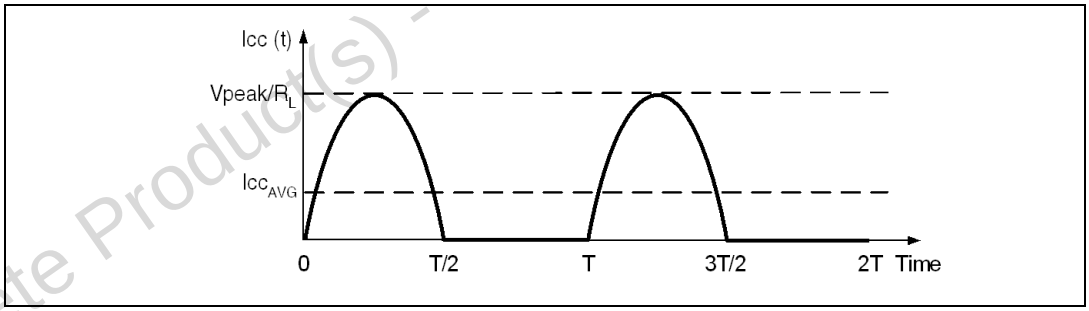
$$P_{out} = \frac{V_{PEAK}^2}{2R_L}(A)$$

4.3.1 Single-ended output configuration (modes 5 and 6)

The average current delivered by the supply voltage is:

$$cc_{AVG} = \frac{1}{2\pi}\int_0^{\pi}\frac{V_{PEAK}}{R_L}\sin(t)dt = \frac{V_{PEAK}}{\pi R_L}(A)$$

Figure 124. Current delivered by supply voltage in a single-ended output configuration



The power delivered by the supply voltage is:

$$P_{supply} = V_{CC}I_{CC_{AVG}}(W)$$

Therefore, the **power dissipation by the single-ended amplifier** is

$$P_{diss} = P_{supply} - P_{out}(W)$$

$$P_{diss} = \frac{\sqrt{2}V_{CC}}{\pi\sqrt{R_L}}\sqrt{P_{out}} - P_{out}(W)$$

and the maximum value is obtained when:

$$\frac{\partial P_{diss}}{\partial P_{out}} = 0$$

and its value is:

$$P_{diss_{MAX}} = \frac{V_{CC}^2}{\pi^2 R_L}(W)$$

Note: This maximum value depends only on the power supply voltage and load values.

The **efficiency** is the ratio between the output power and the power supply:

$$\eta = \frac{P_{out}}{P_{supply}} = \frac{\pi V_{PEAK}}{2V_{CC}}$$

The maximum theoretical value is reached when $V_{PEAK} = V_{CC}/2$, so

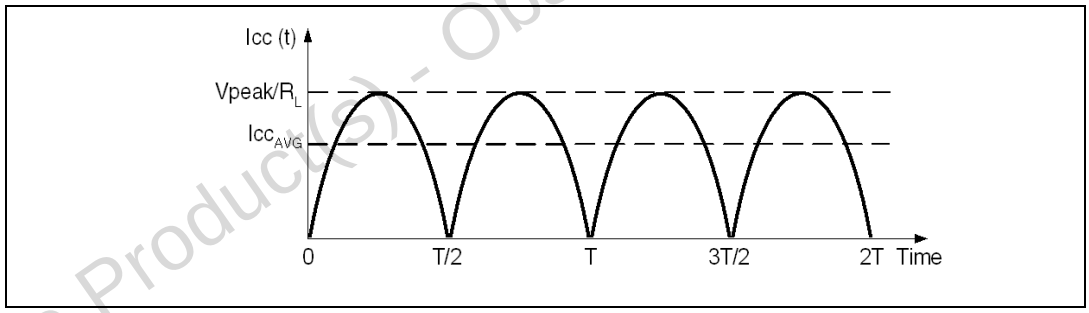
$$\eta = \frac{\pi}{4} = 78.5\%$$

4.3.2 Phantom ground output configuration (modes 3, 4):

The average current delivered by the supply voltage is:

$$Icc_{AVG} = \frac{1}{\pi}\int_0^{\pi} \frac{V_{PEAK}}{R_L}\sin(t)dt = \frac{2V_{PEAK}}{\pi R_L}(A)$$

Figure 125. Current delivered by supply voltage in a phantom ground output configuration



The power delivered by the supply voltage is:

$$P_{supply} = V_{CC}Icc_{AVG}(W)$$

Then, the power dissipation by each amplifier is

$$P_{diss} = \left(\frac{2\sqrt{2}V_{CC}}{\pi\sqrt{R_L}}\sqrt{P_{out}}\right) - P_{out}(W)$$

and the maximum value is obtained when:

$$\frac{\partial P_{diss}}{\partial P_{out}} = 0$$

and its value is:

$$P_{diss_{MAX}} = \frac{2V_{CC}^2}{\pi^2 R_L}(W)$$

Note: This maximum value depends only on the power supply voltage and load values.

The efficiency is the ratio between the output power and the power supply.

$$\eta = \frac{P_{out}}{P_{supply}} = \frac{\pi V_{PEAK}}{4V_{CC}}$$

The maximum theoretical value is reached when $\mathbf{V_{PEAK} = V_{CC}/2}$, so

$$\eta = \frac{\pi}{8} = 39.25\%$$

In modes 3 and 4, the TS4956 has two active output power amplifiers. Each amplifier produces heat due to its power dissipation. Therefore the maximum die temperature is the sum of each amplifier's maximum power dissipation. It is calculated as follows.

$P_{diss\ 1}$ = power dissipation due to the first power amplifier.

$P_{diss\ 2}$ = power dissipation due to the second power amplifier.

$Total\ P_{diss} = P_{diss\ 1} + P_{diss\ 2}$ (W)

In most cases, $P_{diss\ 1} = P_{diss\ 2}$, giving:

$$TotalP_{diss} = 2P_{diss1}$$

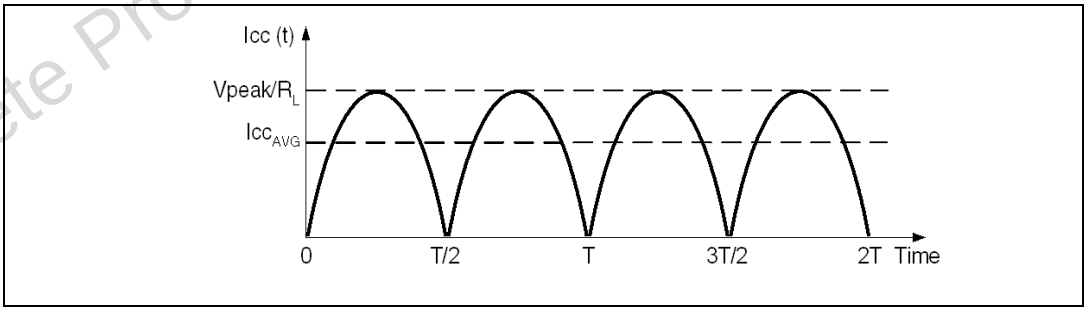
$$TotalP_{diss} = \frac{4\sqrt{2}V_{CC}}{\pi\sqrt{R_L}}\sqrt{P_{out}} - 2P_{out}(W)$$

4.3.3 BTL output configuration (modes 1, 2, 7)

The average current delivered by the supply voltage is:

$$Icc_{AVG} = \frac{1}{\pi}\int_0^{\pi} \frac{V_{PEAK}}{R_L}\sin(t)dt = \frac{2V_{PEAK}}{\pi R_L}(A)$$

Figure 126. Current delivered by supply voltage in a BTL output configuration



The power delivered by the supply voltage is:

$$P_{supply} = V_{CC}Icc_{AVG}(W)$$

Then, the power dissipation by each amplifier is:

$$P_{diss} = \frac{2\sqrt{2}V_{CC}}{\pi\sqrt{R_L}}\sqrt{P_{out}} - P_{out}(W)$$

and the maximum value is obtained when:

$$\frac{\partial P_{diss}}{\partial P_{out}} = 0$$

and its value is:

$$P_{diss_{MAX}} = \frac{2V_{CC}^2}{\pi^2 R_L}(W)$$

Note: This maximum value depends only on the power supply voltage and load values.

The efficiency is the ratio between the output power and the power supply.

$$\eta = \frac{P_{out}}{P_{supply}} = \frac{\pi V_{PEAK}}{4V_{CC}}$$

The maximum theoretical value is reached when $V_{PEAK} = V_{CC}$, so

$$\eta = \frac{\pi}{4} = 78.5\%$$

The TS4956 has one active output BTL power amplifier when in modes 1 and 2. In mode 7, the TS49656 has two active output BTL power amplifiers.

Each amplifier produces heat due to its power dissipation. Therefore the maximum die temperature is the sum of each amplifier's maximum power dissipation. It is calculated as follows.

- $P_{diss\ 1}$ = power dissipation due to the first BTL power amplifier.
- $P_{diss\ 2}$ = power dissipation due to the second BTL power amplifier.
- *Total* $P_{diss} = P_{diss\ 1} + P_{diss\ 2}$ (W)

In most cases, $P_{diss\ 1} = P_{diss\ 2}$, giving:

$$TotalP_{diss} = 2P_{diss1}$$

$$TotalP_{diss} = \frac{4\sqrt{2}V_{CC}}{\pi\sqrt{R_L}}\sqrt{P_{out}} - 2P_{out} \quad (W)$$

4.4 Low frequency response

4.4.1 Input capacitor C_{in}

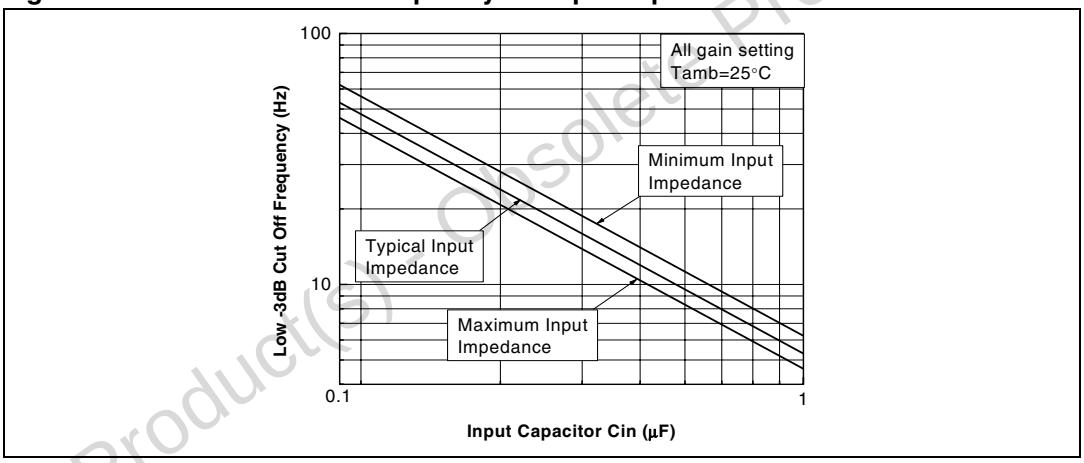
The input coupling capacitor blocks the DC part of the input signal at the amplifier input. In the low-frequency region, C_{in} starts to have an effect. C_{in} with Z_{in} forms a first-order, high-pass filter with -3 dB cut-off frequency.

$$F_{CL} = \frac{1}{2\pi Z_{in} C_{in}} \quad (Hz)$$

Z_{in} is the input impedance of the corresponding input.

Note: For all inputs, the impedance value remains constant for all gain settings. This means that the lower cut-off frequency does not change with the gain setting. Note also that 30 kΩ is a typical value and there is tolerance around this value. Using Figure 127 you can easily establish the C_{in} value required for a -3 dB cut-off frequency.

Figure 127. 3dB lower cutoff frequency vs. input capacitance



4.4.2 Output capacitor C_{out}

In the single-ended configuration an external output coupling capacitor, C_{out}, is needed. This coupling capacitor C_{out}, together with the output load R_L, forms a first-order high-pass filter with -3 dB cut off frequency.

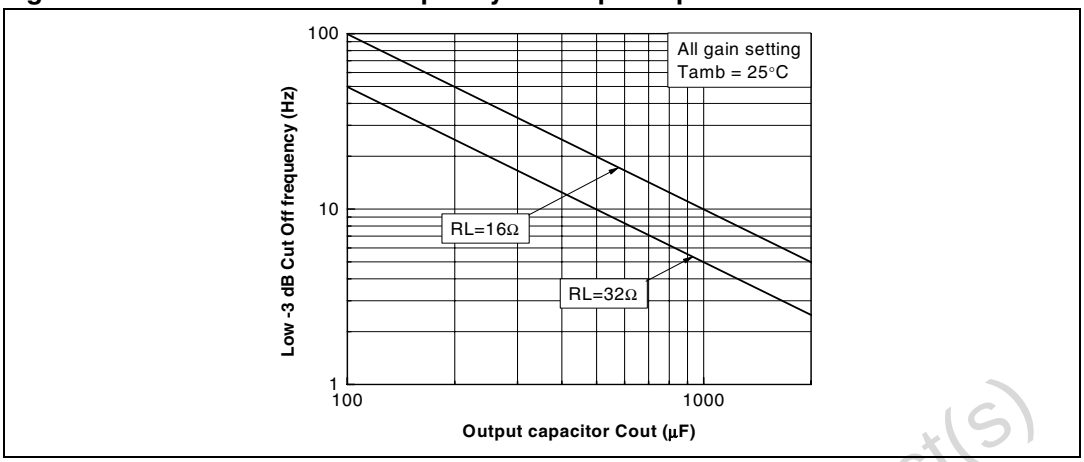
$$F_{CL} = \frac{1}{2\pi R_L C_{out}} (Hz)$$

See *Figure 128* to establish the C_{out} value for a -3 dB cut-off frequency required.

These two first-order filters form a second-order high-pass filter. The -3 dB cut-off frequency of these two filters should be the same, so the following formula should be respected:

$$\frac{1}{2\pi Z_{in} C_{in}} \cong \frac{1}{2\pi R_L C_{out}}$$

Figure 128. 3dB lower cut off frequency vs. output capacitance

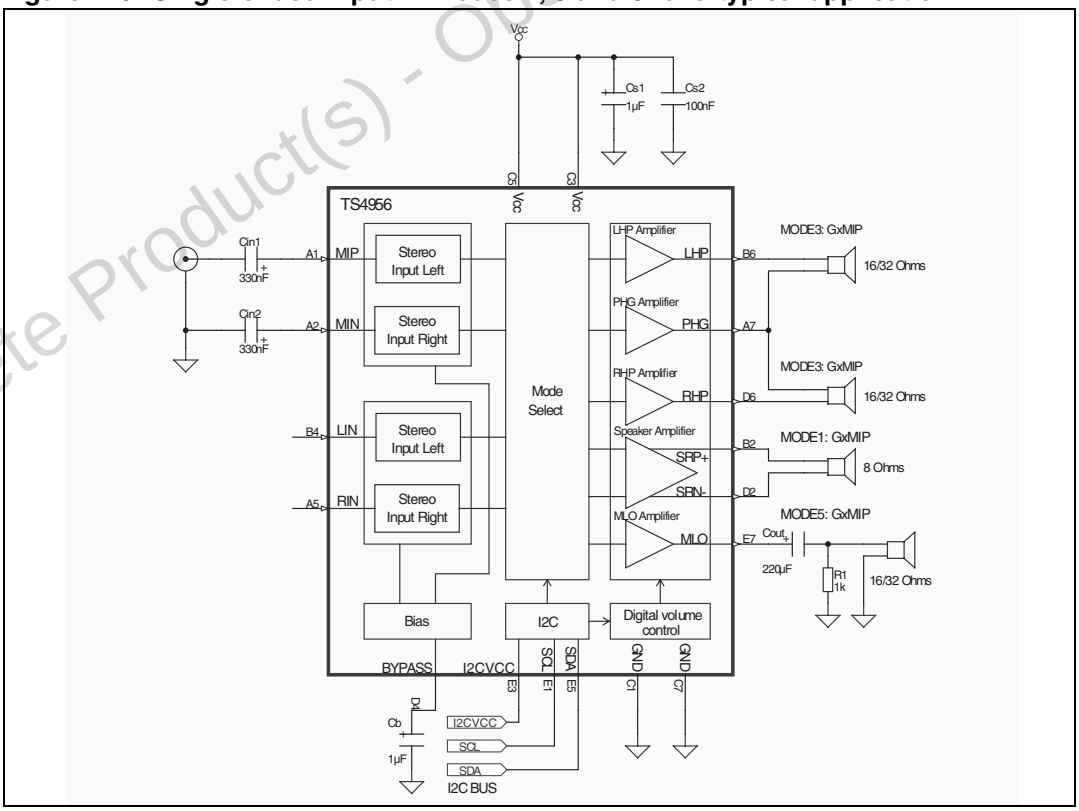


4.5 Single-ended input configuration in modes 1, 3 and 5

It is possible to use the differential inputs MIP and MIN of the TS4956 as one single-ended input in modes where the differential inputs are active (modes 1, 3 and 5).

Figure 129 illustrates this configuration.

Figure 129. Single-ended input in modes 1, 3 and 5 for a typical application



4.6 Decoupling of the circuit

Two capacitors are needed to properly bypass the TS4956 — a power supply capacitor C_s and a bias voltage bypass capacitor C_b.

C_s has a strong influence on the THD+N at high frequencies (above 7 kHz) and indirectly on the power supply disturbances.

With a C_s value of about 1 µF, you can expect to obtain THD+N performances similar to those shown in the datasheet.

If C_s is lower than 1 µF, THD+N increases in high frequency and disturbances on power supply rail are less filtered.

On the contrary, if C_s is higher than 1 µF, disturbances on the power supply rail are more filtered.

C_b has an influence on THD+N at lower frequencies, but its value has critical impact on the final result of PSRR with inputs grounded at lower frequencies:

- If C_b is lower than 1 µF, THD+N increases at lower frequencies and the PSRR worsens upwards.
- If C_b is higher than 1 µF, the benefit on THD+N and PSRR in the lower frequency range is small.

The value of C_b also has an influence on startup time.

4.7 Power-on reset

When power is applied to V_{CC}, an internal power-on reset holds the TS4956 in a reset state (shutdown) until the supply voltage reaches its nominal value. The power-on reset has a typical threshold of 1.75 V.

During this reset state the output configuration is the same as in the shutdown mode.

4.8 PSRR measurements

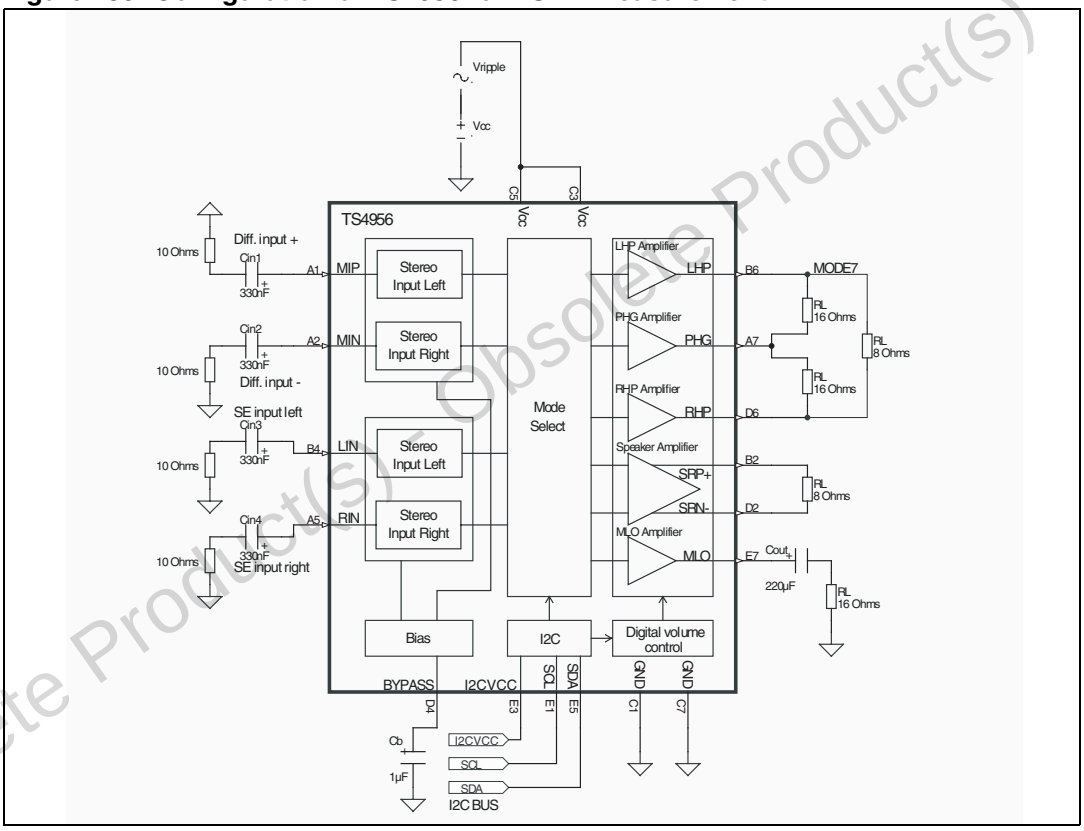
4.8.1 What is PSRR?

The PSRR is the power supply rejection ratio. The PSRR of a device is the ratio between a power supply disturbance and the result on the output. In other words, the PSRR is the ability of a device to minimize the impact of power supply disturbance to the output.

4.8.2 How is PSRR measured?

The PSRR was measured with the TS4956 configured as shown in *Figure 130*.

Figure 130. Configuration of TS4956 for PSRR measurement



Main operating principles of TS4956 for purposes of PSRR measurement

- The DC voltage supply (V_{CC}) is fixed.
- The AC sinusoidal ripple voltage (V_{ripple}) is fixed.
- No bypass capacitor C_s is used.

The PSRR value for each frequency is calculated as:

$$PSRR = 20Log\left[\frac{RMS_{(Output)}}{RMS_{(Vripple)}}\right](dB)$$

RMS is a rms selective measurement.

4.9 Pop and click performance

The TS4956 has an internal pop and click reduction circuitry which eliminates the output transients, such as, for example, during switch-on or switch-off phases, or during a switch from one output mode to another, or when changing the volume. The performance of this circuitry is closely linked to the values of the input capacitor C_{in}, the output capacitor C_{out} (for single-ended configuration) and the bias voltage bypass capacitor C_b.

The values of C_{in} and C_{out} are determined by the lower cut-off frequency value requested. The value of C_b will affect the THD+N and PSRR values at lower frequencies.

The TS4956 is optimized to have low pop and click in the typical schematic configurations (*Figure 1 on page 5* and *Figure 2 on page 6*).

4.10 Thermal shutdown

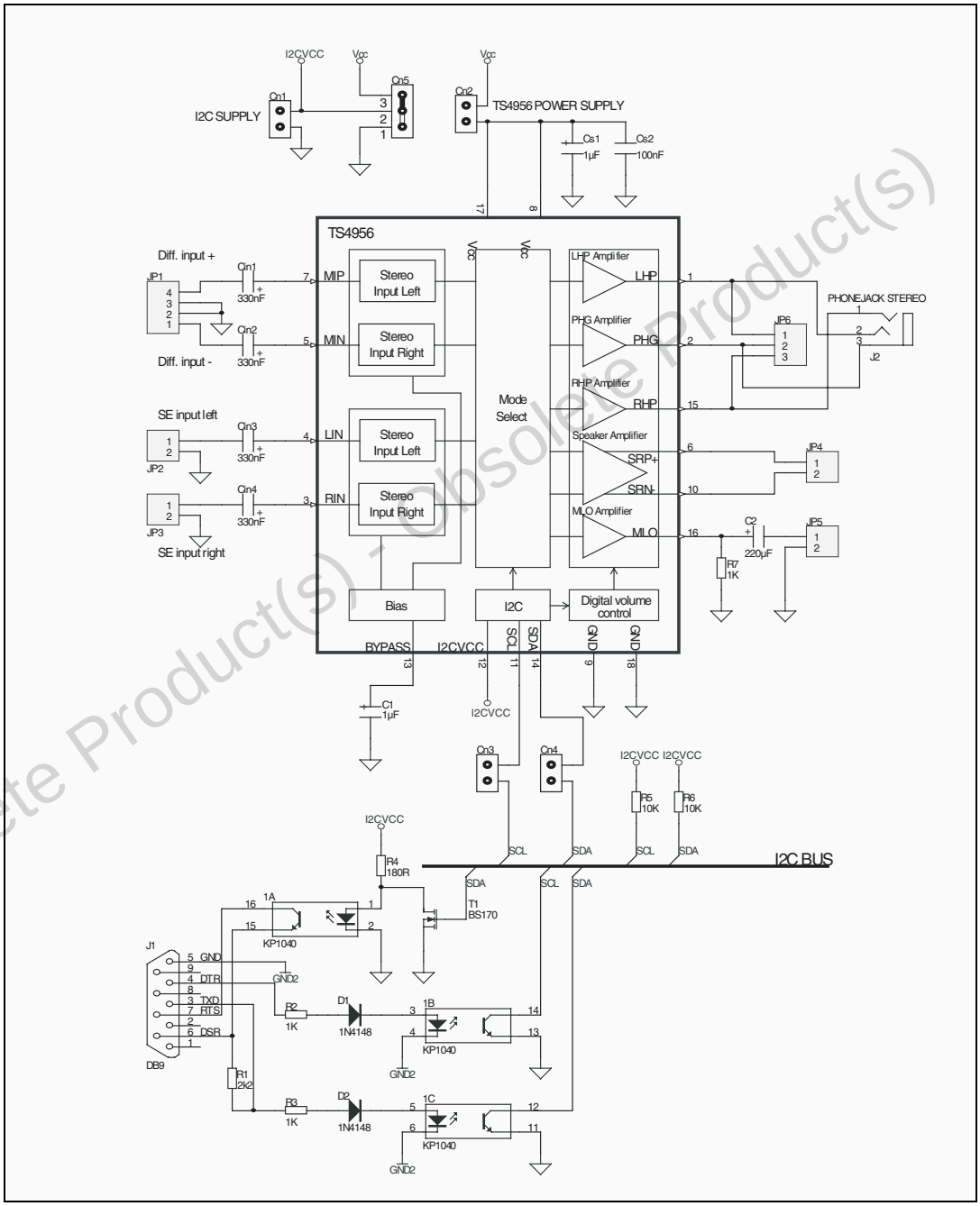
The TS4956 device has an internal thermal shutdown protection in the event of extreme temperatures. Thermal shutdown is active when the device reaches a temperature of 150° C.

4.11 Demonstration board

A demonstration board for the TS4956 is available.

For more information about this demonstration board, refer to the application note *AN2465,* which you can find on **www.st.com.**

Figure 131. Demonstration board schematic for the TS4956

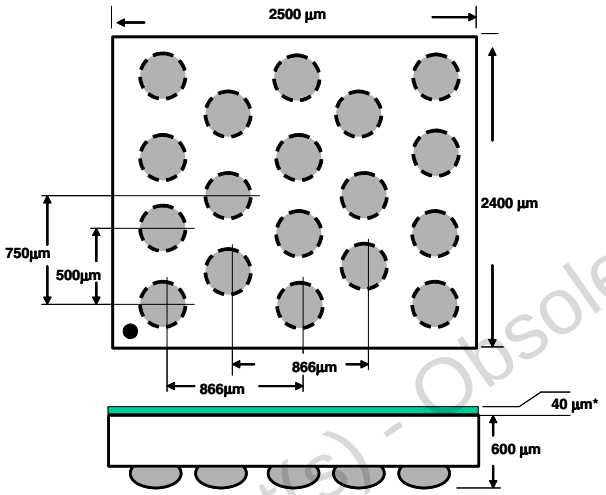


5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

5.1 18-bump flip-chip package

Figure 132. 18-bump flip-chip package



Die size: **2.5 x 2.4 mm** ± 30 µm
Die height (including bumps): **600 µm**
Bumps diameter: **315 µm** ±50 µm
Bump diameter before reflow: **300 µm** ±10 µm
Bumps height: **250 µm** ±40 µm
Die height: **350 µm** ±20 µm
Pitch: **500 µm** ±50 µm
Coplanarity: **50 µm max**
Optional*: back coating height: 40 µm

Figure 133. Footprint recommendations

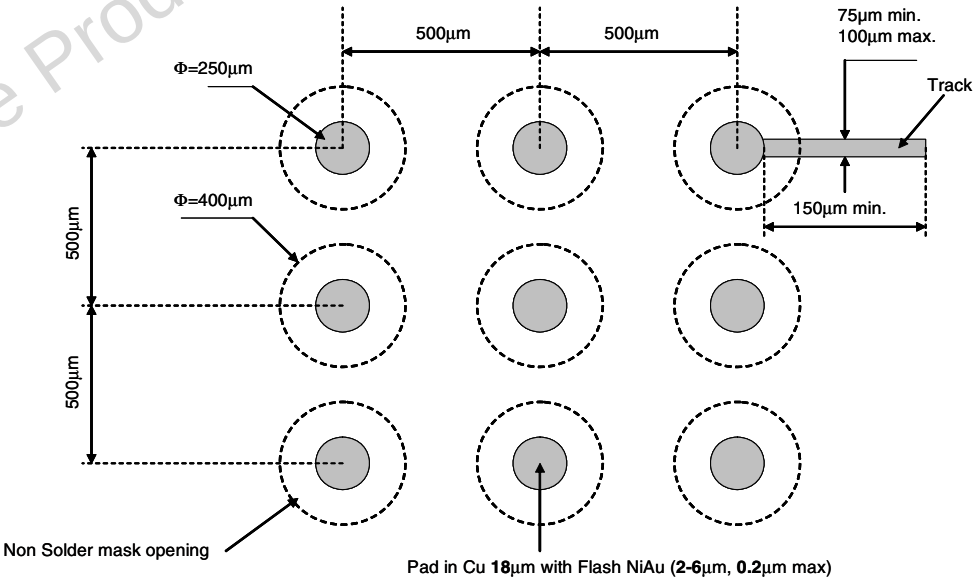


Figure 134. Pinout (top view)

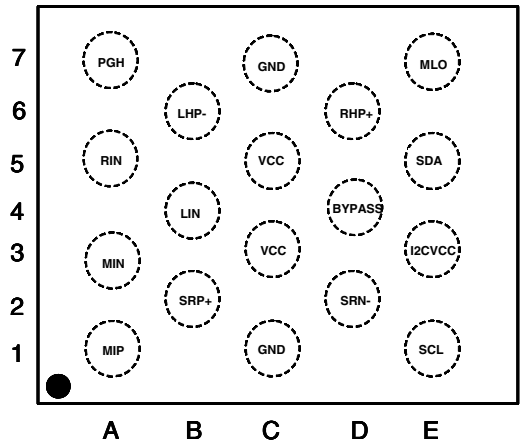
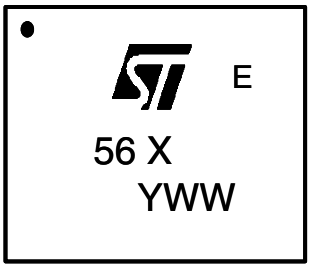


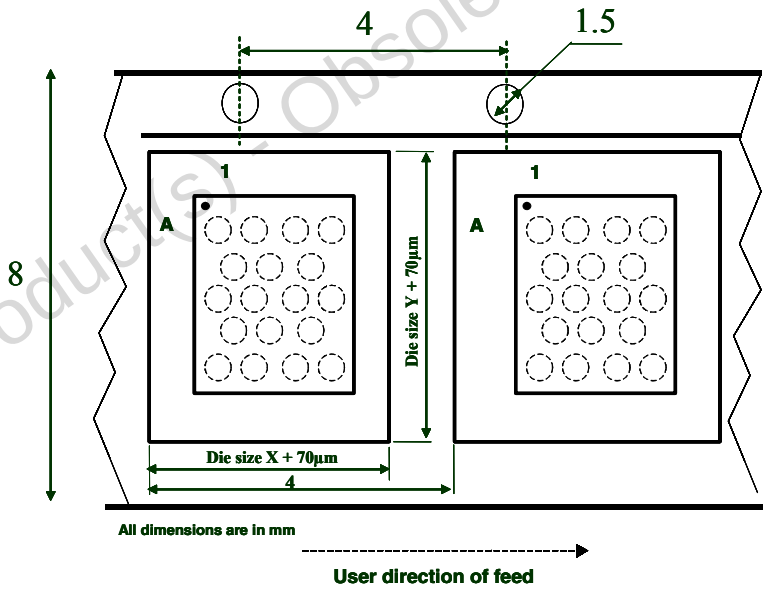
Figure 135. Marking (top view)



Markings are:

- ST logo
- First two letters give part number code:**56**
- Third letter gives assembly plant code: **X**
- Three digit date code: **YWW**
- Lead-free EcoPack symbol: **E**
- The dot marks pin **A1**

Figure 136. Tape and reel schematic (top view)

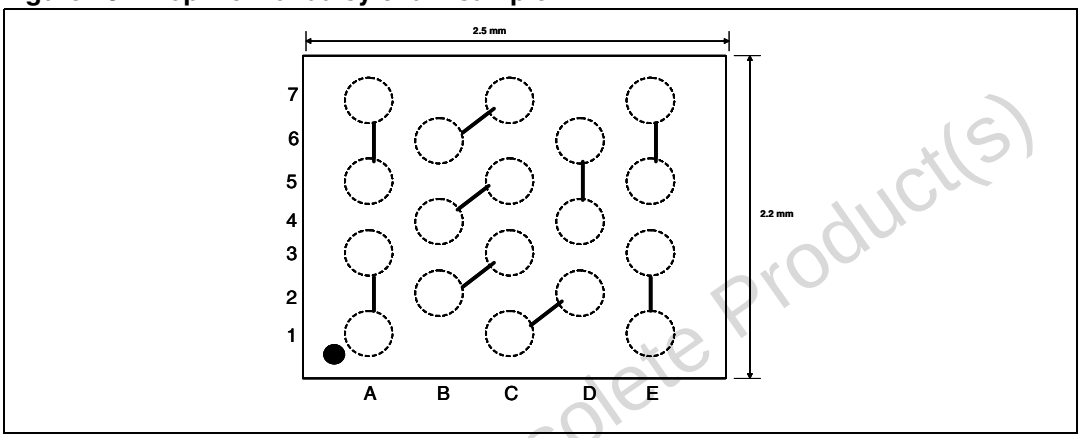


The devices are oriented in the carrier pocket with pin number 1A adjacent to the sprocket holes.

5.2 Daisy chain sample

The daisy chain sample features pins connected two by two. *Figure 137* illustrates the way in which the pins are connected to each other. This sample is used for testing continuity on the board. The PCB needs to be designed the opposite way, so that pins that are unconnected in the daisy chain sample are connected on the PCB. If you do this, by simply connecting an ohmmeter between pin A1 and pin A3, the soldering process continuity can be tested.

Figure 137. Top view of daisy chain sample



6 Ordering information

Table 14. Order code for daisy chain sample

Order code	Temperature range	Package	Marking
TSDC02JT	-40, +85° C	Flip-Chip18	DC2

Table 15. Order codes

Order code	Temperature range	Package	Packing	Marking
TS4956EIJT	-40°C to +85°C	Lead free flip-chip18	Tape & reel	56

7 Revision history

Table 16. Document revision history

Date	Revision	Changes
01-Nov-2005	1	First release corresponding to the preliminary data version.
01-Dec-2005	2	Cancellation of the back coating sale type.
01-May-2006	3	Final datasheet.
10-Mar-2009	4	Document reformatted. Updated input impedance values in all tables in *Chapter 3: Electrical characteristics*.