Ordering number : EN2769D

SANYO Semiconductors
DATA SHEET

LA5693D
LA5693M

Monolithic Linear IC with Watchdog Timer Voltage Regulator Driver

Overview

The LA5693D and LA5693M is a single-chip voltage regulator for microcomputer system monitor use that performs the functions of 5V output voltage control, watchdog timer, and voltage detector. Since the LA5693D and LA5693M can hold the reset output, it is especially suited for use in peripheral control and monitor output applications (example: valves used in refrigeration equipment, hot water supply system).

Features

- An external PNP transistor can be used to provide a low-saturation voltage regulator.
- Since the CK input has no edge detector, a high degree of flexibility is allowed in applications.
- Variable detection voltage.
- The watchdog time can be made longer.

Functions

- Output voltage 5V control.
- Watchdog timer.
- Power-ON reset function.
- Reset hold output [RES (2)] (Cleared with CK re-input).

Applications

- Microcomputer system for car equipment, refrigeration/heating equipment, office automation equipment.

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Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Control pin voltage	V_{CONT} max	1s	60	V
			41	V
Control pin current	I_{CONT} max		11	mA
CK input voltage	V_{CK} max		25	V
Reset pin voltage	$V_{\overline{RES}(1)}$ max, $V_{\overline{RES}(2)}$ max		41	V
Allowable power dissipation	Pd max	LA5693D	500	mW
		LA5693M	370	mW
Operating temperature	Topr		-40 to +85	°C
Storage temperature	Tstg		-55 to +150	°C

* : A PNP transistor is connected to the LA5693D, LA5693M externally to provide a low-saturation voltage regulator.
Therefore, ICONT≈100mA will flow, as starting current, in the VCC range where the output cannot be regulated.

Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Control pin voltage	V_{CONT}		6 to 40	V
Control pin current	I_{CONT} max		10	mA
Reset output current	$V_{\overline{RES}(1)}$ max, $V_{\overline{RES}(2)}$ max	External R pull-up	8	mA
Reset detection voltage	V_S min		4	V

Electrical Characteristics at Ta = 25°C, V_{CC} = 14V, I_O=50mA, unless otherwise specified.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Output voltage	VO		4.8	5.0	5.2	V
Line regulation1	$\Delta V_{OLN}1$	9V ≤ V_{CC} ≤ 16V		2	5	mV
Line regulation2	$\Delta V_{OLN}2$	6V ≤ V_{CC} ≤ 40V		4	30	mV
Load regulation	ΔV_{OLD}	1mA ≤ I_O ≤ 50mA		4	30	mV
Current dissipation	I_{CC}	I_O=0		4.4	6.5	mA
Output noise voltage	V_{NO}	10Hz ≤ f ≤ 100kHz, V_{CK} = 0V		150		μV
Temperature coefficient of output voltage	$\Delta V_O/\Delta Ta$	I_O = 5mA, –40°C ≤ Ta ≤ +85°C		±0.2		mV/°C
Reference voltage	V_{REF}		1.13	1.18	1.23	V
'H'-level CK input voltage	V_{IH}		2			V
'L'-level CK input voltage	V_{IL}				0.8	V
'H'-level CK input current	I_{IH}	V_{CK} = 5V		0.3	0.7	mA
'L'-level CK input current	I_{IL}	V_{CK} = 0V	-1.0	-0.1		μA
'H'-level reset output voltage	$V_{\overline{ORH}(1)}$/ $V_{\overline{ORH}(2)}$	$\overline{RES}$(2): 10kΩ pull-up	4.8	5.0	5.2	V
'L'-level reset output voltage 1	$V_{\overline{ORL}(1)}1$/ $V_{\overline{ORL}(2)}1$	$\overline{RES}$(2): 10kΩ pull-up		40	200	mV
'L'-level reset output voltage 2	$V_{\overline{ORL}(1)}2$/ $V_{\overline{ORL}(2)}2$	$I_{\overline{RES}(1)}$ = $I_{\overline{RES}(2)}$ = 8mA		0.16	0.8	V
CK input pulse width	t_{CKW}	V_{CK} = 5V	3			μs
Reset output delay time	t_d	C_t = 1μF	7.5	10	12.5	ms
Watchdog time	t_{WD}	C_t = 1μF	30	40	50	ms
Watchdog reset time	t_{WR}	C_t = 1μF	0.1	0.25	0.4	ms
Reset hysteresis voltage	V_{hys}	V_S = 4.5V	100	200	300	mV

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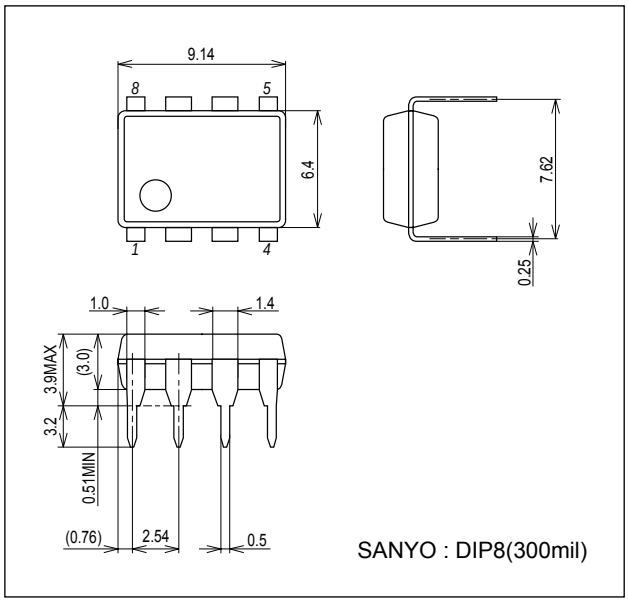
Package Dimensions

unit : mm (typ)

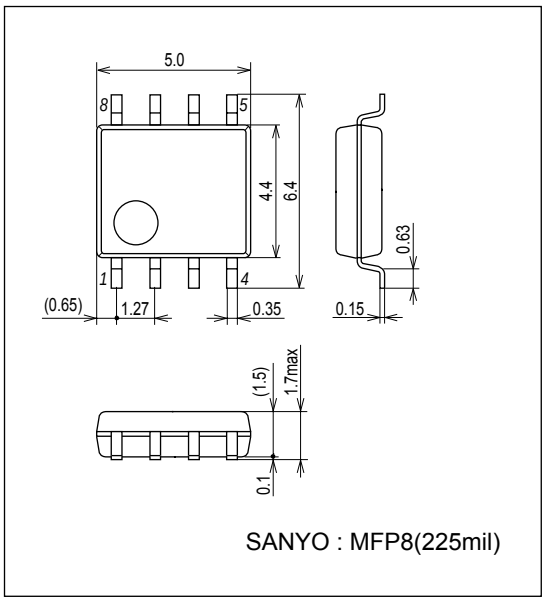
3001D [LA5693D]



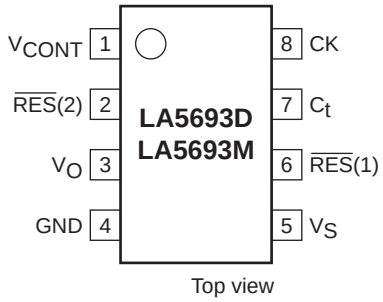
Package Dimensions

unit : mm (typ)

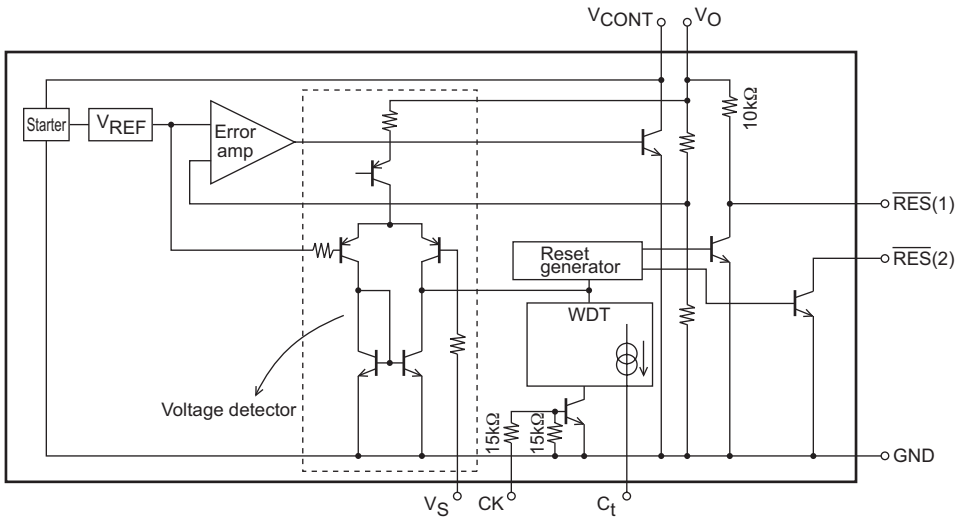
3032D [LA5693M]



Pin Assignment



Block Diagram



RES(1) : Contains a pull-up resistor of 10kΩ.
RES(2) : Open collector.

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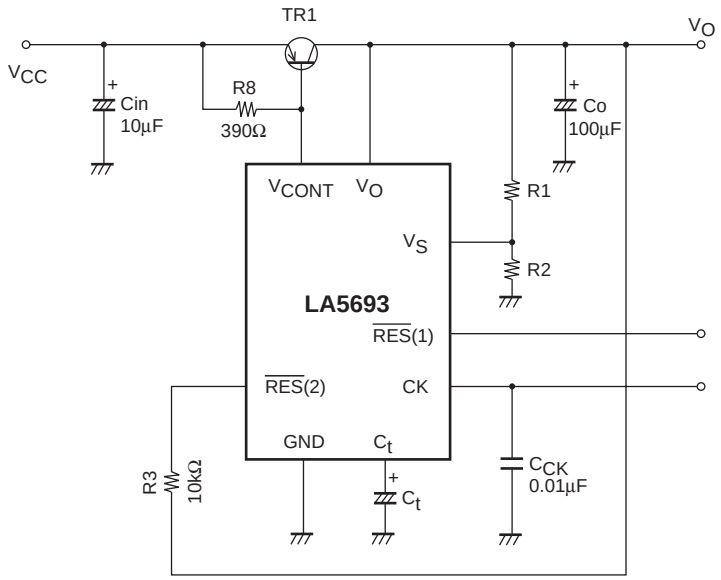
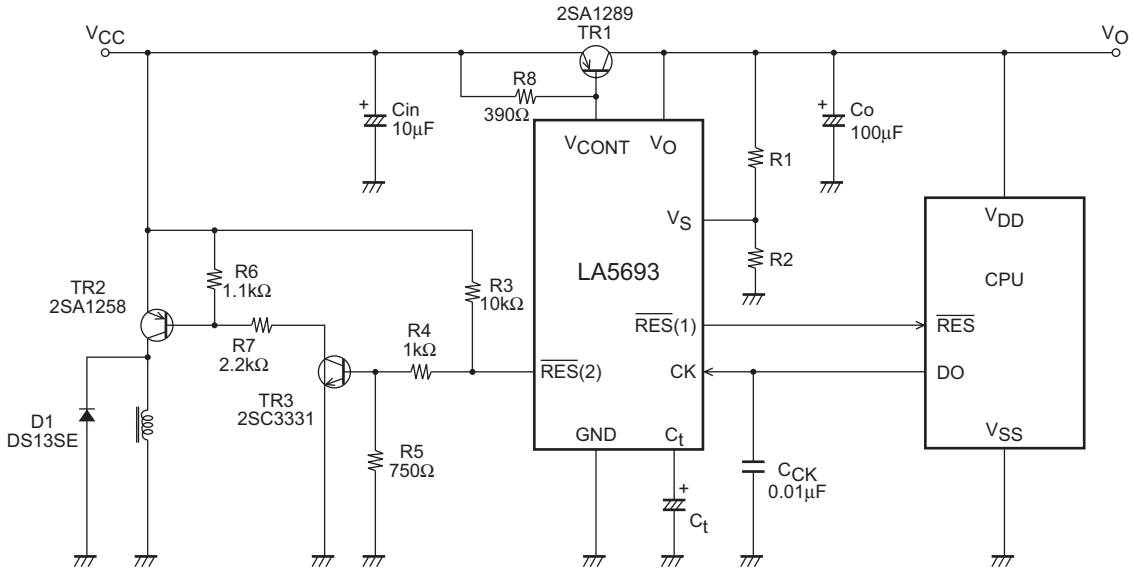
Test Circuit



Application Circuit Example



$V_S = V_{REF} \times \left(\frac{R1}{R2} + 1\right)$

$V_{REF} \approx 1.18$[V]

$t_d = 10 \times C_t(\mu F)$ [ms]

$t_{WD} = 40 \times C_t(\mu F)$ [ms]

$t_{WR} = 0.25 \times C_t(\mu F)$ [ms]

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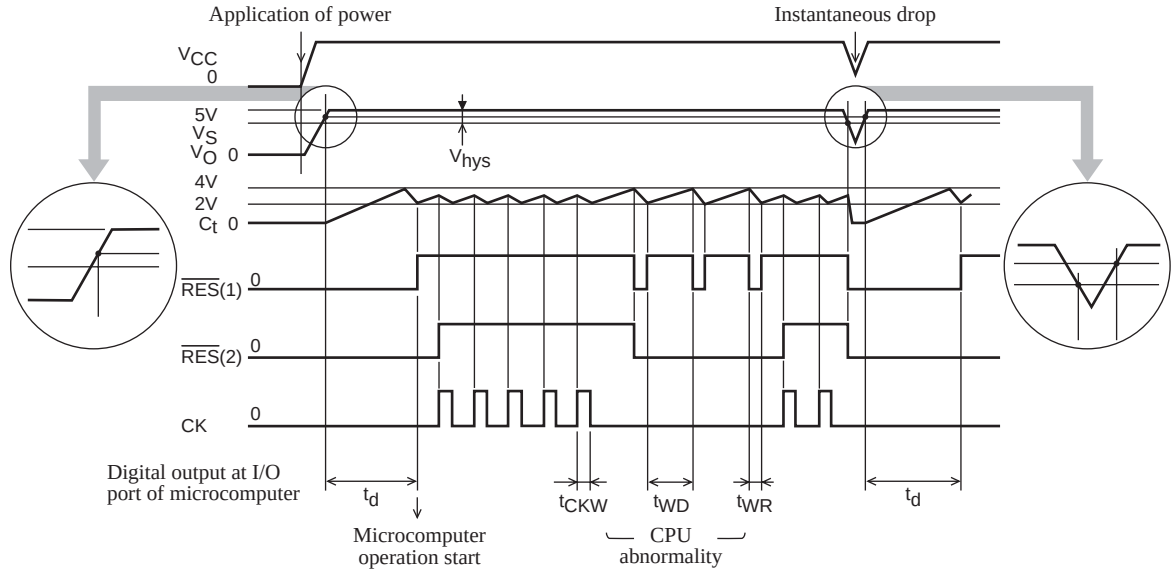
Note on application

1. For stable operation, place C_{in}, C_O, and TR1 as near to the IC as possible.
2. When used in 0°C or below it, a capacitor of which impedance at high-frequency operation is low and has a good temperature characteristic (such as SANYO OS-CON capacitor or others) should be used to prevent oscillation.
3. Set V_S to the output voltage level where the circuit will be reset using external resistors R1 and R2. VS should be set to 4V or greater due to internal circuit operation.
4. C_{CK} must be inserted to cut the high range element of clock noise to prevent it from becoming a reset output noise.
5. For C_t, a capacitor which less varies the capacitance according to the temperature should be used.

Timing Chart



Note : Edge-triggered at the point indicated by the arrow of CK signal.

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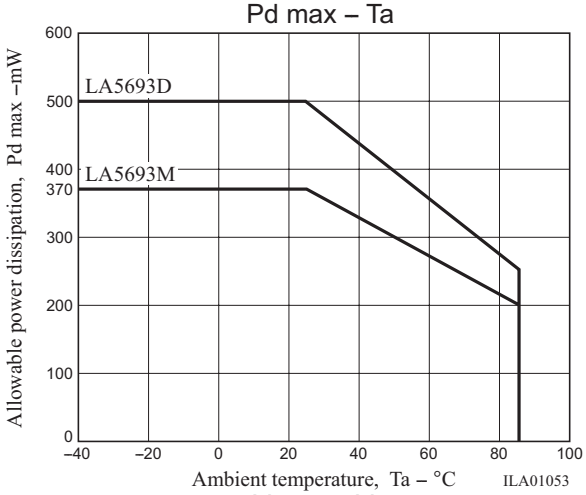
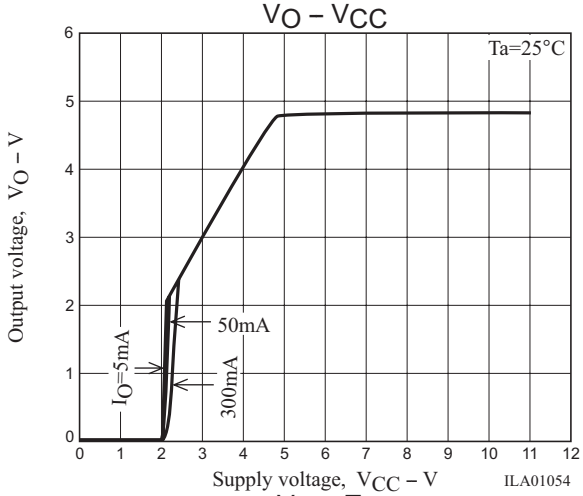
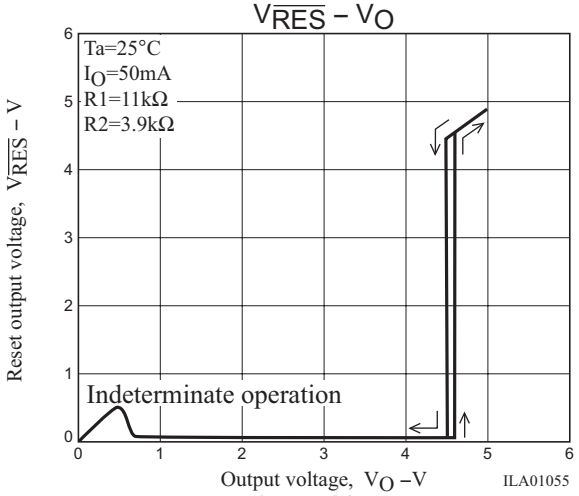
Pd max – Ta



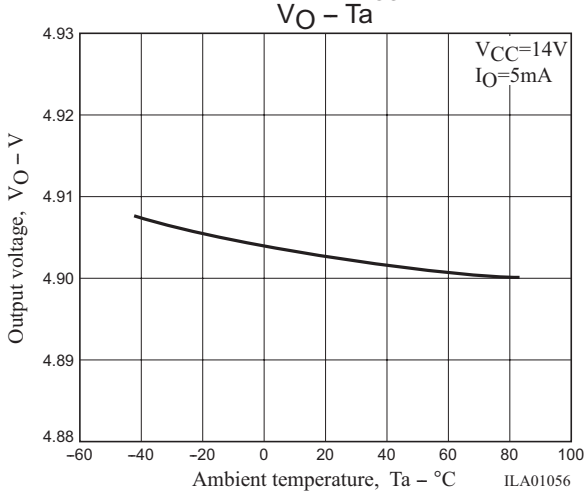
V_O – V_{CC}



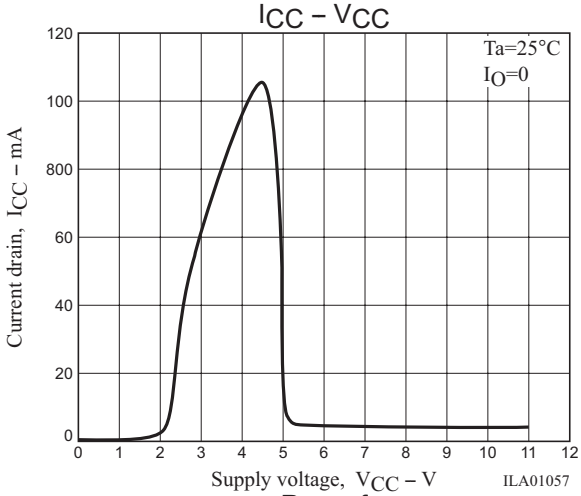
$V_{\overline{RES}}$ – V_O



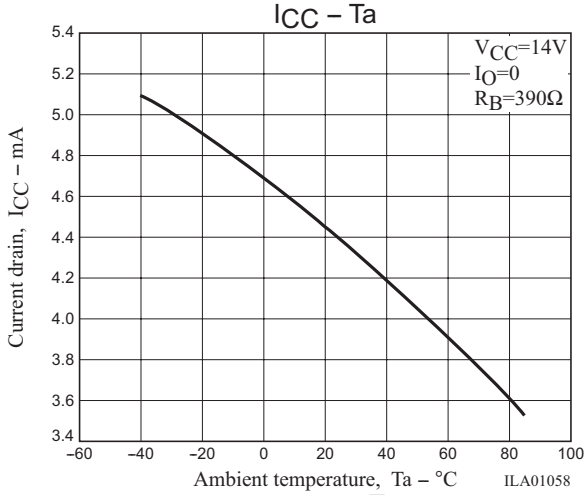
V_O – Ta



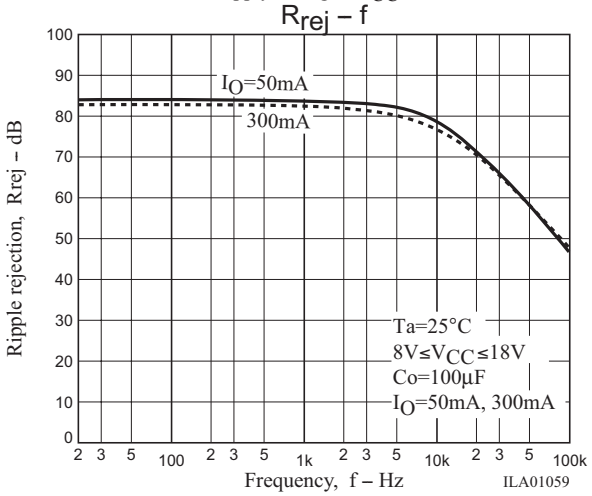
I_{CC} – V_{CC}



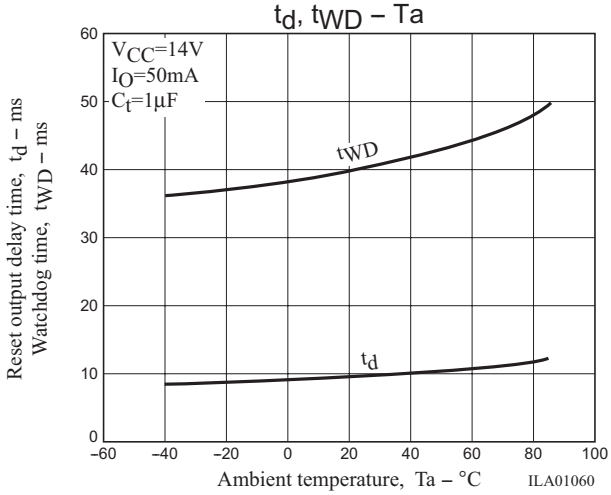
I_{CC} – Ta



R_{rej} – f



t_d, t_{WD} – Ta



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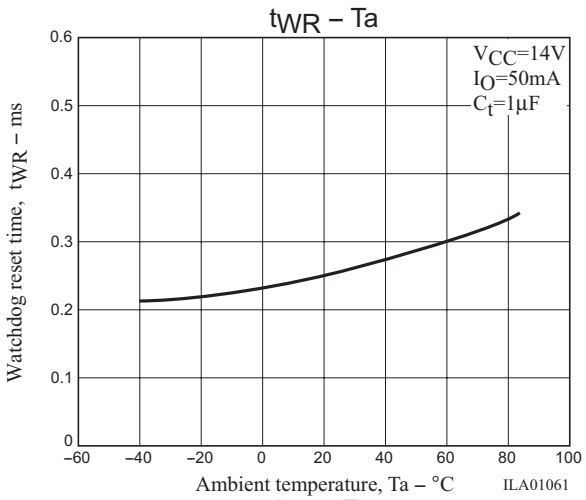

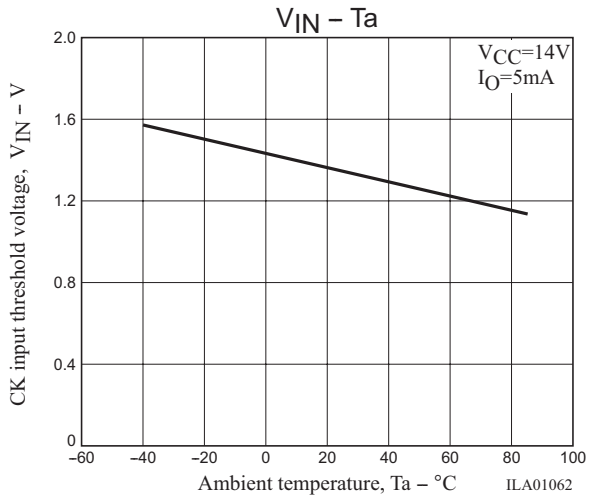

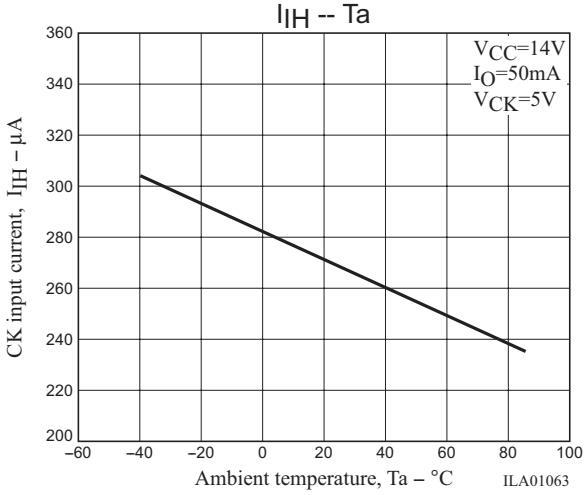

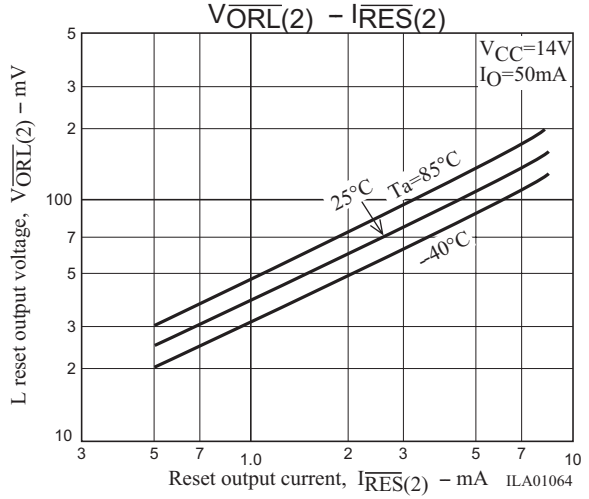

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