# STM6905

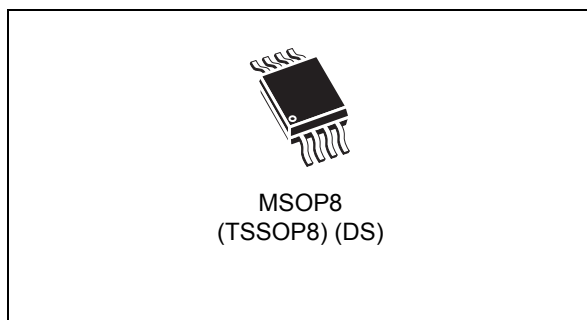## Quintuple, ultralow voltage supervisor with push-button reset

MSOP8
(TSSOP8) (DS)

- 600 mV internal reference
- $\overline{RST}$ output (open drain)
- Output guaranteed for $V_{CC} \geq 0.8$ V
- Reset delay time ($T_{REC}$) on power-up: 210 ms (typ)
- Manual reset input ($\overline{MR}$)
- Low supply current of 12 µA (typ)
- Power supply voltage 0.8 V to 5.5 V
- RoHS compliant (green package)
- 8-pin MSOP/TSSOP
- Operating temperature: –40 °C to 85 °C (industrial grade)

## Features

- Quintuple voltage monitoring
- Accurate ±1.8 % across temperature voltage threshold  (±1 % at 25 °C)
- Primary supply ($V_{CC}$) monitor. Fixed (factory - programmed) reset thresholds: 3.078 V to 2.866 V
- Second fixed (V2IN) monitor. Fixed (factory-programmed) reset thresholds: 2.333 V to 1.050 V
- Three additional adjustable supply monitor inputs (externally adjustable)

## Applications

- Set-top boxes
- Multi-voltage systems
- Cable/satellite applications
- Computer systems
- Data storage equipment

### Table 1. Device summary[1]

| Order code | $V_{RST1}$ (V) | $V_{RST2}$ (V) | $t_{REC}$ (ms) | Package |
|---|---|---|---|---|
| STM6905TZEDS6F | 3.078 | 2.333 | 210 | MSOP8 (TSSOP8) |
| STM6905TWEDS6F | 3.078 | 1.683 | 210 | MSOP8 (TSSOP8) |
| STM6905TGEDS6F | 3.078 | 1.110 | 210 | MSOP8 (TSSOP8) |
| STM6905SYEDS6F | 2.955 | 2.188 | 210 | MSOP8 (TSSOP8) |
| STM6905SFEDS6F | 2.955 | 1.050 | 210 | MSOP8 (TSSOP8) |
| STM6905PWEDS6F | 2.866 | 1.683 | 210 | MSOP8 (TSSOP8) |

1.    Other reset threshold voltages and $t_{REC}$ time-out periods are offered. Contact local ST sales office for availability.

This is information on a product in full production.

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# 1      Description

The STM6905 supervisor is a low voltage/low supply current processor supervisor, designed to monitor up to five system power supply voltages. This device is targeted at applications such as set-top boxes (STBs), portable, battery-powered systems, networking and communication systems.

The device supports a push-button type manual reset input ($\overline{MR}$). Two of the five supply monitors ($V_{CC}$ and V2IN) have fixed (customer-selectable, factory-trimmed) thresholds ($V_{RST1}$ and $V_{RST2}$). The other three voltage monitor inputs (V3IN, V4IN and V5IN) are monitored using externally adjustable threshold (600 mV internal reference) to meet specific level requirements.

If any of the five monitored voltages drops below its factory-trimmed or adjustable thresholds, or if the $\overline{MR}$ is asserted to logic low, the reset output $\overline{RST}$ is asserted (driven low). Once asserted, $\overline{RST}$ is maintained low for a minimum delay period ($t_{REC}$) after ALL monitored supplies rise above their respective thresholds and $\overline{MR}$ returns to high. The reset output logic state is valid for $V_{CC}$ greater than 0.8 V.

The STM6905 is available in a standard 8-lead MSOP (TSSOP) package.

**Figure 1. Logic diagram**
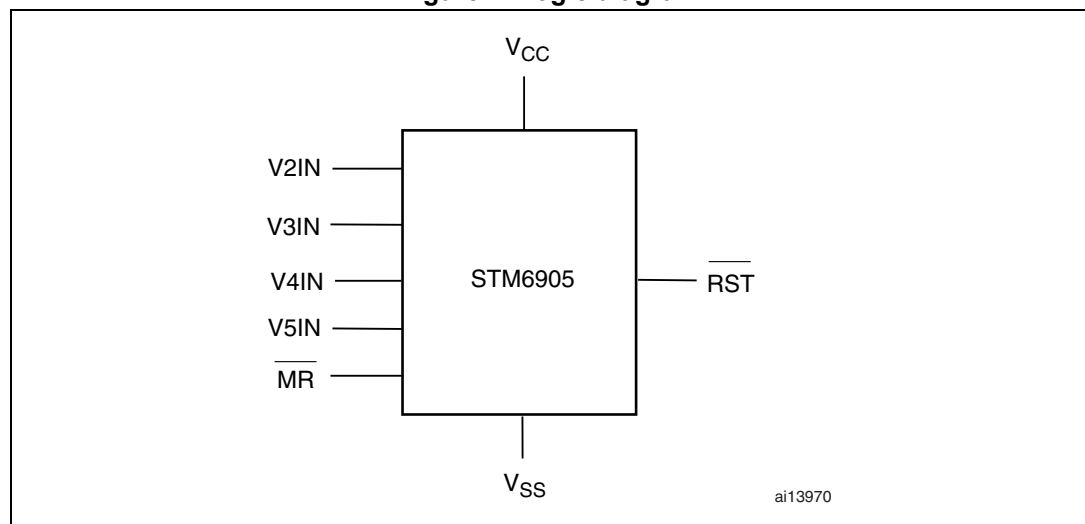


**Figure 2. MSOP/TSSOP-8 connections**
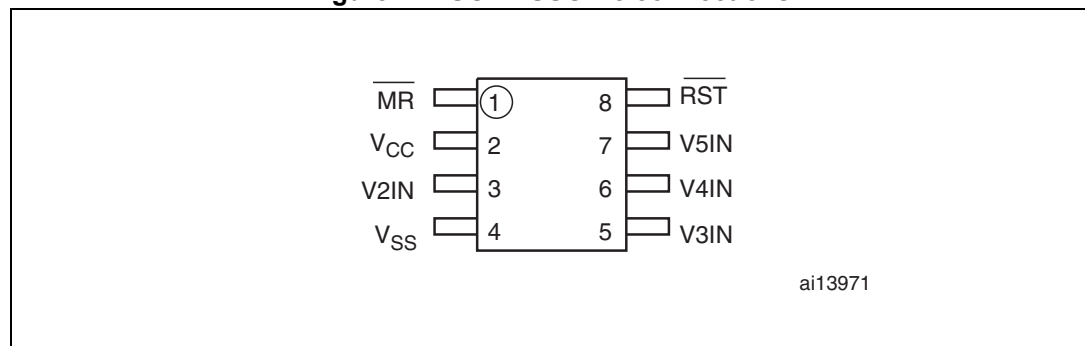
## Table 2. Signal names and functions

| Pin | Name | Type | Function |
|-----|------|------|----------|
| 1 | $\overline{\text{MR}}$ | Input | Active-low manual reset input with internal pull-up resistor |
| 2 | $V_{CC}$ | Supply | Primary supply voltage input and integrated fixed threshold under-voltage monitor |
| 3 | V2IN | Input | Second fixed threshold input monitor |
| 4 | $V_{SS}$ | Supply | Ground |
| 5 | V3IN | | Adjustable third reset comparator input |
| 6 | V4IN | Input | Adjustable fourth reset comparator input |
| 7 | V5IN | | Adjustable fifth reset comparator input |
| 8 | $\overline{\text{RST}}$ | Output | Active-low open-drain reset output (10 kΩ internal pull-up) |

# 2 Pin descriptions

## 2.1 Push-button reset input ($\overline{MR}$)

When $\overline{MR}$ goes low the $\overline{RST}$ output is driven low. $\overline{RST}$ remains low as long as $\overline{MR}$ is low and for the $t_{REC}$ after $\overline{MR}$ returns to high. The active-low input has an internal 10 kΩ pull-up resistor to $V_{CC}$. It can be driven from a TTL or CMOS logic line, or with open drain/collector outputs, or connected to $V_{SS}$ through a switch. If unused, leave this pin open or connect it to $V_{CC}$.

Connect a normally open momentary switch from $\overline{MR}$ to $V_{SS}$. An external debounce circuitry is not required (if $\overline{MR}$ is driven from long cables or if the device is used in noisy environments, connecting a 0.1 µF capacitor from $\overline{MR}$ to $V_{SS}$ provides additional noise immunity).

## 2.2 $V_{CC}$ primary supply voltage monitoring input

The $V_{CC}$ pin is also the input for the primary reset threshold monitor. Fixed (customer-selectable, factory programmed) reset thresholds include 3.078 V to 2.866 V.

## 2.3 V2IN second fixed voltage monitoring input

The V2IN input is the second fixed-voltage input for reset threshold monitoring. Available fixed (customer-selectable, factory programmed) reset thresholds include 2.333 V to 1.050 V.

## 2.4 $V_{SS}$

This pin is the ground pin for the power supply.

## 2.5 V3IN, V4IN, and V5IN

The V3IN, V4IN and V5IN are high impedance inputs. $\overline{RST}$ is driven low when the voltage (VTRIP) at the pin falls below 600 mV (internal reference voltage at their respective comparators). The monitored voltage reset threshold is set with an external resistor-divider network.

## 2.6 $\overline{RST}$ active-low, open drain reset output

The reset output ($\overline{RST}$) pin is driven low and stays low whenever $V_{CC}$ or V2IN, or V3IN, or V4IN, or V5IN falls below its factory-trimmed or adjustable reset threshold or when $\overline{MR}$ goes to logic low. It remains low for $t_{REC}$ after all supply voltages being monitored rise above their reset thresholds and $\overline{MR}$ goes from low to high. Connect an external pull-up resistor to $V_{CC}$. A 10 kΩ pull-up resistor should be sufficient for most applications.

## Figure 3. Functional block diagram
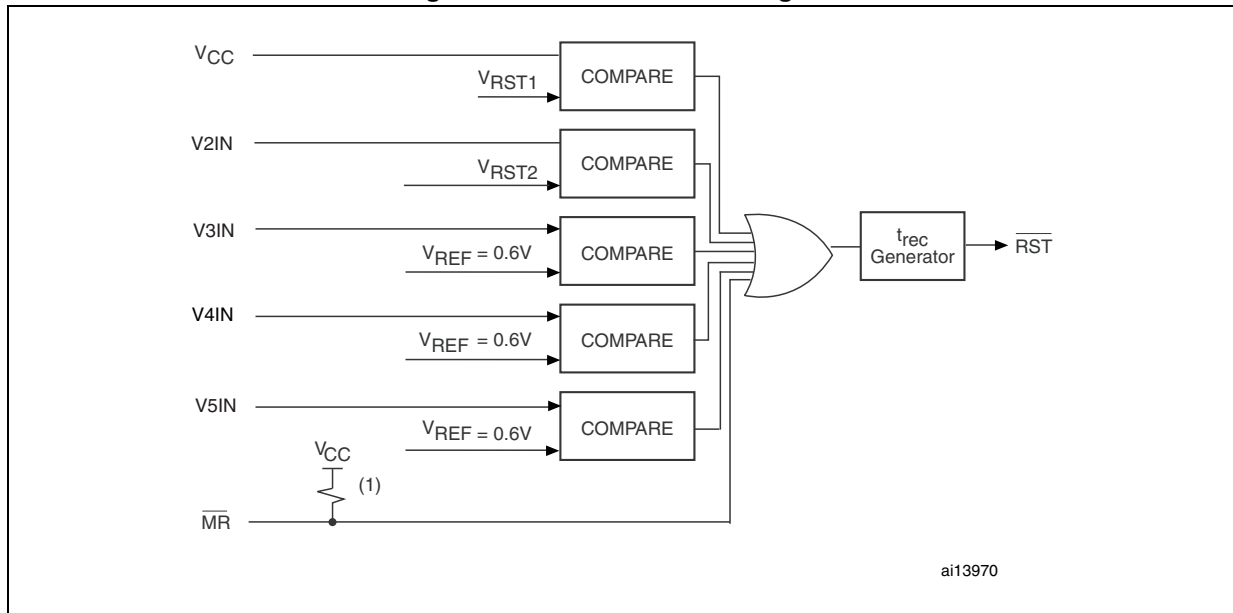


1. Internal pull-up on $\overline{MR}$ input of 10 kΩ (typ).

## Figure 4. Typical hardware hookup application diagram
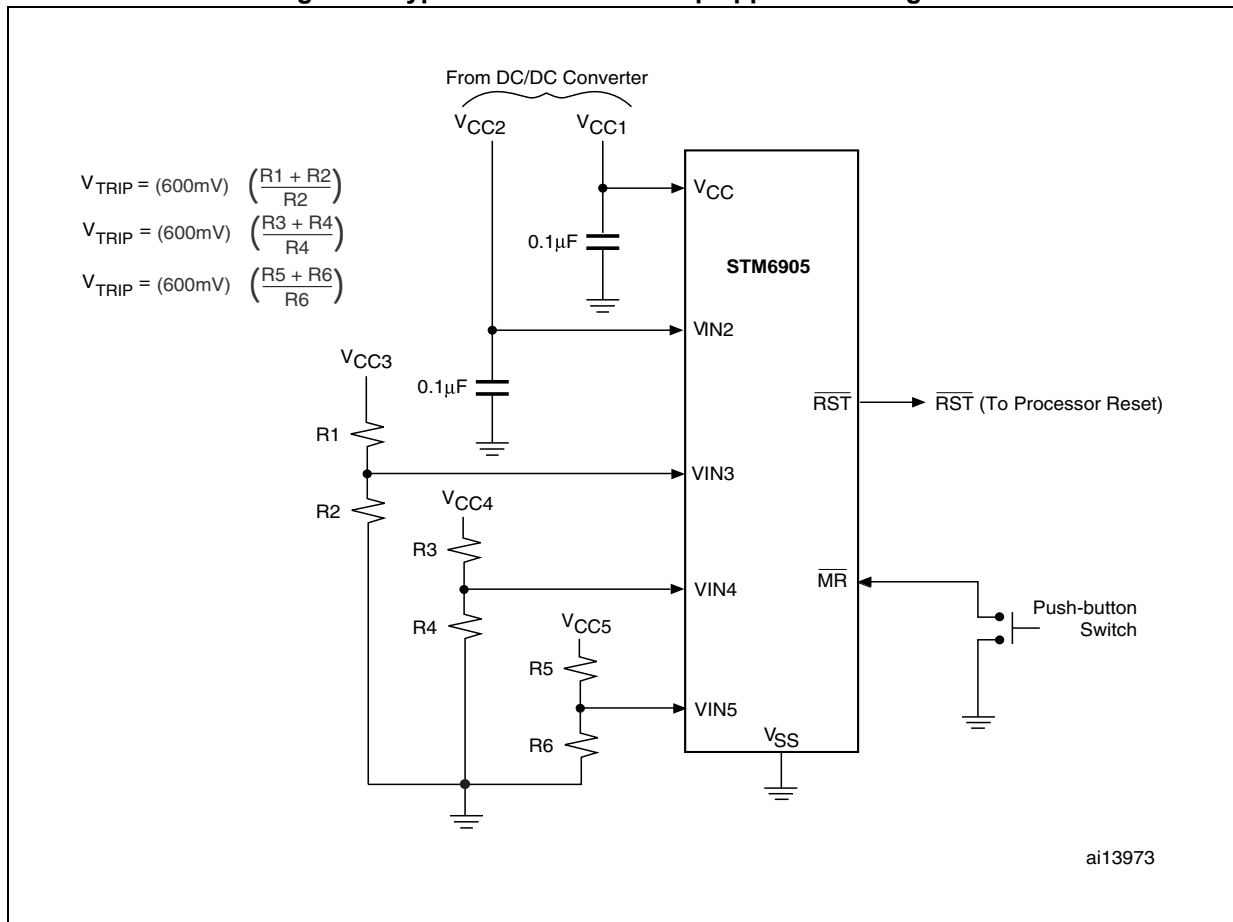
# 3 Operation

The STM6905 can monitor critical voltages such as power-supply and battery voltage levels, while interfacing easily with the system controllers/microprocessors.

*Figure 4* shows the typical hardware hookup for monitoring five voltages: two fixed thresholds (customer-selectable, factory-programmed) and three adjustable monitor inputs. The $\overline{RST}$ output is open drain and requires a 10 kΩ pull-up resistor tied to $V_{CC}$.

## 3.1 Setting the adjustable voltage levels for V3IN, V4IN, and V5IN inputs

The user can customize the minimum voltage levels for the three adjustable voltage inputs by connecting an external resistor divider network to the V3IN, V4IN and V5IN pins in order to set the trip point at some voltage above the 600 mv ($V_{REF}$) according to the following formula.

$$VTRIP \; = \; 0.6\,V \times \frac{R1 + R2}{R2}$$

During normal operation, the STM6905 monitors the voltage levels at all five pins (Vcc, V2IN, V3IN, V4IN, and V5IN).

## 3.2 Power on reset ($t_{REC}$)

On power up, the STM6905 activates a power-on reset circuit which asserts the reset pin (i.e. $\overline{RST}$ goes low). The $\overline{RST}$ signal remains active until $V_{CC}$ (and V2IN, V3IN, V4IN, V5IN, and $\overline{MR}$) rises above the minimum voltage level for the time period $t_{REC}$ thereby ensuring that the supply voltage has stabilized to sufficient operating levels.

# 4 Voltage monitoring

**Figure 5. $\overline{MR}$ timing waveforms**
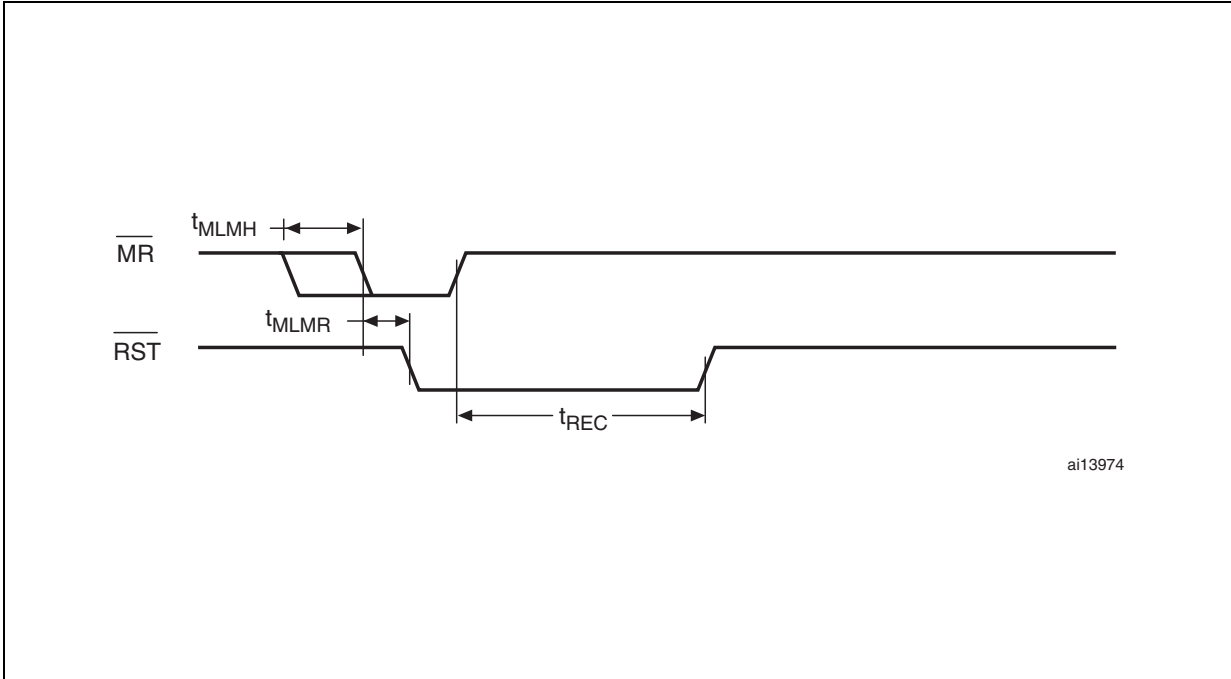


**Figure 6. Voltage monitoring diagram**
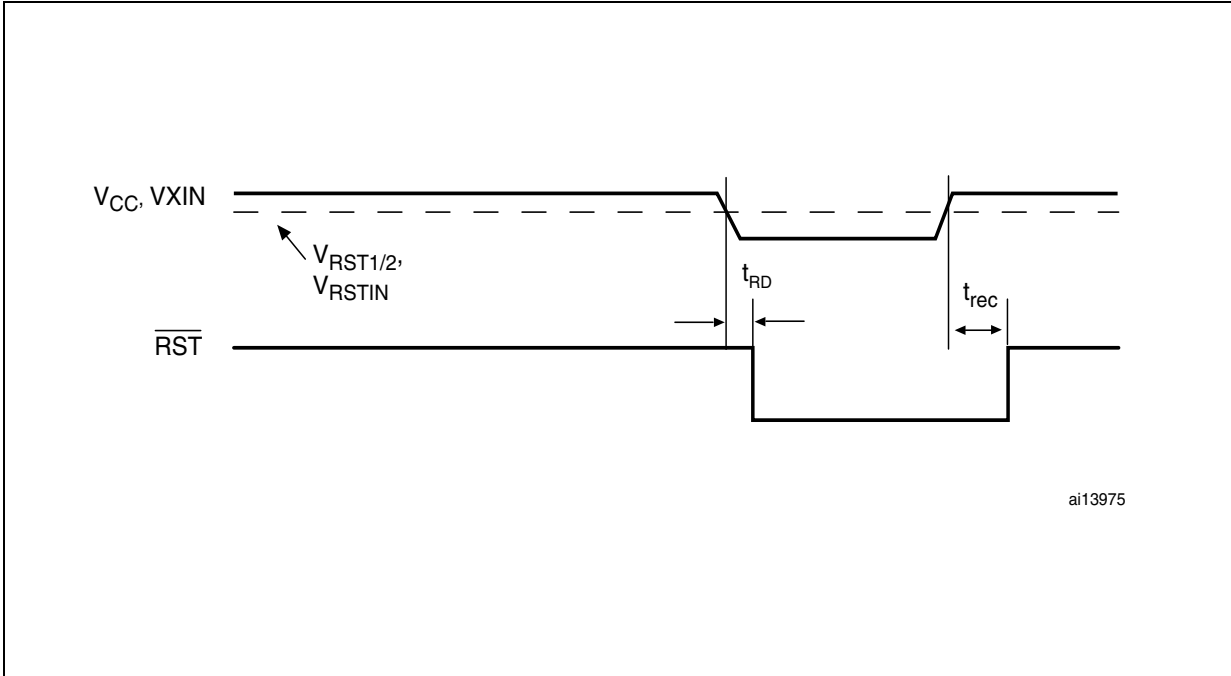
# 5      Maximum rating

Stressing the device above the ratings listed in the "Absolute maximum ratings" table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE program and other relevant quality documents.

**Table 3. Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|--------|-----------|-------|------|
| $T_{STG}$ | Storage temperature ($V_{CC}$ off) | -55 to +150 | °C |
| $T_{SLD}$[1] | Lead solder temperature for 10 seconds | 260 | |
| $V_{IO}$ | Input or output voltage | -0.3 to $V_{CC}$ +0.3 | V |
| $V_{CC}$ | Supply voltage | -0.3 to 7.0 | |
| $I_O$ | Output current | 20 | mA |
| $\theta_{JA}$ | Thermal resistance (junction to ambient) | 146 | °C/W |

1.    Reflow at peak temperature of 255 °C to 260 °C for < 30 seconds (total thermal budget not to exceed 180 °C for between 90 to 150 seconds).

# 6      DC and AC parameters

This section summarizes the operating measurement conditions and the DC and AC characteristics of the device. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

**Table 4. DC and AC characteristics**

| Symbol | Alter-native | Description | Test condition[1] | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| $V_{CC}$ | | Operating voltage | | | 0.8 | | 5.5 | V |
| $I_{CC}$ | | $V_{CC}$ supply current | $V_{CC}$ < 5.5 V | | | 12 | 16 | |
| | | | $V_{CC}$ = 3.3 V | | | 11 | 15 | |
| I2IN | | V2IN supply current | V2IN = 3.3 V | | | 3 | 5 | |
| $I_{LI}$ | | Input leakage current ($\overline{MR}$)[2] | $V_{IN}$ = $V_{CC}$ or $V_{SS}$ | | -0.5 | | +0.5 | μA |
| $I_{LO}$[3] | | Open drain $\overline{RST}$ output leakage current | $V_{CC}$ > VRST, $\overline{RST}$ not asserted | | -0.5 | | +0.5 | |
| $V_{OL}$ | | Output low voltage ($\overline{RST}$, open drain) | $V_{CC}$ ≥ 0.8 V, $I_{SINK}$ = 1 μA | | | | 0.3 | V |
| | | | $V_{CC}$ ≥ 1.0 V, $I_{SINK}$ = 50 μA | | | | 0.3 | |
| | | | $V_{CC}$ ≥ 1.2 V, $I_{SINK}$ = 100 μA | | | | 0.3 | |
| | | | $V_{CC}$ ≥ 2.7 V, $I_{SINK}$ = 1.2 mA | | | | 0.3 | |
| | | | $V_{CC}$ ≥ 4.5 V, $I_{SINK}$ = 3.2 mA | | | | 0.4 | |
| $V_{RST1}$[4] | $V_{TH1}$ | $V_{CC}$ reset threshold | T (falling) | 25°C | 3.047 | 3.078 | 3.109 | |
| | | | | -40 °C to 85 °C | 3.023 | | 3.133 | |
| | | | S (falling) | 25 °C | 2.925 | 2.955 | 2.985 | |
| | | | | -40 °C to 85 °C | 2.902 | | 3.008 | |
| | | | P (falling) | 25 °C | 2.837 | 2.866 | 2.895 | |
| | | | | -40 °C to 85 °C | 2.814 | | 2.918 | |
| $V_{RST2}$[4] | $V_{TH2}$ | V2IN reset threshold | Z (falling) | 25 °C | 2.310 | 2.333 | 2.356 | |
| | | | | -40 °C to 85 °C | 2.291 | | 2.375 | |
| | | | Y (falling) | 25 °C | 2.166 | 2.188 | 2.210 | |
| | | | | -40 °C to 85 °C | 2.149 | | 2.227 | |
| | | | W (falling) | 25 °C | 1.666 | 1.683 | 1.700 | |
| | | | | -40 °C to 85 °C | 1.653 | | 1.713 | |
| | | | G (falling) | 25 °C | 1.099 | 1.110 | 1.121 | |
| | | | | -40 °C to 85 °C | 1.090 | | 1.130 | |
| | | | F (falling) | 25 °C | 1.040 | 1.050 | 1.061 | |
| | | | | -40 °C to 85 °C | 1.031 | | 1.069 | |

**Table 4. DC and AC characteristics (continued)**

| Symbol | Alter-native | Description | Test condition[1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{HYST}$ | | Reset threshold hysteresis | Referenced to $V_{RST1}/V_{RST2}$ typical | | 0.5 | | % |
| $t_{RD}$ | | $V_{CC}$ to $\overline{RST}$ delay | $V_{CC}$ = ($V_{RST1}$ + 100 mV) to ($V_{RST1}$ – 100 mV) | | 20 | | µs |
| | | | V2IN = ($V_{RST2}$ + 75 mV) to ($V_{RST2}$ – 75 mV) | | 20 | | |
| $t_{REC}$ | $t_{RP}$ | $\overline{RST}$ time-out period | Option B[5] | 20 | 30 | 40 | ms |
| | | | Option C[5] | 80 | 120 | 180 | |
| | | | Option E | 140 | 210 | 280 | |
| | | | Option F[5] | 280 | 420 | 560 | |
| **Adjustable reset comparator input (V3IN, V4IN, V5IN)** | | | | | | | |
| $V_{RSTIN}$ | | V3IN, V4IN, V5IN input threshold | | 589 | 600 | 611 | mV |
| $I_{RSTIN}$ | | V3IN, V4IN, V5IN input current | V3IN, V4IN, V5IN > 0.8 V | –25 | | +25 | nA |
| | | V3IN, V4IN, V5IN hysteresis | | | 3 | | mV |
| $t_{RSTIND}$ | | V3IN, V4IN, V5IN to $\overline{RST}$ output delay | VRSTIN to (VRSTIN – 30 mV) | | 22 | | µs |
| **Manual (push-button) reset input** | | | | | | | |
| $V_{IL}$ | | $\overline{MR}$ input voltage | | | | 0.3 x $V_{CC}$ | V |
| $V_{IH}$ | | | | 0.7 x $V_{CC}$ | | | |
| $t_{MLMH}$ | $t_{MR}$ | $\overline{MR}$ minimum pulse width | | 1 | | | µs |
| $t_{MLRL}$ | $t_{MRD}$ | $\overline{MR}$ to $\overline{RST}$ output delay | | | 200 | | ns |
| | | $\overline{MR}$ glitch immunity | | | 100 | | |
| | | $\overline{MR}$ pull-up resistance | | | 10 | | kΩ |

1.  Valid for ambient operating temperature: $T_A$ = –40 °C to +85 °C; $V_{CC}$ = 0.8 V to 5.5 V (except where noted).

2.  10 kΩ (typ) internal pull-up resistor.

3.   The leakage current measured on the $\overline{RST}$ pin is tested with the reset de-asserted (output high impedance).

4.  Other reset threshold voltages are offered. Minimum order quantities may apply. Contact local sales office for availability.

5.  Other $t_{REC}$ time-out periods are offered. Minimum order quantities may apply. Contact local sales office for availability.

# 7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

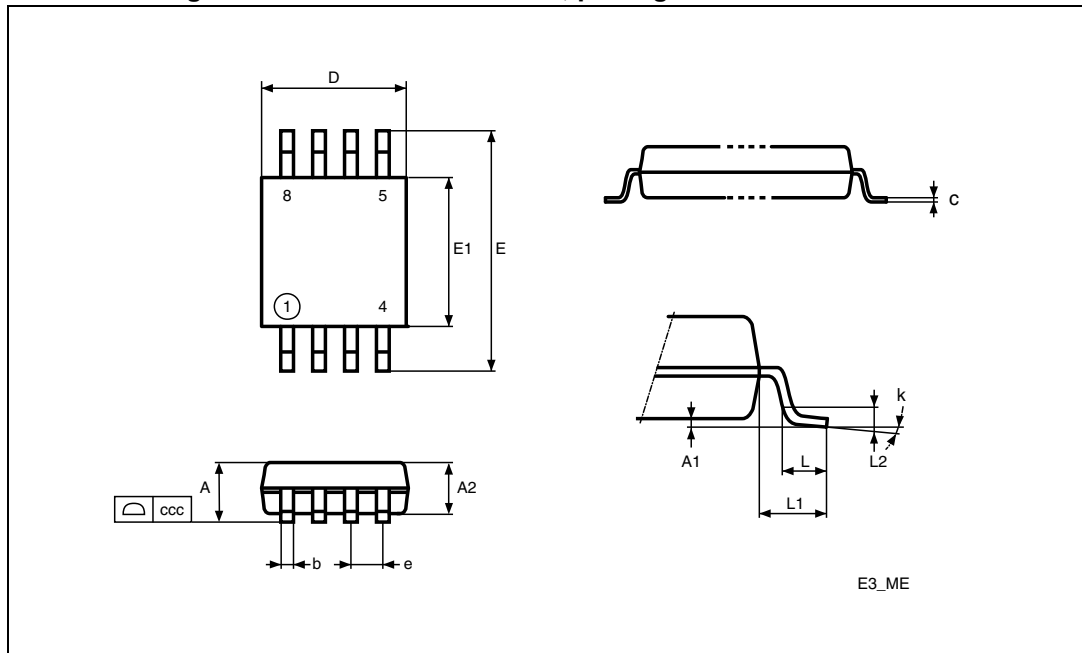### Figure 7. TSSOP8 3 mm x 3 mm, package mechanical outline



### Table 5. TSSOP8 3 mm x 3 mm, package mechanical data

| Symbol | mm | | | inches | | |
|--------|-----|-----|-----|-----|-----|-----|
|        | Min | Typ | Max | Min | Typ | Max |
| A      |     |     | 1.100 |     |     | 0.043 |
| A1     | 0.00 |    | 0.15 | 0.000 |   | 0.006 |
| A2     | 0.75 | 0.85 | 0.95 | 0.030 | 0.034 | 0.037 |
| b      | 0.22 |    | 0.40 | 0.009 |   | 0.016 |
| c      | 0.08 |    | 0.23 | 0.003 |   | 0.009 |
| ccc    |     |     | 0.10 |     |     | 0.004 |
| D      | 2.80 | 3.00 | 3.20 | 0.110 | 0.118 | 0.126 |
| e      |     | 0.65 |     |     | 0.026 |     |
| E      | 4.65 | 4.90 | 5.15 | 0.183 | 0.193 | 0.203 |
| E1     | 2.80 | 3.00 | 3.10 | 0.110 | 0.118 | 0.122 |
| L      | 0.40 | 0.60 | 0.80 | 0.016 | 0.024 | 0.032 |
| L1     |     | 0.95 |     |     | 0.037 |     |
| L2     |     | 0.25 |     |     | 0.010 |     |
| k      | 0° | 4 | 6° | 0° | 4 | 6° |
| N      | 8 | | | 8 | | |

# 8 Part numbering

## Table 6. Ordering information scheme

Example: STM6905 TZ E DS 6 F

**Device type**

STM6905

**Reset threshold voltages[1]**

| Suffix | $V_{RST1}$ | $V_{RST2}$ |
|--------|-----------|-----------|
| TZ | 3.078 | 2.333 |
| TW | 3.078 | 1.683 |
| TG | 3.078 | 1.110 |
| SY | 2.955 | 2.188 |
| SF | 2.955 | 1.050 |
| PW | 2.866 | 1.683 |

**$t_{REC}$**

B = 30 ms[1]

C = 120 ms[1]

E = 210 ms

F = 420 ms[1]

**Package**

DS = MSOP8 (TSSOP8)

**Temperature range**

6: -40 °C to 85 °C

**Shipping method**

E = ECOPACK® package, tubes

F = ECOPACK® package, tape and reel

1. Other reset threshold voltages and $t_{REC}$ time-out periods are offered. Minimum order quantities may apply. Contact local sales office for availability.

# 9     Package marking information

**Table 7. Marking description**

| Part marking | $V_{RST1}$ (V) | $V_{RST2}$ (V) | Package | Topside marking |
|---|---|---|---|---|
| STM6905TZEDS6F | | 2.333 | | STZE |
| STM6905TWEDS6F | 3.078 | 1.683 | | STWE |
| STM6905TGEDS6F | | 1.110 | MSOP (TSSOP8) | STGE |
| STM6905SYEDS6F | 2.955 | 2.188 | | SSYE |
| STM6905SFEDS6F | | 1.050 | | SSFE |
| STM6905PWEDS6F | 2.866 | 1.683 | | SPWE |

# 10 Revision history

**Table 8. Document revision history**

| Date | Revision | Changes |
|------|----------|---------|
| 19-Dec-2007 | 1 | Initial release. |
| 23-Jan-2008 | 2 | Document status upgraded to full datasheet. |
| 28-Jan-2008 | 3 | Updated cover page, *Figure 6*, and *Table 4*. |
| 20-Oct-2014 | 4 | Small text changes to English<br>*Table 1*: updated footnote *1*<br>*Table 6*: updated the reset threshold voltage of "SY" ($V_{RST2}$) |

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