NCP802

Highly Integrated Lithium Battery Protection Circuit for One Cell Battery Packs

The NCP802 resides in a lithium battery pack where the battery cell continuously powers it. This circuit senses cell voltage, charge current, and discharge current, and correspondingly controls the state of two, N−channel MOSFET switches. These switches reside in series with the negative terminal of the cell and the negative terminal of the battery pack. During a fault condition, the NCP802 open circuits the pack by turning off one of these MOSFET switches, which disconnects the current path. Internal delay circuitry minimizes external component count.

Features

- Highly Accurate Overvoltage Detector
  - ±25 mV at Room Temperature
  - ±30 mV from −5 to 55°C
- Fault Detection Thresholds
  - Overvoltage Threshold:
    - SN1/SAN1 = 4.35 V, SAN5 = 4.275 V, SAN6 = 4.28 V
  - Undervoltage Threshold:
    - SN1/SAN1 = 2.4 V, SAN5/6 = 2.3 V
  - Discharge Current Threshold:
    - SN1/SAN1/SAN6 = 0.2 V, SAN5 = 0.1 V
  - Charge Current Threshold: 0.1 V
- Internal Output Delays
  - Overvoltage Output Delay:
    - SN1/SAN1/SAN6 = 250 ms, SAN5 = 1 ms
  - Undervoltage Output Delay: 20 ms
  - Discharge Current Output Delay:
    - SN1/SAN1/SAN6 = 12 ms, SAN5 = 6 ms
  - Charge Current Output Delay:
    - SN1/SAN1/SAN6 = 16 ms, SAN5 = 8 ms
- Absolute Maximum Rating of 28 V for the Charger Input
- Low Quiescent Current
  - Normal Operating Current: 3.0 μA
  - Standby Current when Cells are Discharged: 0.1 μA
- Zero Volt Charging
- Available in a Low Profile Surface Mount Package
- Pb−Free Packages are Available*

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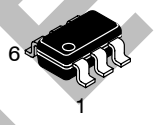
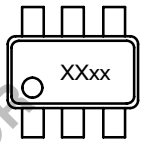
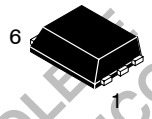
MARKING DIAGRAMS

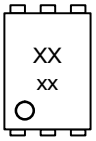


SOT23−6
SN SUFFIX
CASE 1262



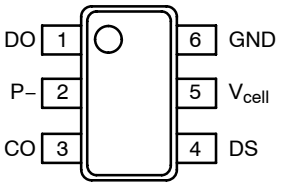


SON−6
SAN SUFFIX
CASE 494

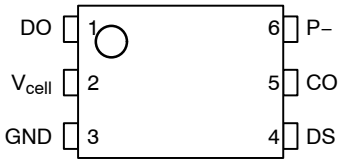


XX = Specific Device Code
xx = Date Code

PIN CONNECTIONS



SOT23−6
(Top View)



SON−6
(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 20 of this data sheet.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

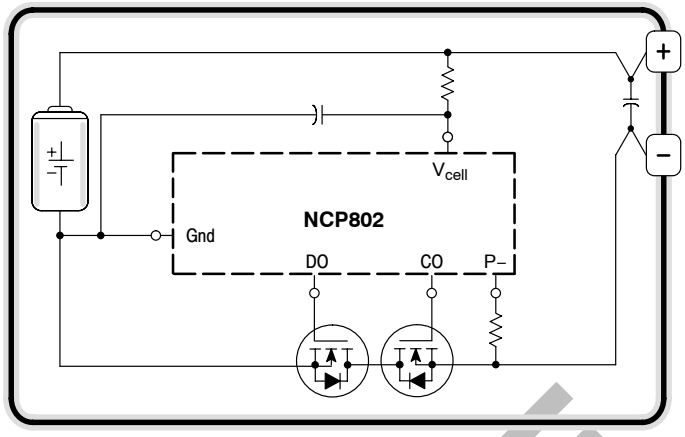


Figure 1. Typical One Cell Lithium Ion Battery Pack

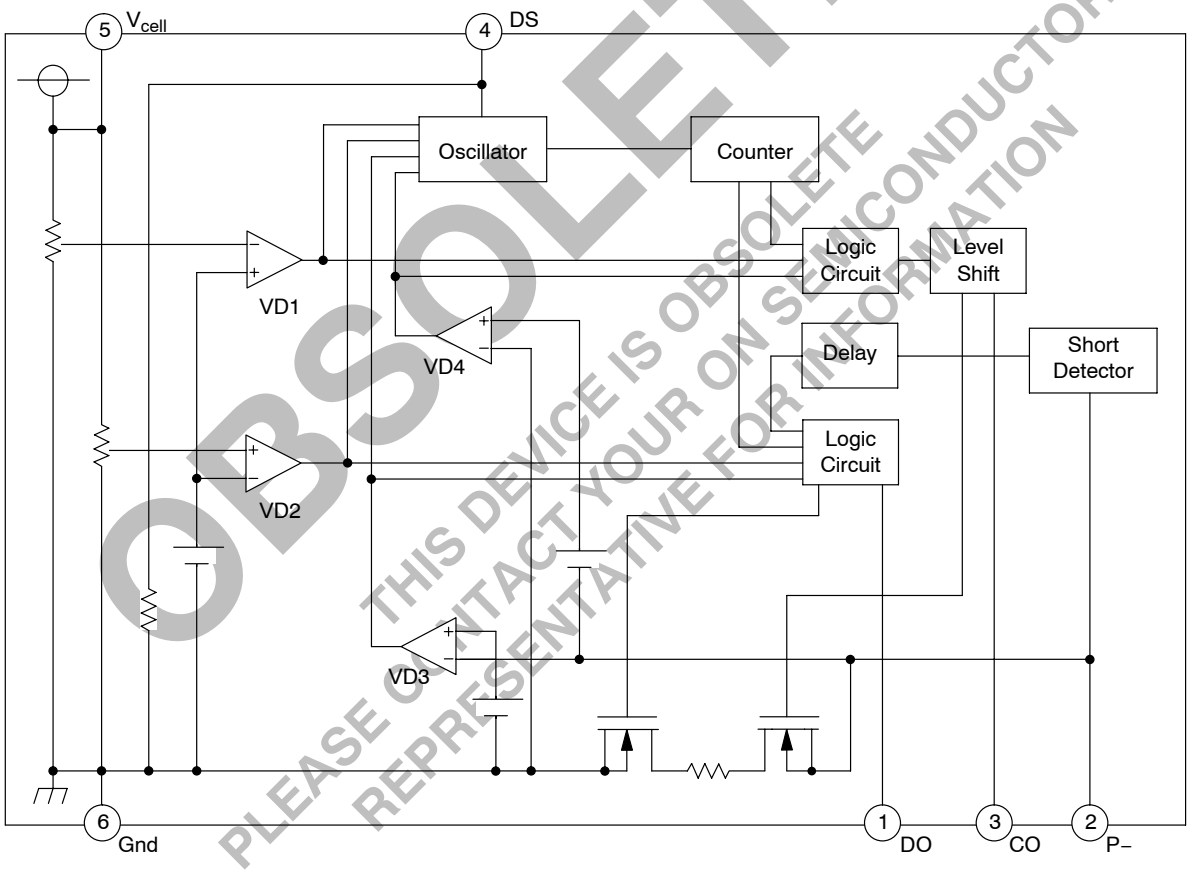


Figure 2. Detailed Block Diagram

PIN FUNCTION DESCRIPTION

Pin # SOT23−6	Pin # SON−6	Symbol	Description
1	1	DO	This output connects to the gate of the discharge MOSFET allowing it to enable or disable battery pack discharging.
2	6	P−	This is the charger negative input pin. It connects to the excess current detectors and serves as the common node for the CO pin during turn−off.
3	5	CO	This output connects to the gate of the charge MOSFET switch allowing it to enable or disable battery pack charging.
4	4	DS	This is the delay time reduction pin.
5	2	V_{cell}	This input connects to the positive terminal of the cell for voltage monitoring and provides operating bias for the integrated circuit.
6	3	Gnd	This is the ground pin of the IC.

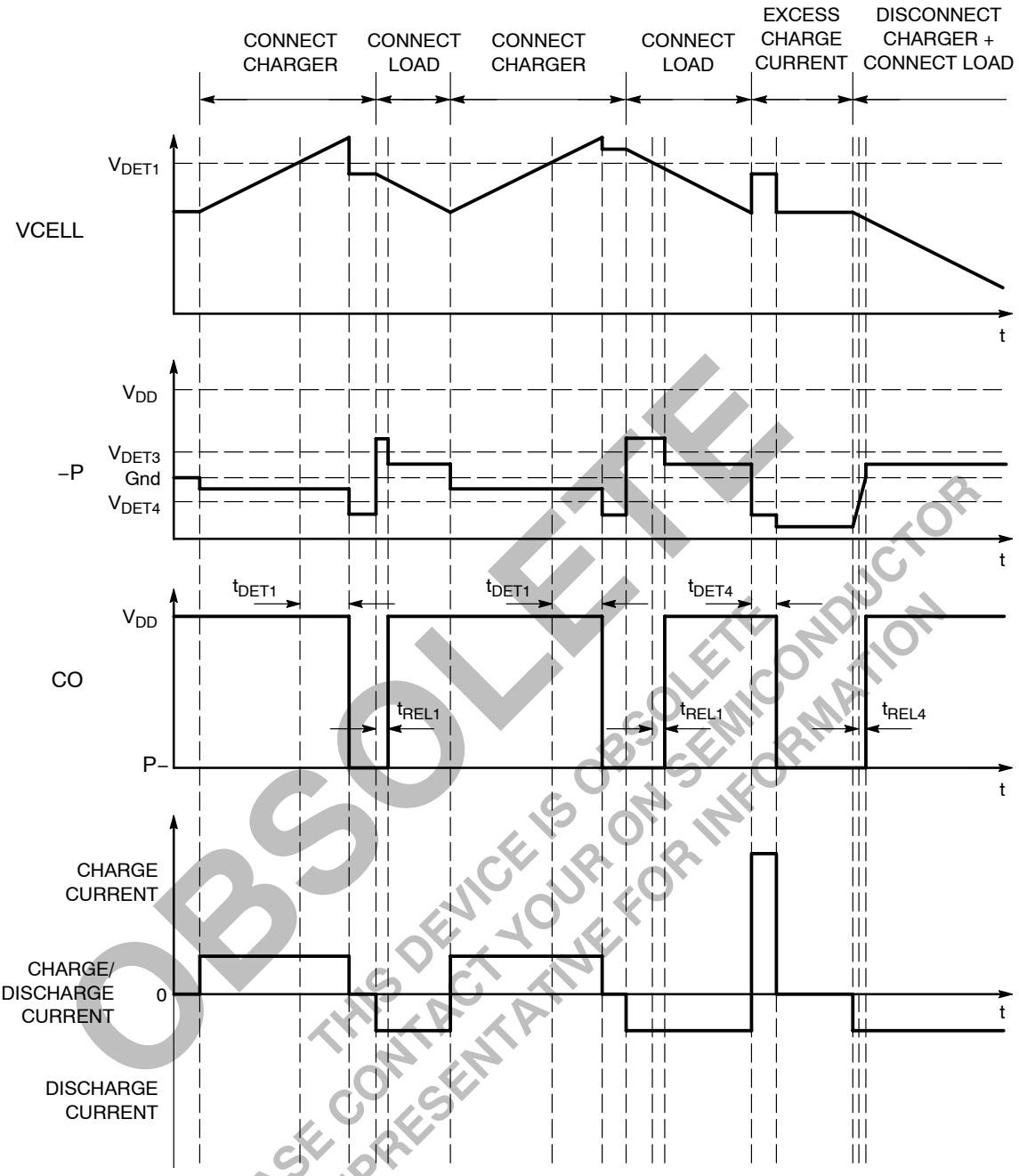


Figure 3. Overvoltage/Excess Charge Current Timing Chart

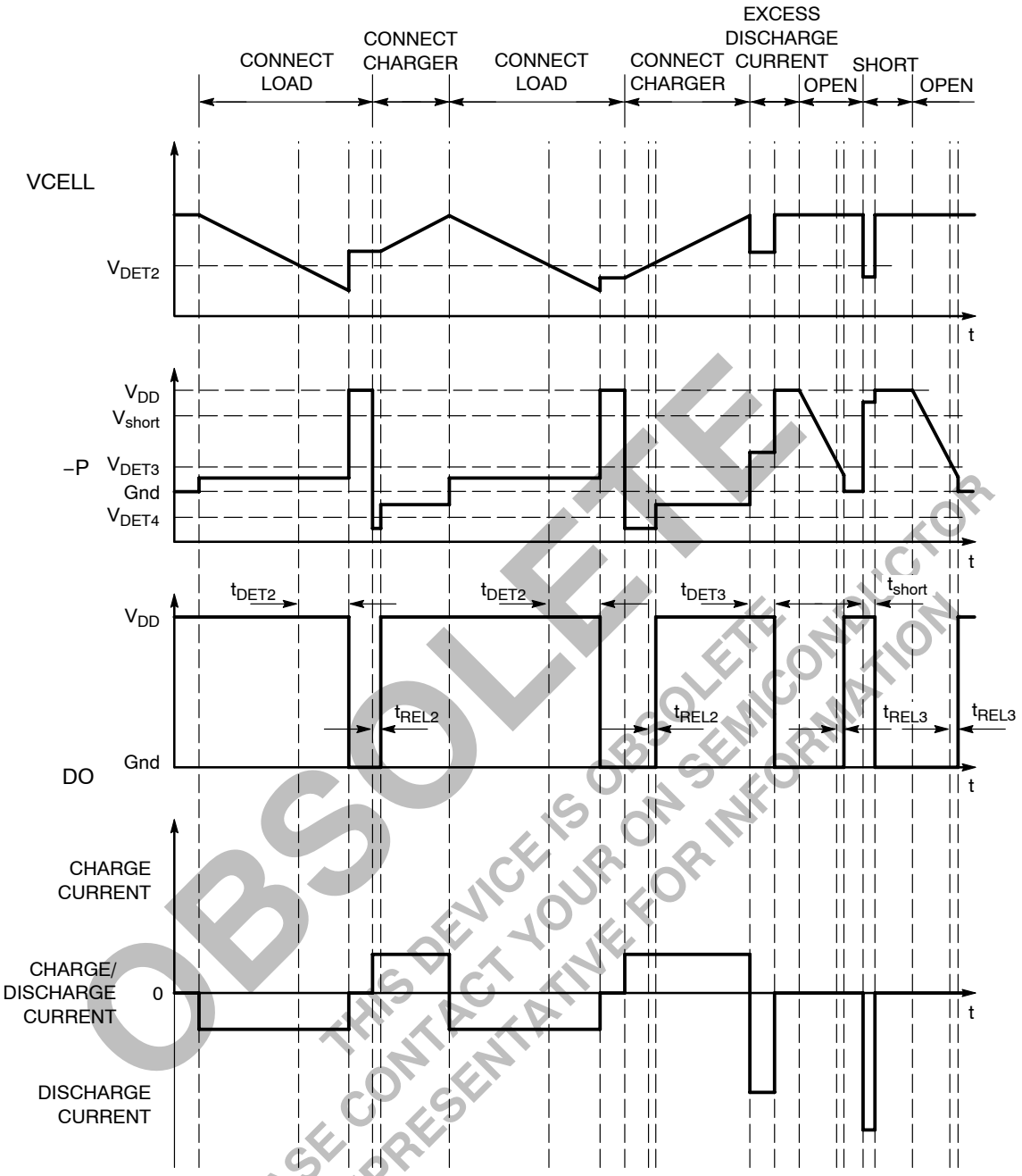


Figure 4. Undervoltage/Excess Discharge Current Timing Chart

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (Pin 5 to Pin 6)	V_{DD}	−0.3 to 12	V
Input Voltage P− Pin Voltage (Pin 5 to Pin 2) DS Pin Voltage (Pin 4 to Pin 6)	 V_{P-} V_{DS}	 V_{DD} + 0.3 to V_{DD} − 28 −0.3 to 12	 V V
Output Voltage CO Pin Voltage (Pin 3 to Pin 2) DO Pin Voltage (Pin 1 to Pin 6)	 V_{CO} V_{DO}	 V_{DD} + 0.3 to V_{DD} − 28 −0.3 to 12	 V V
Power Dissipation	P_D	150	mW
Operating Ambient Temperature Range	T_A	−40 to 85	°C
Storage Temperature	T_{stg}	−55 to 125	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

ATTRIBUTES

Characteristics		Value
ESD Protection Human Body Model (HBM) Machine Model (MM)	 (C = 100 pF, R = 1.5 kΩ) (C = 200 pF, R = 0 Ω)	 ≤1 kV ≤150 V
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)		Level 1
Latch−up Current Maximum Rating per JEDEC standard JESD78		≤150 mA

1. For additional Moisture Sensitivity information, refer to Application Note AND8003/D.

ELECTRICAL CHARACTERISTICS

(T_A = 25°C, for min/max values T_A is the operating junction temperature that applies, unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit	Note 2
VOLTAGE SENSING							
Cell Charging Cutoff (Pin 5 to Pin 6) Overvoltage Threshold, V_{DD} Increasing (R1 = 330 Ω)		V_{DET1}					
T_A = 25°C	SN1/SAN1T1		4.325	4.35	4.375	V	
T_A = −5°C to 55°C	SN1/SAN1T1		4.32	4.35	4.38	V	A
T_A = 25°C	SAN5T1		4.25	4.275	4.30	V	
T_A = −5°C to 55°C	SAN5T1		4.245	4.275	4.305	V	A
T_A = 25°C	SAN6T1		4.255	4.28	4.305	V	
T_A = −5°C to 55°C	SAN6T1		4.25	4.28	4.31	V	A
Overvoltage Delay Time (V_{DD} = 3.6 V to 4.4 V)	SN1/SAN1T1/SAN6T1	t_{DET1}	0.175	0.250	0.325	s	A
	SAN5T1		0.7	01.0	1.3		
Overvoltage Release Time (V_{DD} = 4.0 V, V_{P-} = 0 V to 1.0 V)		t_{REL1}	11	16	21	ms	B
Cell Discharging Cutoff (Pin 5 to Pin 6) Undervoltage Threshold, V_{DD} Decreasing		V_{DET2}				V	C
	SN1/SAN1T1		2.34	2.4	2.46		
	SAN5T1/SAN6T1		2.24	2.3	2.36		
Undervoltage Time (V_{DD} = 3.6 V to 2.2 V)		t_{DET2}	14	20	26	ms	C
Undervoltage Release Delay Time (V_{DD} = 3.0 V, V_{P-} = 3.0 V to 0 V)		t_{REL2}	0.7	1.2	1.7	ms	D
CURRENT SENSING							
Excess Discharge Current Threshold, V_{P-} Increasing		V_{DET3}				V	K
	SN1T1/SAN1T1/SAN6T1		0.180	0.200	0.220		
	SAN5T1		0.080	0.100	0.120		
Excess Discharge Current Delay Time (V_{DD} = 3.0 V, V_{P-} = 0 V to 1.0 V)	SN1T1/SAN1T1/SAN6T1	t_{DET3}	8.0	12	16	ms	K
	SAN5T1		4.0	6.0	8.0		
Excess Discharge Current Release Time (V_{DD} = 3.0 V, V_{P-} = 3.0 V to 0 V)		t_{REL3}	0.7	1.2	1.7	ms	K
Excess Charge Current Threshold, V_{P-} Decreasing		V_{DET4}	−0.13	−0.1	−0.07	V	E
Excess Charge Current Delay Time (V_{DD} = 3.0 V, V_{P-} = 0 V to −1.0 V)	SN1T1/SAN1T1/SAN6T1	t_{DET4}	11	16	21	ms	E
	SAN5T1		5.0	8.0	11		
Excess Charge Current Release Time (V_{DD} = 3.0 V, V_{P-} = −1.0 V to 0 V)		t_{REL4}	0.7	1.2	1.7	ms	E
Short Protection Voltage (V_{DD} = 3.0 V)		V_{SHORT}	V_{DD} −1.4	V_{DD} −1.1	V_{DD} −0.8	V	K
Short Protection Delay Time (V_{DD} = 3.0 V, V_{P-} = 0 V to 3.0 V)		t_{SHORT}	250	400	600	μs	K
Reset Resistance (V_{DD} = 3.6 V, V_{P-} = 1.0 V)		R_{SHORT}	15	30	45	kΩ	K

2. Indicates test circuits shown on pages 16 and 17.

ELECTRICAL CHARACTERISTICS

(T_A = 25°C, for min/max values T_A is the operating junction temperature that applies, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit	Note 3
OUTPUTS						
Charge Gate Drive Output Low (Pin 3 to Pin 2) (V_{DD} = 4.5 V, I_o = 50 μA)	V_{ol1}	–	0.4	0.5	V	G
Charge Gate Drive Output High (Pin 5 to Pin 3) (V_{DD} = 3.9 V, I_o = −50 μA)	V_{oh1}	3.4	3.7	–	V	H
Discharge Gate Drive Output Low (Pin 1 to Pin 6) (V_{DD} = 2.0 V, I_o = 50 μA)	V_{ol2}	–	0.2	0.5	V	I
Discharge Gate Drive Output High (Pin 5 to Pin 1) (V_{DD} = 3.9 V, I_o = −50 μA)	V_{oh2}	3.4	3.7	–	V	J
DELAY SHORTENING (DS PIN)						
DS Pin High Input Voltage	V_{IH}	V_{DD} −0.5	–	V_{DD} +0.3	V	F
DS Pin Middle Input Voltage (V_{DD} = 3.6 to 4.4 V)	V_{IM}	1.05	–	V_{DD} −1.1	V	F
DS Pin Pull−down Resistance (V_{DD} = 3.6 V)	RDS	0.5	1.3	2.5	MΩ	F
TOTAL DEVICE						
Supply Current Operating (V_{DD} = 3.9 V, V_{P-} = 0 V) Standby (V_{DD} = 2.0 V)	I_{cell}	 – –	 3.0 –	 6.0 0.1	 μA μA	L
Operating Voltage	V_{DD}	1.5	–	5.0	V	–
Minimum Operating Cell Voltage for Zero Volt Charging (Pin 5 to Pin 2) (V_{DD} − Gnd = 0 V)	V_{ST}	–	–	1.5	V	M

3. Indicates test circuits shown on pages 16 and 17.

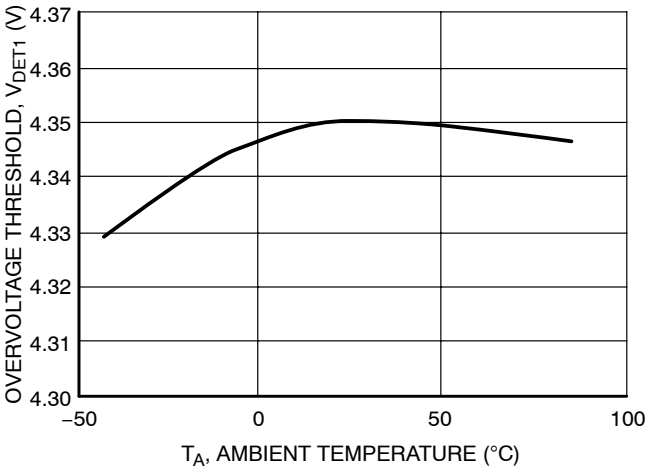


Figure 5. Overvoltage Threshold vs. Temperature

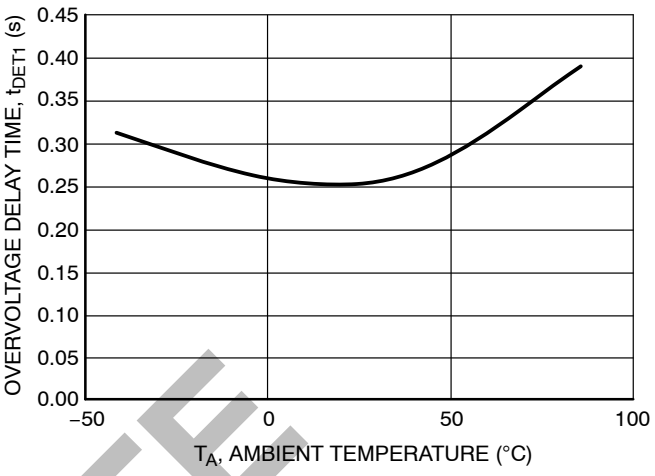


Figure 6. Overvoltage Delay Time vs. Temperature

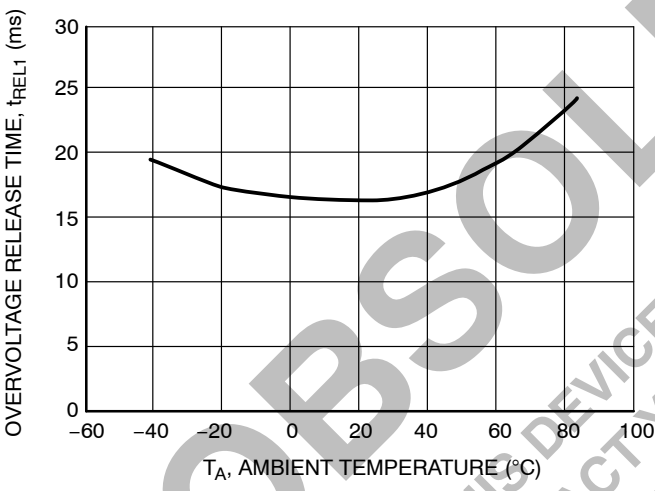


Figure 7. Overvoltage Release Time vs. Temperature

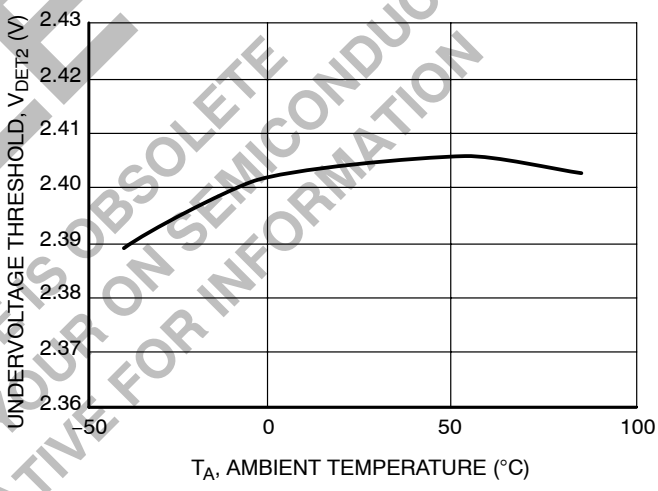


Figure 8. Undervoltage Threshold vs. Temperature

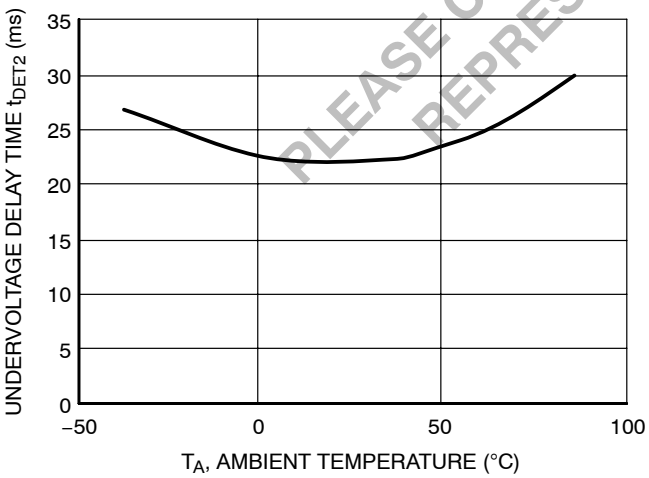


Figure 9. Undervoltage Delay Time vs. Temperature

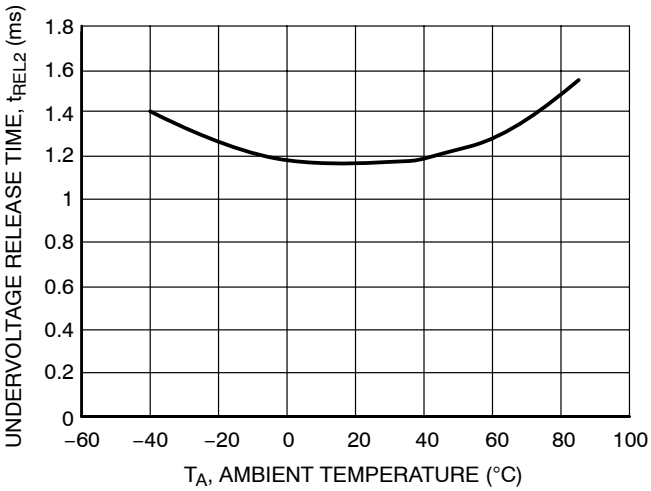


Figure 10. Undervoltage Release Time vs. Temperature

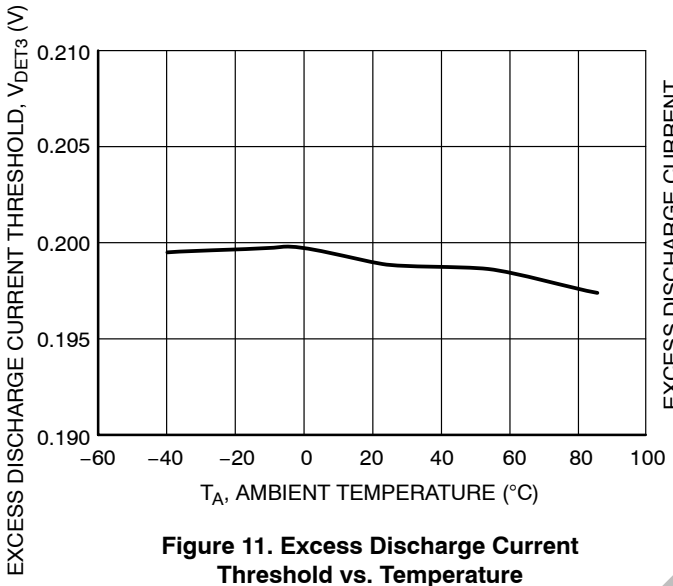


Figure 11. Excess Discharge Current Threshold vs. Temperature

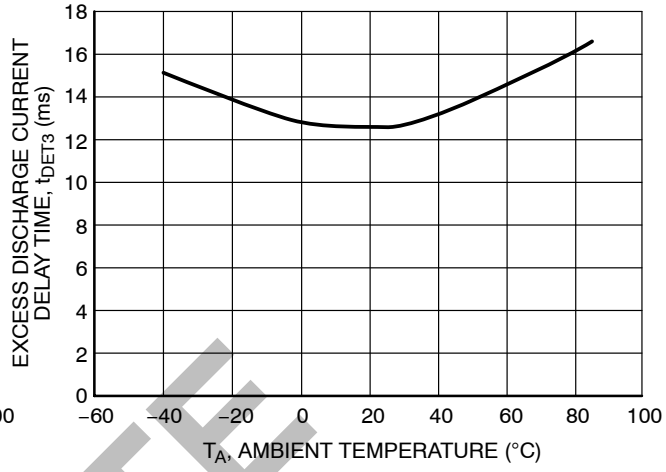


Figure 12. Excess Discharge Current Delay Time vs. Temperature

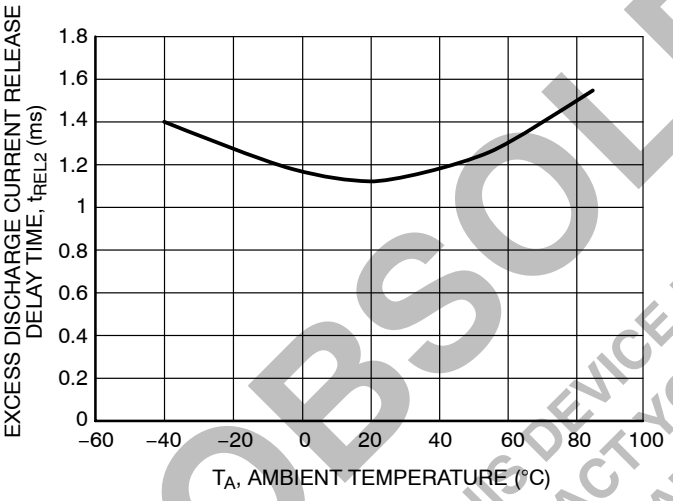


Figure 13. Excess Discharge Current Release Time vs. Temperature

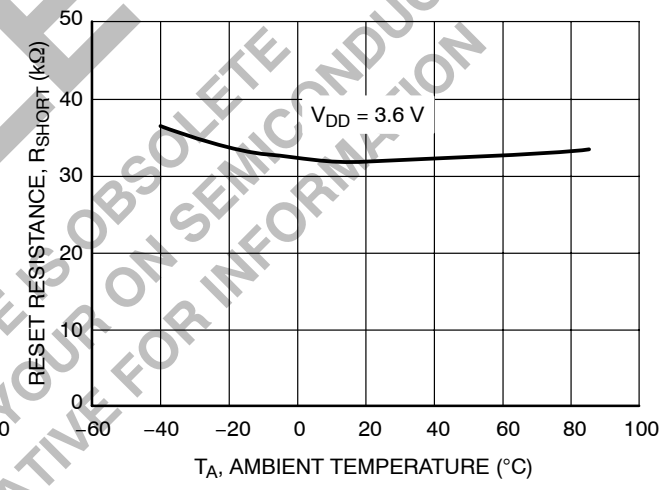


Figure 14. Reset Resistance vs. Temperature

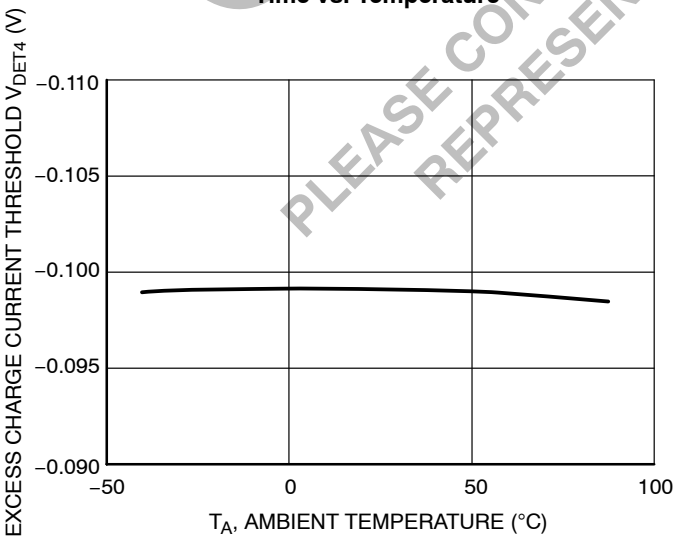


Figure 15. Excess Charge Current Threshold vs. Temperature

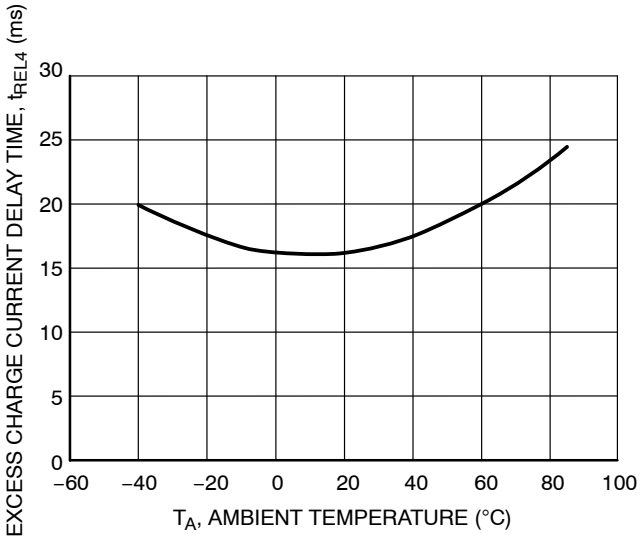


Figure 16. Excess Charge Current Delay Time vs. Temperature

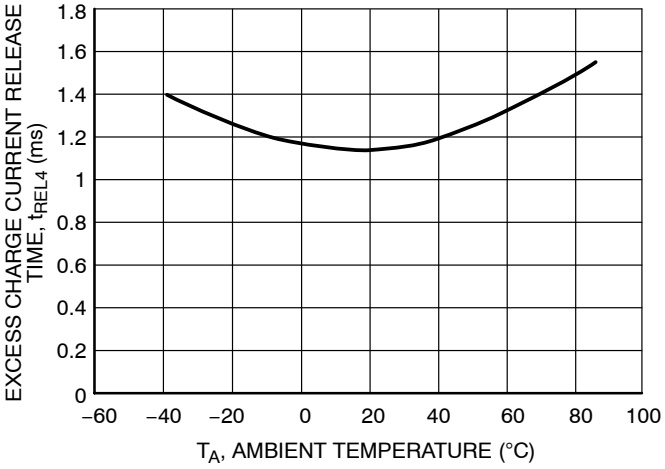


Figure 17. Excess Charge Current Release Time vs. Temperature

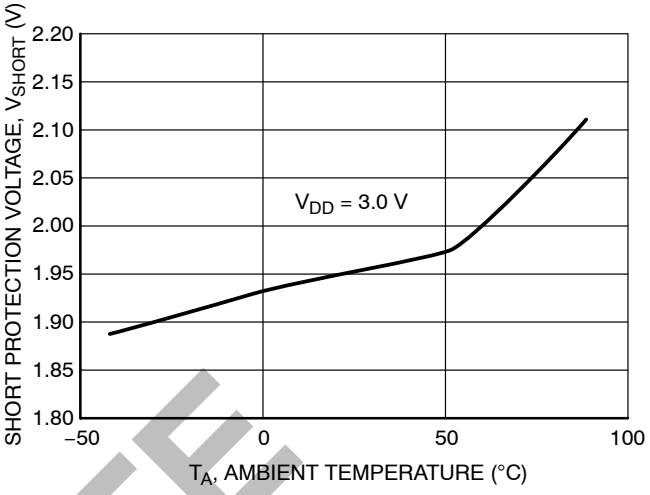


Figure 18. Short Protection Threshold vs. Temperature

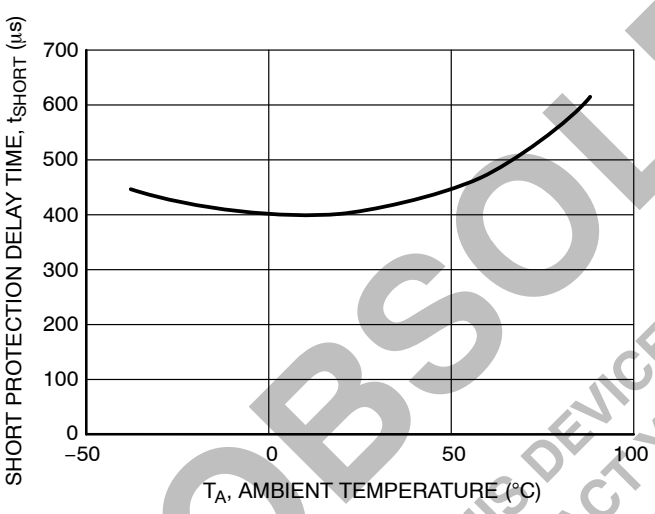


Figure 19. Short Protection Delay Time vs. Temperature

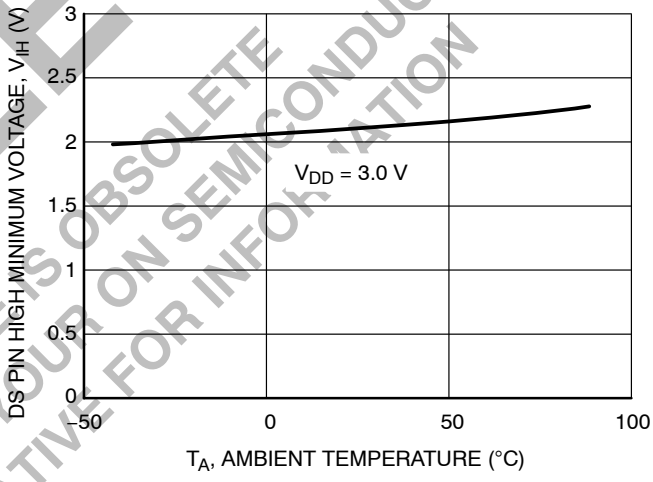


Figure 20. DS Pin High Input Minimum Voltage vs. Temperature

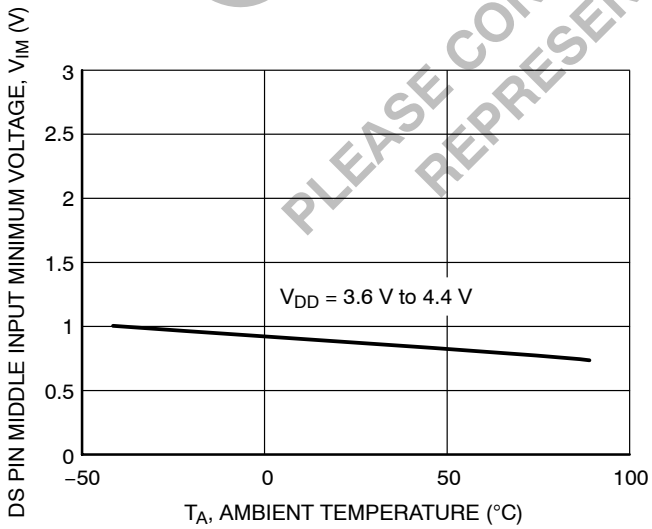


Figure 21. DS Pin Middle Input Minimum Voltage vs. Temperature

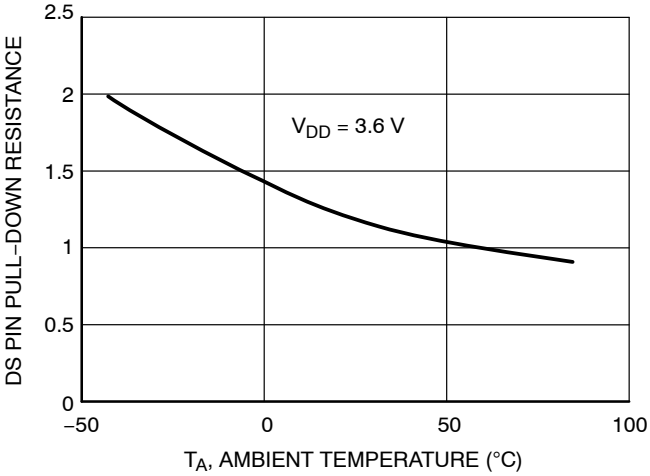


Figure 22. DS Pin Pull−Down Resistance vs. Temperature

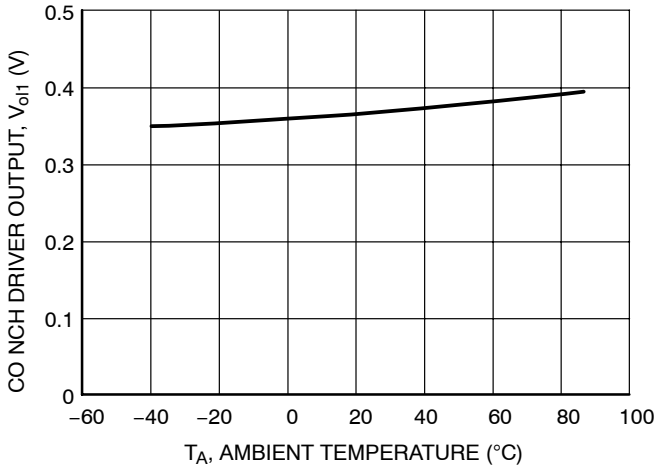


Figure 23. CO NCH Driver Output vs. Temperature

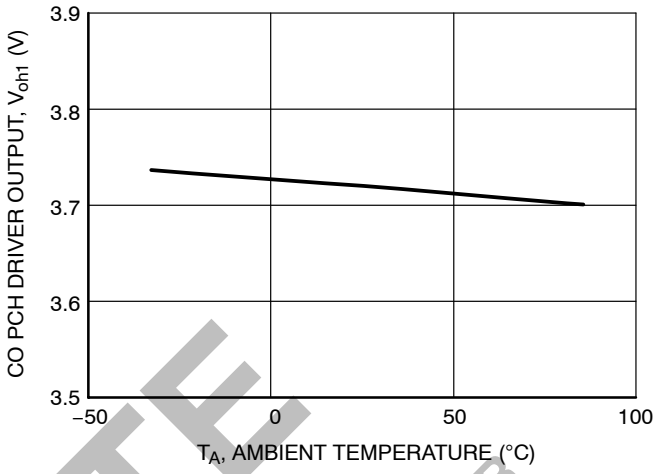


Figure 24. CO PCH Driver Output vs. Temperature

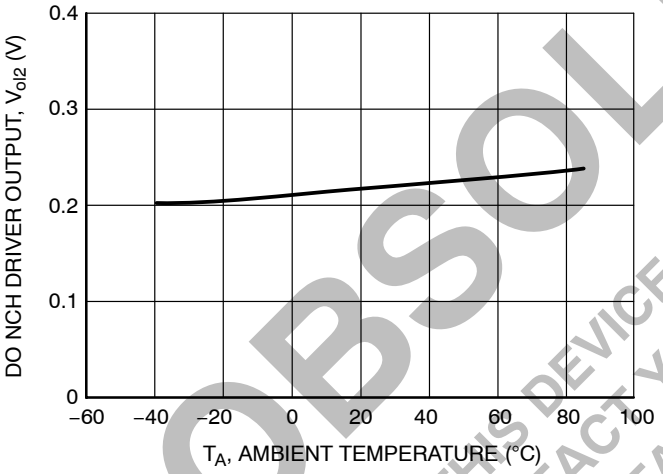


Figure 25. DO NCH Driver Output vs. Temperature

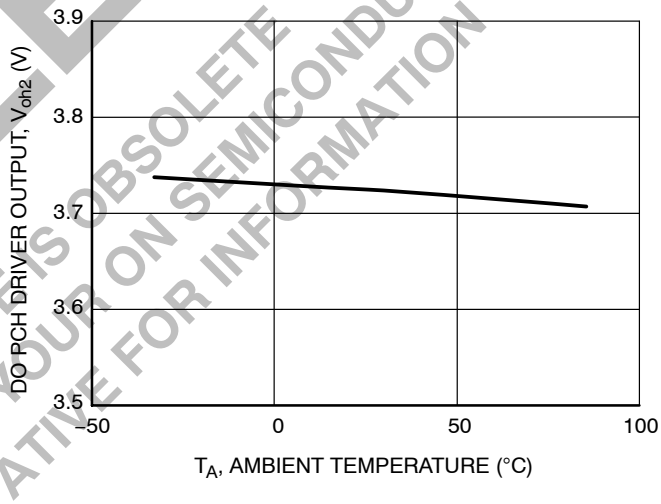


Figure 26. DO PCH Driver Output vs. Temperature

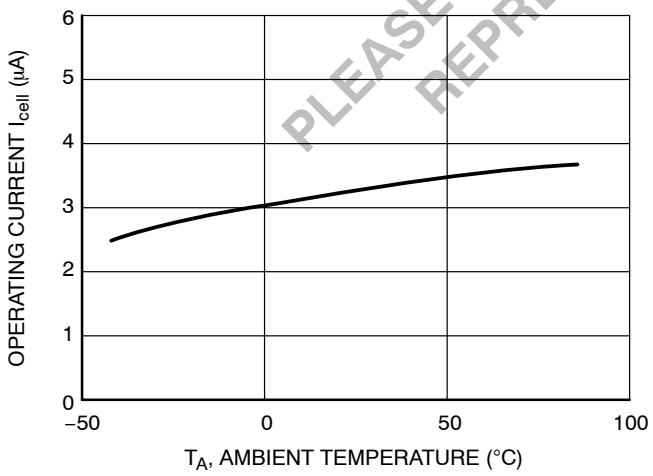


Figure 27. Operating Current vs. Temperature

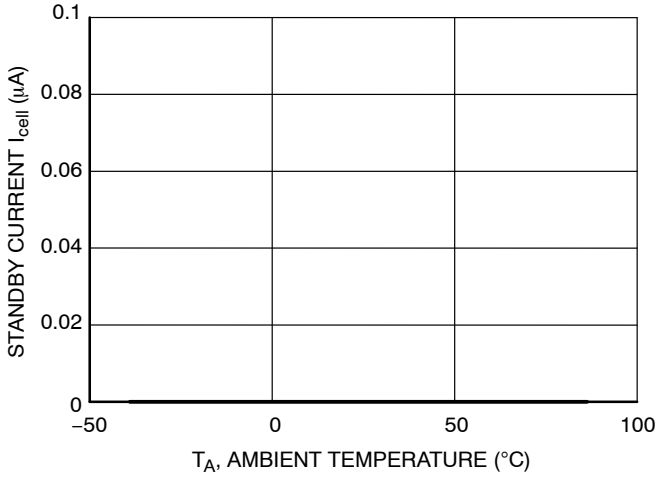


Figure 28. Standby Current vs. Temperature

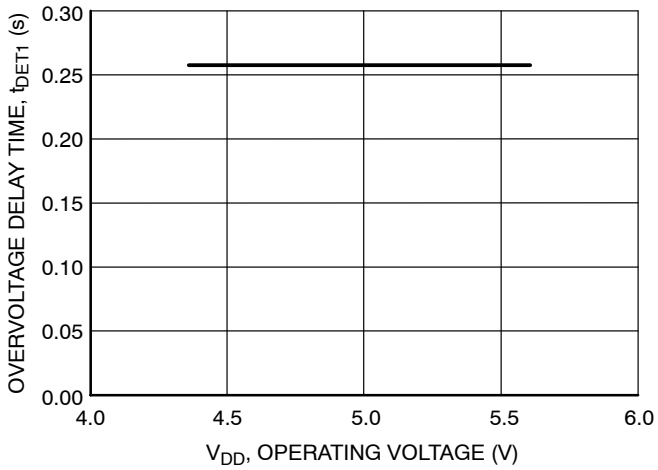


Figure 29. Overvoltage Delay Time vs. Operating Voltage

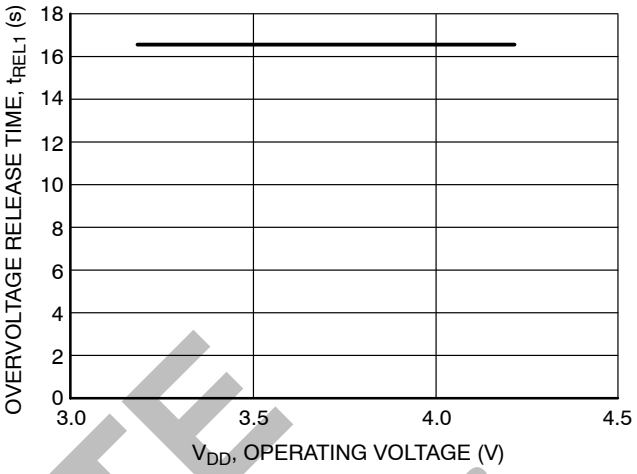


Figure 30. Overvoltage Release Time vs. Operating Voltage

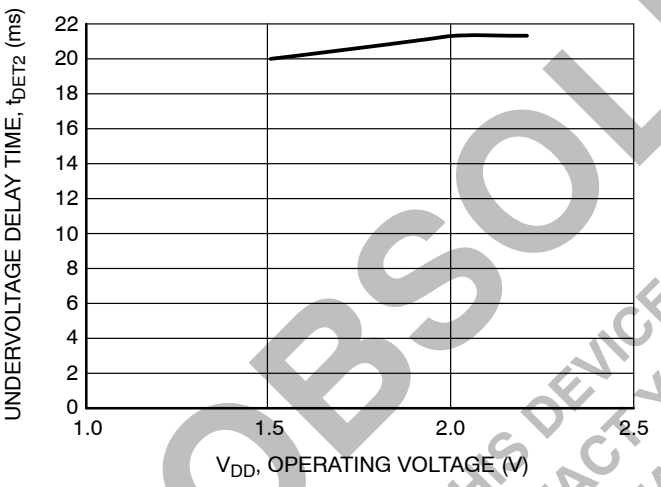


Figure 31. Undervoltage Delay Time vs. Operating Voltage

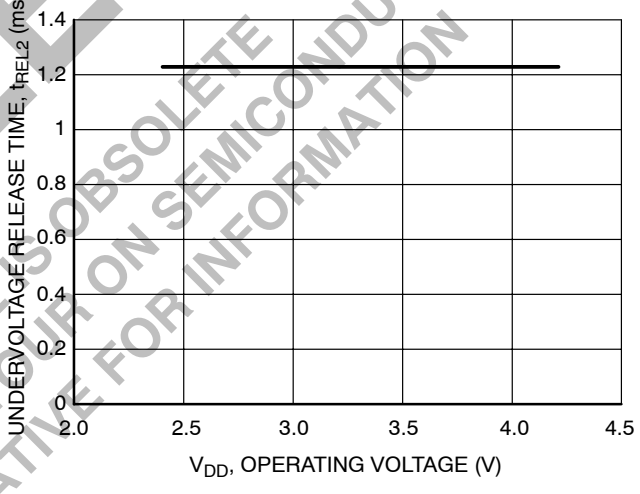


Figure 32. Undervoltage Release Time vs. Operating Voltage

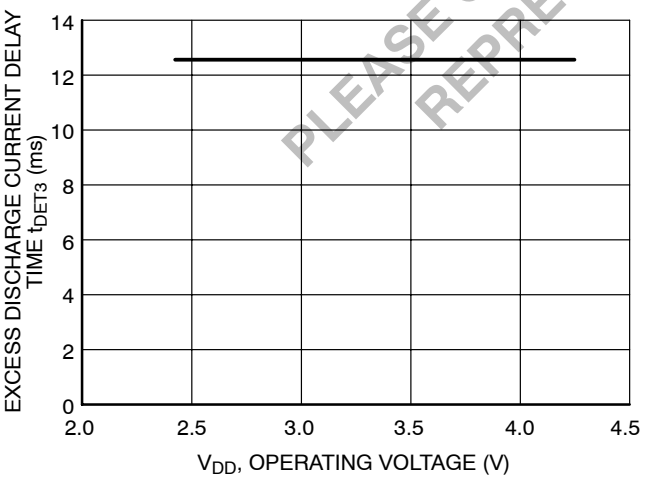


Figure 33. Excess Discharge Current Delay Time vs. Operating Voltage

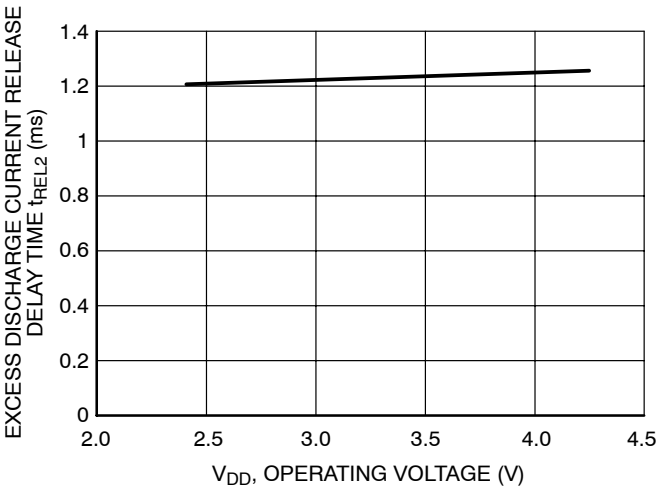


Figure 34. Excess Discharge Current Release Time vs. Operating Voltage

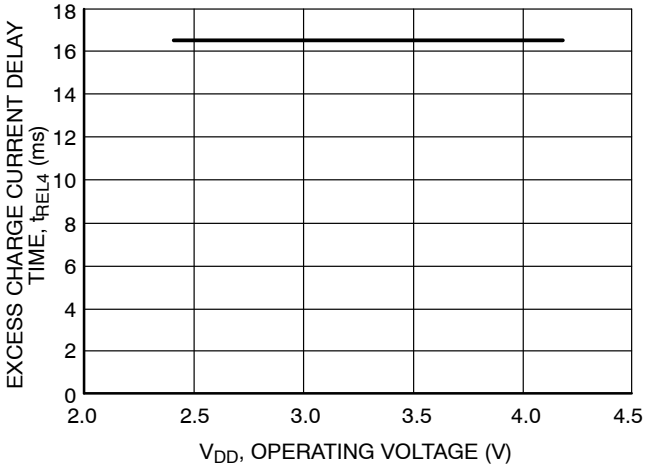


Figure 35. Excess Charge Current Delay Time vs. Operating Voltage

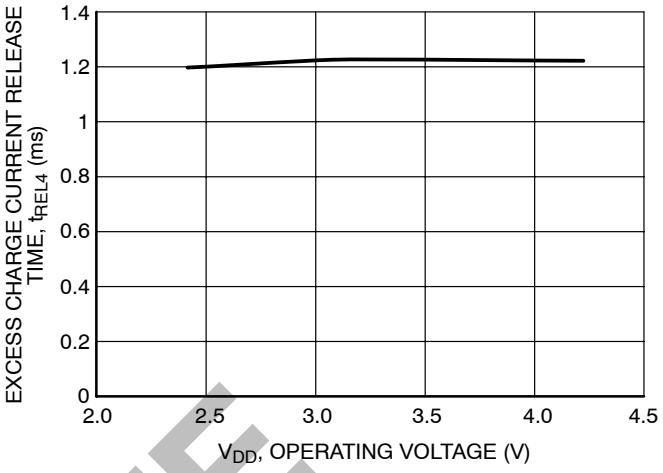


Figure 36. Excess Charge Current Release Time vs. Operating Voltage

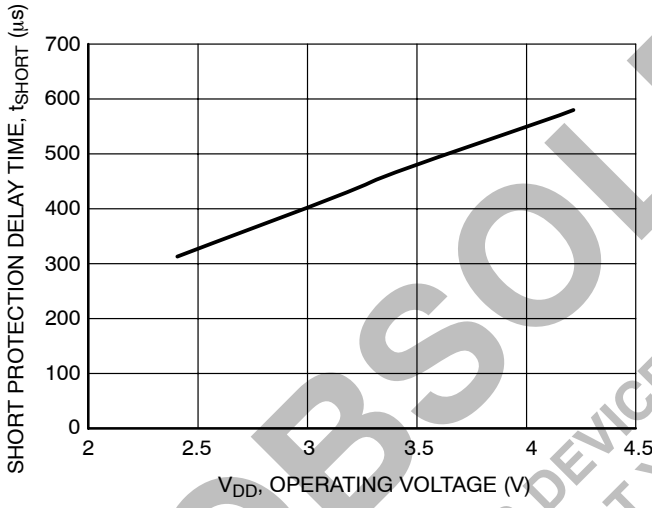


Figure 37. Short Protection Delay Time vs. Operating Voltage

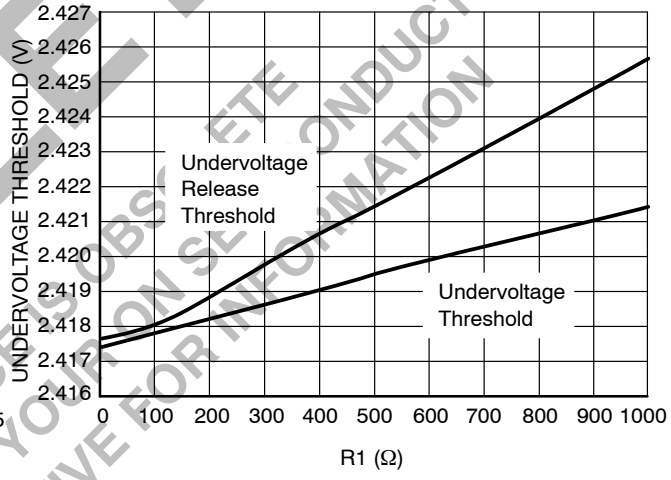


Figure 38. Undervoltage Thresholds vs. R1

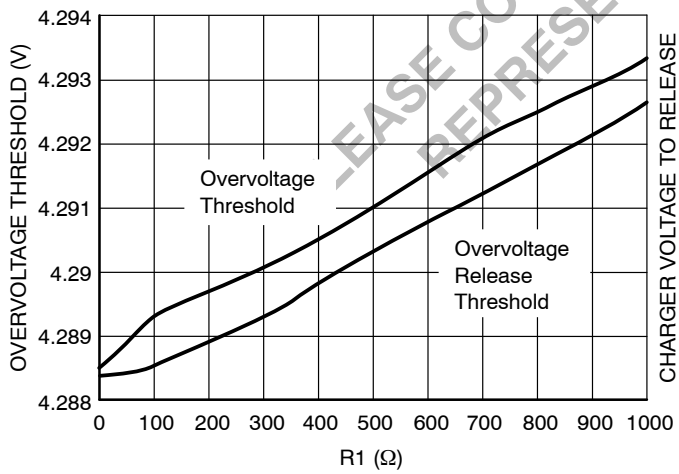


Figure 39. Overvoltage Thresholds vs. R1

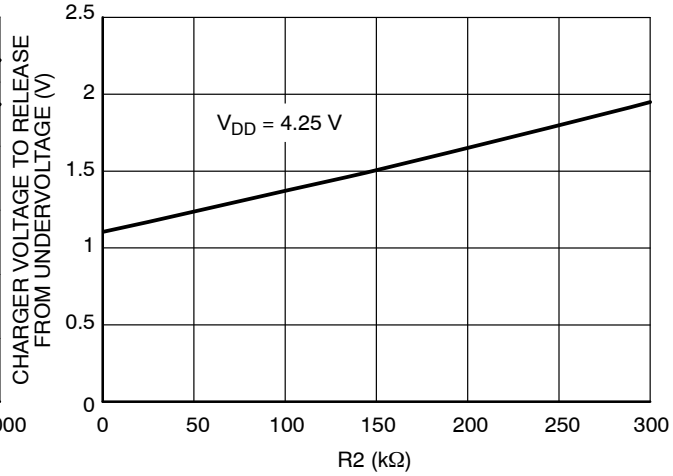


Figure 40. Charger Voltage to Release from Undervoltage vs. R2

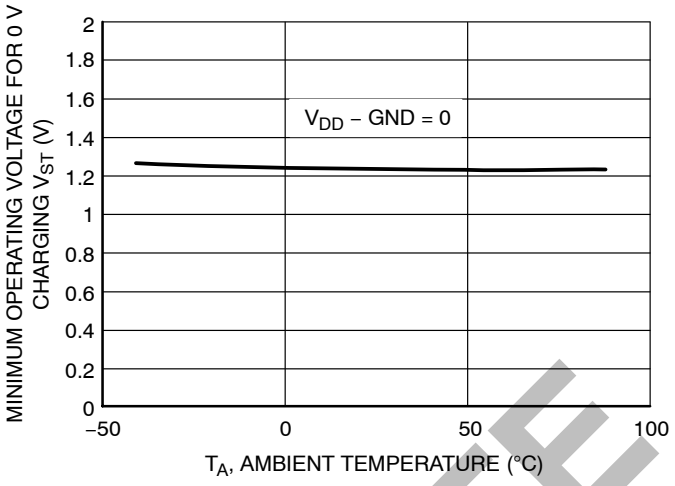


Figure 41. Minimum Operating Voltage for 0 V Charging vs. Temperature

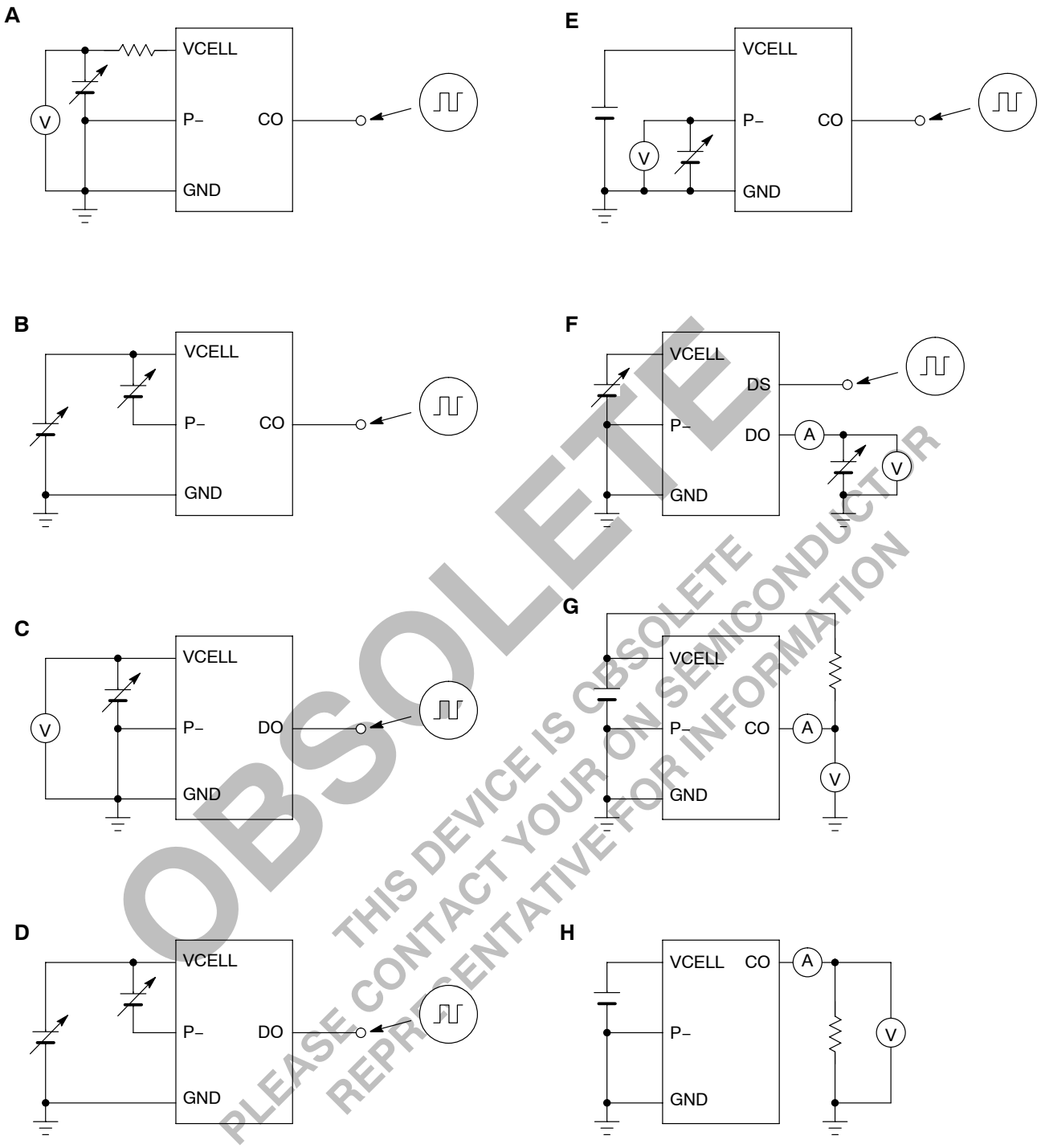


Figure 42. Test Circuits

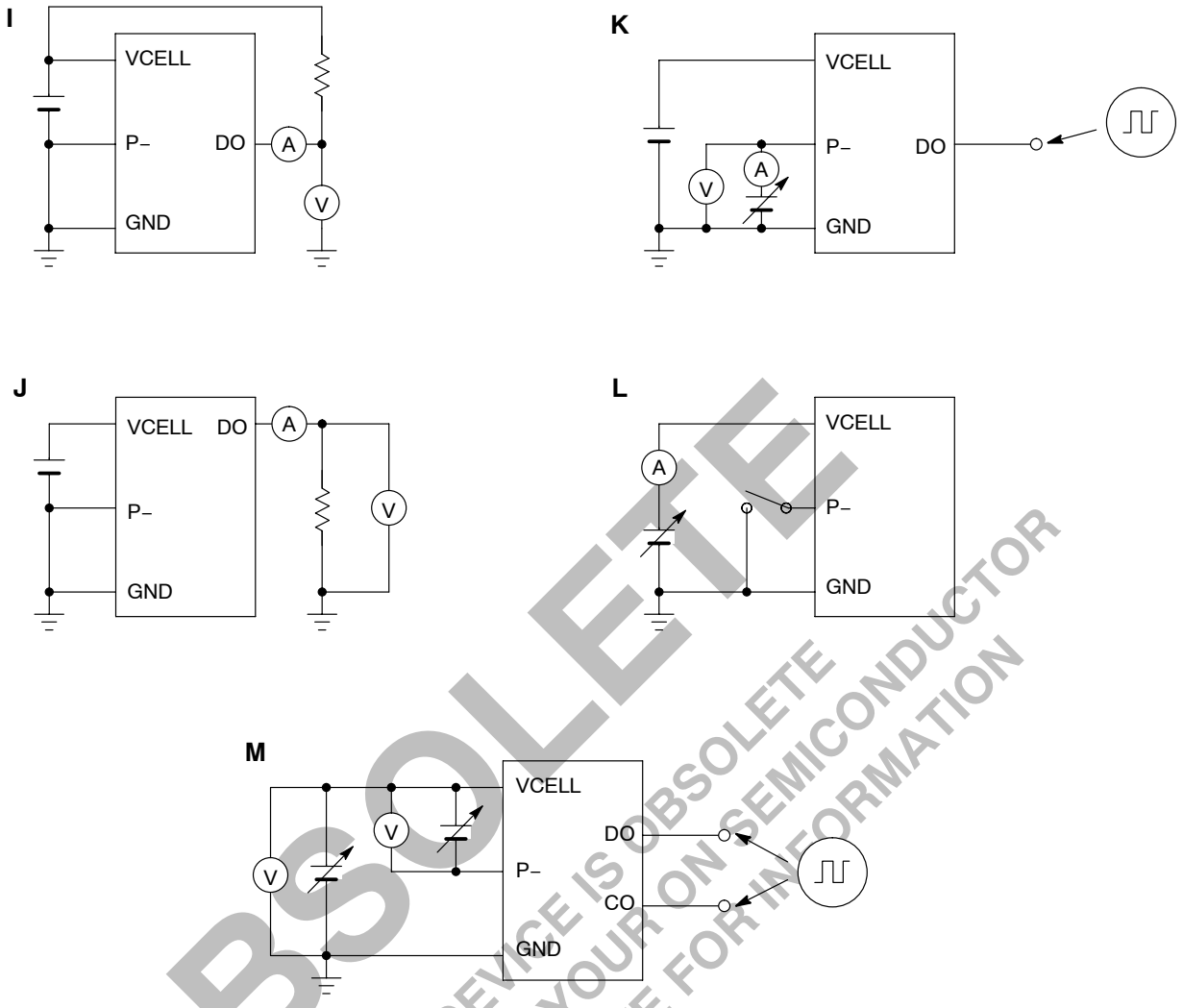


Figure 43. Test Circuits

Overvoltage Detection

The overvoltage detector (VD1) monitors the VCELL pin voltage. When the VCELL voltage crosses the overvoltage detector threshold (VDET1) from a low value to a value higher than VDET1, VD1 detects an over−charging condition. The NCP802 then turns off an external, charge control, N−channel, MOSFET by driving the CO pin to its low level. A level shifter, incorporated in a buffer driver for the CO pin, drives the low level of the CO pin to the P− pin voltage, which is connected to the source of the charge control MOSFET by a resistor. The high level of the CO pin is driven to the VCELL voltage with a CMOS buffer.

To reset the CO pin to its high level, the voltage at the VCELL pin must decrease to a level lower than VDET1. The overvoltage detector does not reset after the battery voltage falls below some hysteresis voltage. The NCP802 will not reset from an overvoltage fault as long as a charger is connected to the battery. Rather, the excess−discharge current detector (VD3) signals the IC to reset from an overvoltage condition by detecting a load while in an overvoltage condition. When the P− pin voltage becomes equal to or greater than than the excess discharge−current detector threshold (VDET3) during an overvoltage fault, the NCP802 senses the voltage drop across the charge MOSFET's body diode induced by the load current. It then resets from the overvoltage state.

There are internal, fixed delay times for both the detection and release from an overvoltage condition. If the fault or reset conditions are shorter than their respective delay times, the NCP802 ignores that condition and stays in its previous state.

Undervoltage Detection

The undervoltage detector (VD2) monitors the VCELL pin voltage. When the VCELL voltage crosses the undervoltage threshold (VDET2) from a high value to a value lower than VDET2, VD2 senses an undervoltage condition, and an external, discharge control, N−channel MOSFET turns off by driving the DO pin to its low level. The low level of DO is set to GND and the high level to VCELL.

To reset the DO pin to its high level, one must connect a charger to the battery pack. While the VCELL voltage remains under VDET2, charge−current can flow through the parasitic diode of the external discharge control MOSFET. Once the VCELL voltage rises above VDET2, the NCP802 drives DO high. Connecting a charger to the battery pack drives the DO level high instantaneously when the VCELL voltage is higher than VDET2. VD2 has no hysteresis.

After VD2 detects an undervoltage condition, the NCP802 enters a low supply current, standby mode. Maximum standby current equals 0.1 μA at VCELL equal to 2.0 V. An internal pull−up disables all the device functions and thus drastically lowers quiescent current. When the charger connects to the battery, it pulls small levels of current from the P− pin. This overcomes the internal pull−up and allows the NCP802 to reset.

There are internal, fixed delay times for both the detection and release from an undervoltage condition. If the fault or reset conditions are shorter than their respective delay times, the NCP802 ignores that condition and stays in its previous state.

Excess Discharge−Current/Short Circuit Detection

The excess discharge−current detector (VD3) and the short circuit detector can function when the control MOSFET's are on. When the P− pin voltage is below the short circuit detection voltage (VSHORT) and above the excess discharge−current threshold (VDET3), VD3 operates. When the P− pin voltage rises higher than VSHORT, the NCP802 enables the short circuit detector. When either detector activates, the NCP802 turns off an external, discharge control, N−channel, MOSFET by driving the DO pin to its low level.

The output delay time for the excess discharge−current detector is internally fixed. If the P− pin, voltage level recovers from a level between VSHORT and VDET3 within the delay time, the discharge MOSFET stays in its high state. Output delay time for release from excess discharge−current detection is typically 1.2 ms. When the short circuit detector activates, DO transitions to its low state after a delay time of approximately 400 μs.

There is an integrated pull−down resistor (RSHORT) connected between the P− and GND pins. After VD3 or the short circuit detector has activated; removing the cause of that activation turns the discharge MOSFET back on. This occurs because RSHORT pulls the P− pin, voltage level down to the GND pin, voltage level. The NCP802 internally disconnects RSHORT during a normal, fault−free, state. The NCP802 only connects RSHORT if it has detected an excess discharge−current or short circuit fault. In other words, VD3 is automatically released from excess discharge−current and short circuit faults when the user removes the load.

The output delay time of excess discharge−current detection is set shorter than the delay time for undervoltage detection. Therefore, if VCELL voltage drops below VDET2 during an excess discharge−current or short circuit fault, the NCP802 detects the current fault first. This prevents large discharge current faults from activating the undervoltage detector and putting the NCP802 into standby mode. Standby mode requires the charger to reset the NCP802, while excess discharge−current and short circuit faults only require that the fault be removed.

Excess Charge−Current Detection

When the battery pack is chargeable and discharge is also possible, VD4 senses the P− pin voltage. For example, if the user connects the battery to an inappropriate charger, excess current can flow. Then, the P− voltage drops below the excess charge−current threshold (VDET4). Next, the output of CO becomes low. This prevents excess current flow into the circuit by turning off the external MOSFET.

The output delay of the excess charge−current detector is internally fixed. If the fault condition is within the delay time window, the detector will not sense it and the MOSFET will not change state. VD4 can be released by disconnecting a charger and applying a load.

Delay Shortening Function

The output delay time of over−charge, over−discharge, excess discharge−current, excess charge−current, and the release from those detecting modes can be made shorter than the pre−set value by forcing the VCELL voltage to the DS pin. When one forces the specified middle range voltage to the DS pin, the output delay circuit becomes disabled. Therefore, under this condition, when over−charge or excess charge current is detected, output level can be checked without waiting for the delay.

A 1.3 MΩ pull−down resistor is connected between DS pin and GND internally. For normal operation, the DS pin should be at no connection state.

Zero Battery Voltage Charging

If the charger voltage is equal or higher than the zero−volt charge, minimum voltage (VST), the NCP802 drives the CO pin high. Therefore, it allows charging for batteries as low as zero volts.

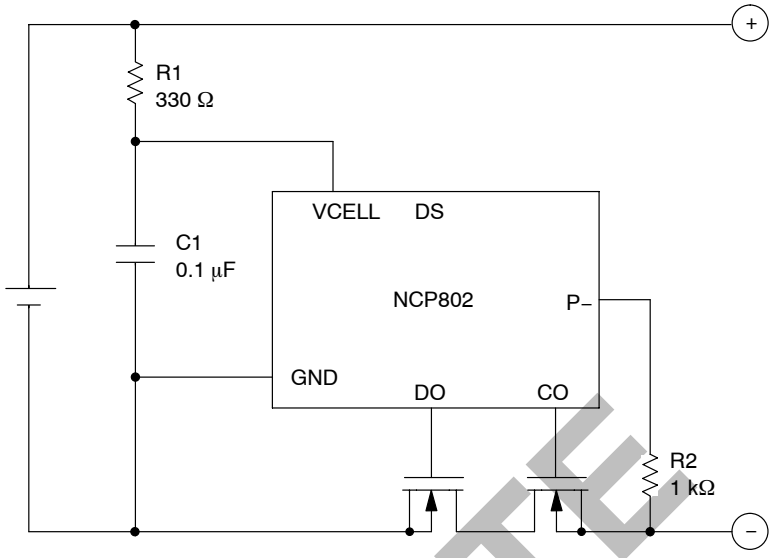


Figure 44. Typical Application Circuit

Technical Notes

R1 and C1 will stabilize a supply voltage to the NCP802. A recommended R1 value is less than 1.0 kΩ A larger value of R1 leads to higher detection voltages. There may also be voltage detector errors from shoot through current into the NCP802. R1 and R2 can also help current limit the circuit against reverse charge or a charger with excess charging voltage applied to the NCP802 battery pack. Smaller R1 and R2 values may cause excessive power consumption over the specified power dissipation rating. Therefore, the total value of R1 + R2 should be equal to or more than 1.0 kΩ. However, if one uses a very large value of R2, it might not be possible to release from undervoltage by connecting a charger. The recommended R2 value is equal to or less than 30 kΩ.

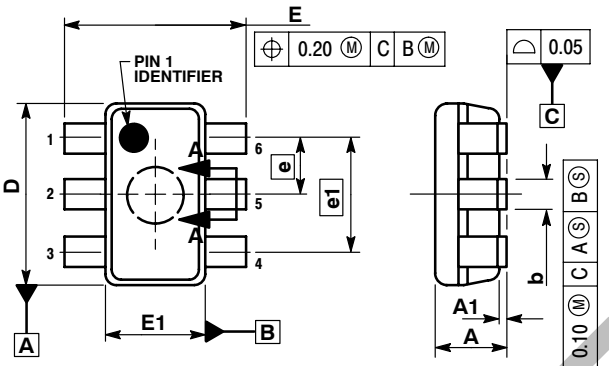
ORDERING INFORMATION

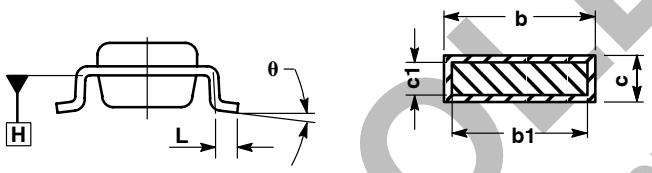
Device	Package	Marking Code	Shipping†
NCP802SN1T1	SOT23−6	KN	3000 / Tape & Reel
NCP802SN1T1G	SOT23−6 (Pb−Free)	KN	3000 / Tape & Reel
NCP802SAN1T1	SON−6	KN	3000 / Tape & Reel
NCP802SAN1T1G	SON−6 (Pb−Free)	KN	3000 / Tape & Reel
NCP802SAN5T1	SON−6	K7	3000 / Tape & Reel
NCP802SAN5T1G	SON−6 (Pb−Free)	K7	3000 / Tape & Reel
NCP802SAN6T1	SON−6	KD	3000 / Tape & Reel
NCP802SAN6T1G	SON−6 (Pb−Free)	KD	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

PACKAGE DIMENSIONS

SOT23−6
SN SUFFIX
PLASTIC PACKAGE
CASE 1262−01
ISSUE A





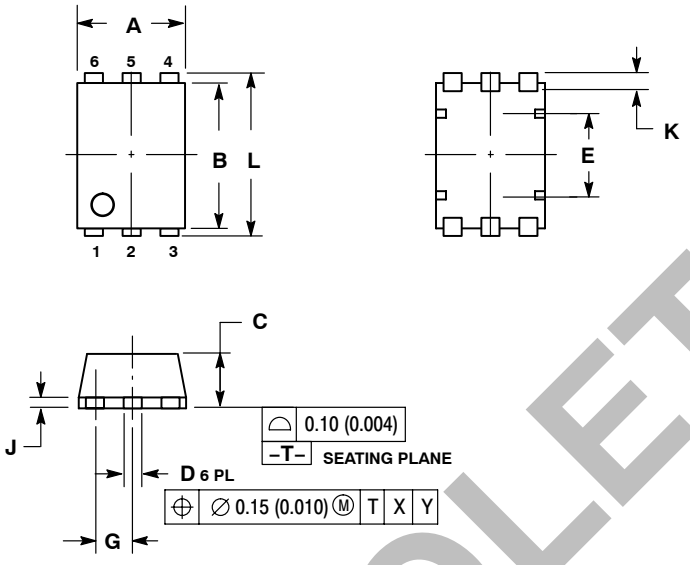
SECTION A−A

NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSION D DOES NOT INCLUDE FLASH OR PROTRUSIONS. FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.23 PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE H.

	MILLIMETERS	
DIM	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
b	0.35	0.50
b1	0.35	0.45
c	0.09	0.20
c1	0.09	0.15
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.75
e	0.95	
e1	1.90	
L	0.25	0.55
θ	0°	10°

PACKAGE DIMENSIONS

SON−6
SAN SUFFIX
PLASTIC PACKAGE
CASE 494−01
ISSUE 0



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.40	1.80	0.055	0.071
B	2.40	2.80	0.094	0.110
C	---	0.90	---	0.035
D	0.10	0.30	0.004	0.012
E	1.24	1.44	0.049	0.057
G	0.50 BSC		0.020 BSC	
J	0.08	0.18	0.003	0.007
K	0.30 BSC		0.012 BSC	
L	2.85	3.15	0.112	0.124

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