DATA SHEET
www.onsemi.com

Micropower Voltage Reference Diodes

LM285, LM385B

The LM285/LM385 series are micropower two−terminal bandgap voltage regulator diodes. Designed to operate over a wide current range of 10 μA to 20 mA, these devices feature exceptionally low dynamic impedance, low noise and stable operation over time and temperature. Tight voltage tolerances are achieved by on−chip trimming. The large dynamic operating range enables these devices to be used in applications with widely varying supplies with excellent regulation. Extremely low operating current make these devices ideal for micropower circuitry like portable instrumentation, regulators and other analog circuitry where extended battery life is required.

The LM285/LM385 series are packaged in a low cost TO−226 plastic case and are available in two voltage versions of 1.235 V and 2.500 V as denoted by the device suffix (see Ordering Information table). The LM285 is specified over a −40°C to +85°C temperature range while the LM385 is rated from 0°C to +70°C.

The LM385 is also available in a surface mount plastic package in voltages of 1.235 V and 2.500 V.

Features

- Operating Current from 10 μA to 20 mA
- 1.0%, 1.5%, 2.0% and 3.0% Initial Tolerance Grades
- Low Temperature Coefficient
- 1.0 Ω Dynamic Impedance
- Surface Mount Package Available
- These Devices are Pb−Free and are RoHS Compliant

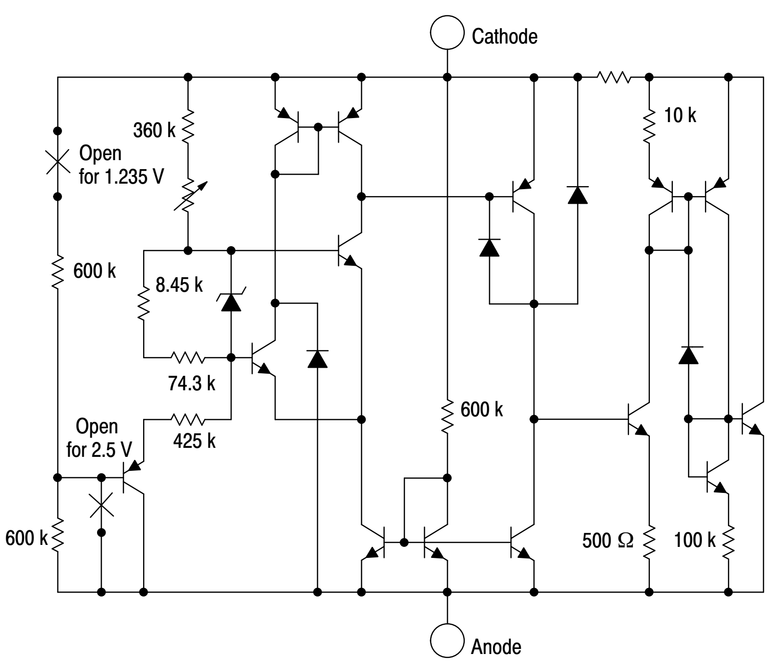
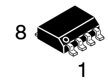
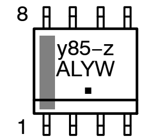


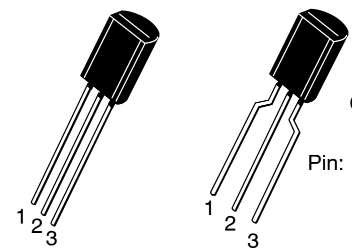
Figure 1. Representative Schematic Diagram

MARKING DIAGRAMS



SOIC−8
D SUFFIX
CASE 751





STRAIGHT LEAD　　BENT LEAD

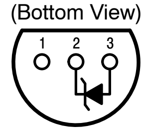
TO−92
CASE 29−10

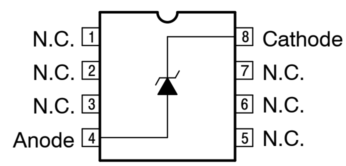
Pin: 1. N.C.
2. Cathode
3. Anode

xxx	= 1.2 or 2.5
y	= 2 or 3
z	= 1 or 2
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

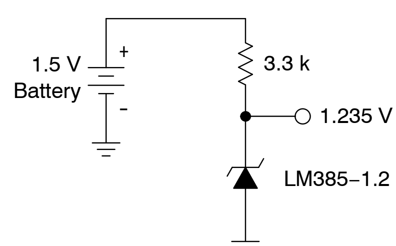
(Note: Microdot may be in either location)

(Bottom View)





Standard Application



ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

April, 2022 − Rev. 11

Publication Order Number:
LM285/D

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted)

Rating	Symbol	Value	Unit
Reverse Current	I_R	30	mA
Forward Current	I_F	10	mA
Operating Ambient Temperature Range LM285 LM385	T_A	 −40 to +85 0 to +70	°C
Operating Junction Temperature	T_J	+150	°C
Storage Temperature Range	T_{stg}	−65 to + 150	°C
Electrostatic Discharge Sensitivity (ESD) Human Body Model (HBM) Machine Model (MM) Charged Device Model (CDM)	ESD	 4000 400 2000	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, unless otherwise noted)

Characteristic	Symbol	LM285−1.2			LM385−1.2/LM385B−1.2			Unit
		Min	Typ	Max	Min	Typ	Max	
Reverse Breakdown Voltage ($I_{Rmin} \le I_R \le$ 20 mA) LM285−1.2/LM385B−1.2 $T_A = T_{low}$ to T_{high} (Note 1) LM385−1.2 $T_A = T_{low}$ to T_{high} (Note 1)	$V_{(BR)R}$	 1.223 1.200 – –	 1.235 – – –	 1.247 1.270 – –	 1.223 1.210 1.205 1.192	 1.235 – 1.235 –	 1.247 1.260 1.260 1.273	V
Minimum Operating Current T_A = 25°C $T_A = T_{low}$ to T_{high} (Note 1)	I_{Rmin}	 – –	 8.0 –	 10 20	 –	 8.0 –	 15 20	µA
Reverse Breakdown Voltage Change with Current $I_{Rmin} \le I_R \le$ 1.0 mA, T_A = +25°C $T_A = T_{low}$ to T_{high} (Note 1) 1.0 mA $\le I_R \le$ 20 mA, T_A = +25°C $T_A = T_{low}$ to T_{high} (Note 1)	$\Delta V_{(BR)R}$	 – – – –	 – – – –	 1.0 1.5 10 20	 – – – –	 – – – –	 1.0 1.5 20 25	mV
Reverse Dynamic Impedance I_R = 100 µA, T_A = +25°C	Z	–	0.6	–	–	0.6	–	Ω
Average Temperature Coefficient 10 µA $\le I_R \le$ 20 mA, $T_A = T_{low}$ to T_{high} (Note 1)	$\Delta V_{(BR)}/\Delta T$	–	80	–	–	80	–	ppm/°C
Wideband Noise (RMS) I_R = 100 µA, 10 Hz $\le$ f $\le$ 10 kHz	n	–	60	–	–	60	–	µV
Long Term Stability I_R = 100 µA, T_A = +25°C ± 0.1°C	S	–	20	–	–	20	–	ppm/kHR
Reverse Breakdown Voltage ($I_{Rmin} \le I_R \le$ 20 mA) LM285−2.5/LM385B−2.5 $T_A = T_{low}$ to T_{high} (Note 1) LM385−2.5 $T_A = T_{low}$ to T_{high} (Note 1)	$V_{(BR)R}$	 2.462 2.415 – –	 2.5 – – –	 2.538 2.585 – –	 2.462 2.436 2.425 2.400	 2.5 – 2.5 –	 2.538 2.564 2.575 2.600	V
Minimum Operating Current T_A = 25°C $T_A = T_{low}$ to T_{high} (Note 1)	I_{Rmin}	 – –	 13 –	 20 30	 – –	 13 –	 20 30	µA

1. T_{low} = −40°C for LM285−1.2, LM285−2.5
   T_{high} = +85°C for LM285−1.2, LM285−2.5
   T_{low} = 0°C for LM385−1.2, LM385B−1.2, LM385−2.5, LM385B−2.5
   T_{high} = +70°C for LM385−1.2, LM385B−1.2, LM385−2.5, LM385B−2.5

ELECTRICAL CHARACTERISTICS (T_A = 25°C, unless otherwise noted)

Characteristic	Symbol	LM285−1.2			LM385−1.2/LM385B−1.2			Unit
		Min	Typ	Max	Min	Typ	Max	
Reverse Breakdown Voltage Change with Current	$\Delta V_{(BR)R}$							mV
$I_{Rmin} \le I_R \le$ 1.0 mA, T_A = +25°C		–	–	1.0	–	–	2.0	
$T_A = T_{low}$ to T_{high} (Note 2)		–	–	1.5	–	–	2.5	
1.0 mA $\le I_R \le$ 20 mA, T_A = +25°C		–	–	10	–	–	20	
$T_A = T_{low}$ to T_{high} (Note 2)		–	–	20	–	–	25	
Reverse Dynamic Impedance I_R = 100 μA, T_A = +25°C	Z	–	0.6	–	–	0.6	–	Ω
Average Temperature Coefficient 20 μA $\le I_R \le$ 20 mA, $T_A = T_{low}$ to T_{high} (Note 2)	$\Delta V_{(BR)}/\Delta T$	–	80	–	–	80	–	ppm/°C
Wideband Noise (RMS) I_R = 100 μA, 10 Hz $\le f \le$ 10 kHz	n	–	120	–	–	120	–	μV
Long Term Stability I_R = 100 μA, T_A = +25°C ± 0.1°C	S	–	20	–	–	20	–	ppm/kHR

2. T_{low} = −40°C for LM285−1.2, LM285−2.5
T_{high} = +85°C for LM285−1.2, LM285−2.5
T_{low} = 0°C for LM385−1.2, LM385B−1.2, LM385−2.5, LM385B−2.5
T_{high} = +70°C for LM385−1.2, LM385B−1.2, LM385−2.5, LM385B−2.5

TYPICAL PERFORMANCE CURVES FOR LM285−1.2/385−1.2/385B−1.2

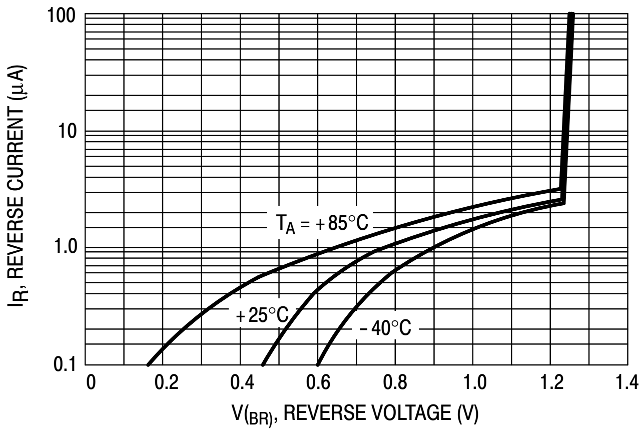


Figure 2. Reverse Characteristics

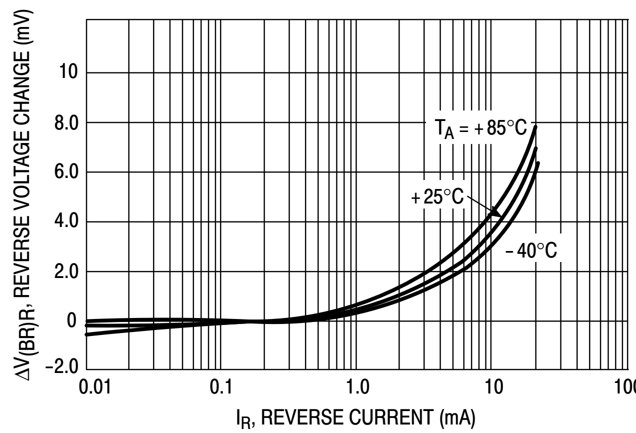


Figure 3. Reverse Characteristics

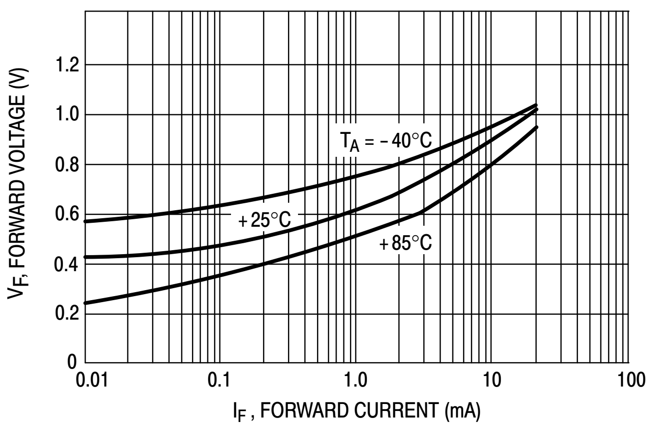


Figure 4. Forward Characteristics

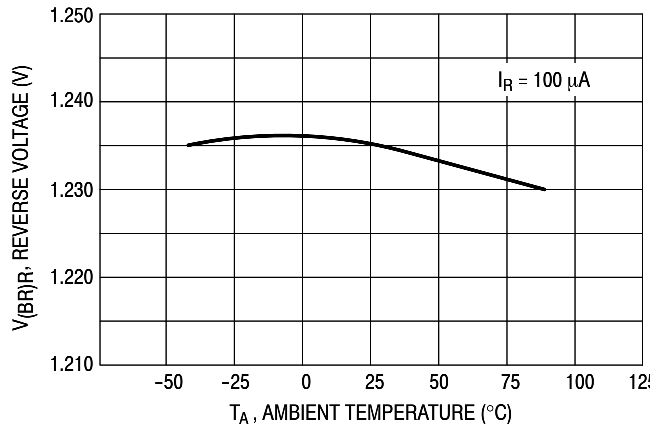


Figure 5. Temperature Drift

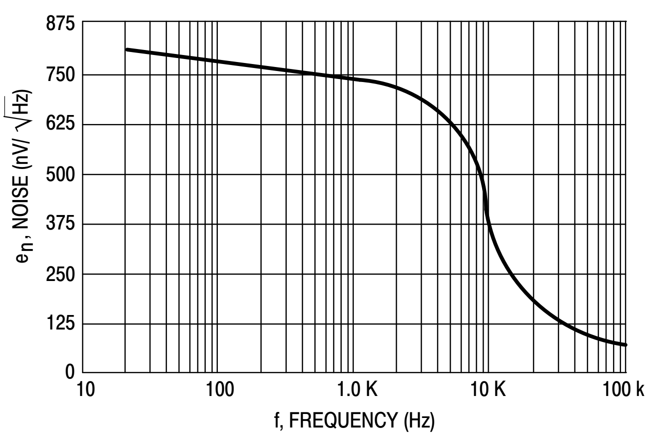


Figure 6. Noise Voltage

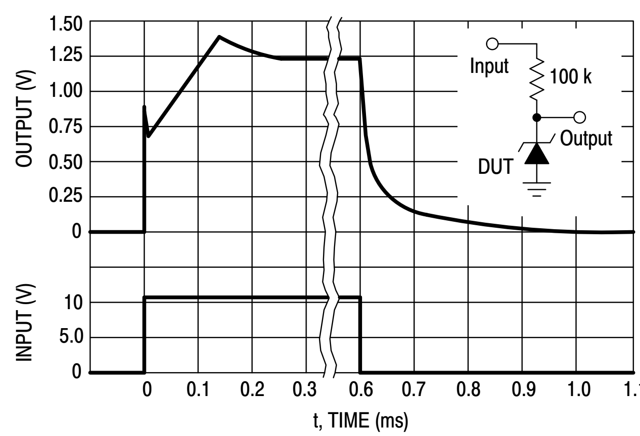


Figure 7. Response Time

TYPICAL PERFORMANCE CURVES FOR LM285−2.5/385−2.5/385B−2.5

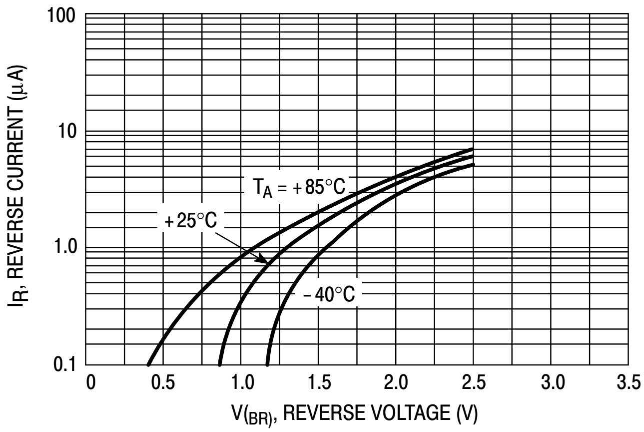


Figure 8. Reverse Characteristics

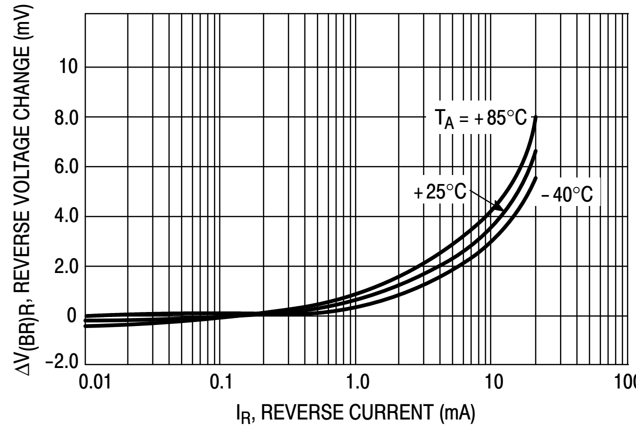


Figure 9. Reverse Characteristics

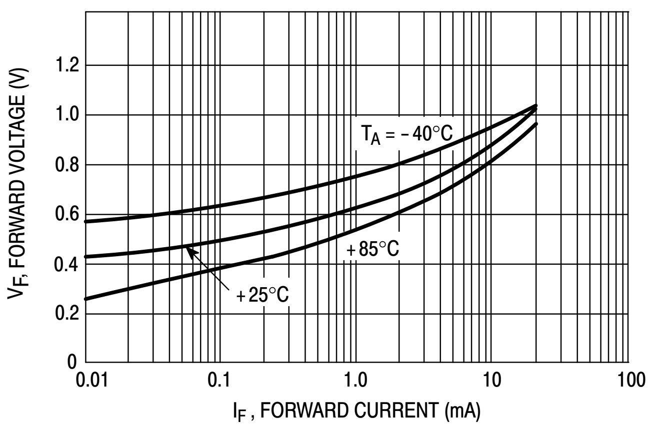


Figure 10. Forward Characteristics

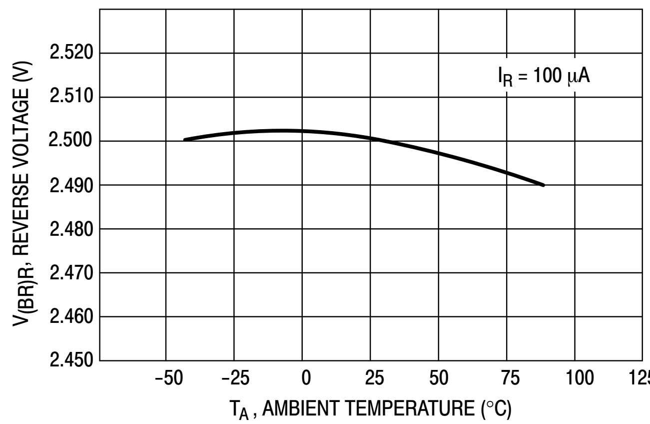


Figure 11. Temperature Drift

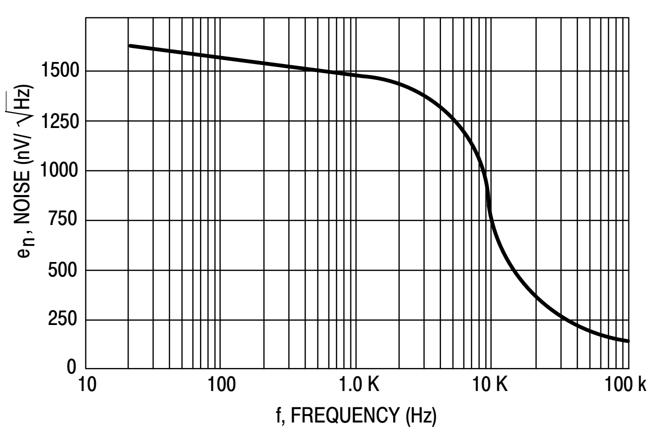


Figure 12. Noise Voltage

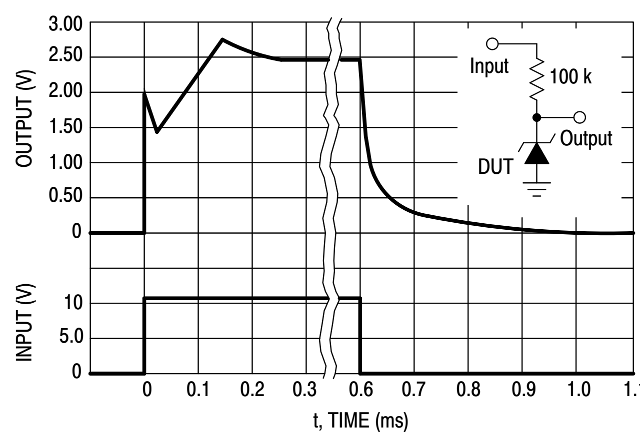


Figure 13. Response Time

ORDERING INFORMATION

Device	Operating Temperature Range	Reverse Break−Down Voltage	Package	Shipping†
LM285D−1.2	T_A = −40°C to +85°C	1.235 V	SOIC−8	98 Units / Rail
LM285D−1.2G			SOIC−8 (Pb−Free)	98 Units / Rail
LM285D−1.2R2			SOIC−8	2500 / Tape & Reel
LM285D−1.2R2G			SOIC−8 (Pb−Free)	2500 / Tape & Reel
LM285D−2.5		2.500 V	SOIC−8	98 Units / Rail
LM285D−2.5G			SOIC−8 (Pb−Free)	98 Units / Rail
LM285D−2.5R2			SOIC−8	2500 / Tape & Reel
LM285D−2.5R2G			SOIC−8 (Pb−Free)	2500 / Tape & Reel
LM285Z−1.2		1.235 V	TO−92	2000 Units / Bag
LM285Z−1.2G			TO−92 (Pb−Free)	2000 Units / Bag
LM285Z−2.5		2.500 V	TO−92	2000 Units / Bag
LM285Z−2.5G			TO−92 (Pb−Free)	2000 Units / Bag
LM285Z−1.2RA		1.235 V	TO−92	2000 / Tape & Reel
LM285Z−1.2RAG			TO−92 (Pb−Free)	2000 / Tape & Reel
LM285Z−2.5RA		2.500 V	TO−92	2000 / Tape & Reel
LM285Z−2.5RAG			TO−92 (Pb−Free)	2000 / Tape & Reel
LM285Z−2.5RP			TO−92	2000 Units / Fan−Fold
LM285Z−2.5RPG			TO−92 (Pb−Free)	2000 Units / Fan−Fold
LM385BD−1.2	T_A = 0°C to +70°C	1.235 V	SOIC−8	98 Units / Rail
LM385BD−1.2G			SOIC−8 (Pb−Free)	98 Units / Rail
LM385BD−1.2R2			SOIC−8	2500 / Tape & Reel
LM385BD−1.2R2G			SOIC−8 (Pb−Free)	2500 / Tape & Reel
LM385BD−2.5		2.500 V	SOIC−8	98 Units / Rail
LM385BD−2.5G			SOIC−8 (Pb−Free)	98 Units / Rail
LM385BD−2.5R2			SOIC−8	2500 / Tape & Reel
LM385BD−2.5R2G			SOIC−8 (Pb−Free)	2500 / Tape & Reel
LM385BZ−1.2		1.235 V	TO−92	2000 Units / Bag
LM385BZ−1.2G			TO−92 (Pb−Free)	2000 Units / Bag
LM385BZ−1.2RA			TO−92	2000 / Tape & Reel
LM385BZ−1.2RAG			TO−92 (Pb−Free)	2000 / Tape & Reel

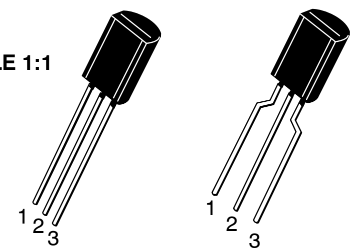
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ORDERING INFORMATION

Device	Operating Temperature Range	Reverse Break−Down Voltage	Package	Shipping†
LM385BZ−2.5	T_A = 0°C to +70°C	2.500 V	TO−92	2000 Units / Bag
LM385BZ−2.5G			TO−92 (Pb−Free)	2000 Units / Bag
LM385BZ−2.5RA			TO−92	2000 / Tape & Reel
LM385BZ−2.5RAG			TO−92 (Pb−Free)	2000 / Tape & Reel
LM385D−1.2		1.235 V	SOIC−8	98 Units / Rail
LM385D−1.2G			SOIC−8 (Pb−Free)	98 Units / Rail
LM385D−1.2R2			SOIC−8	2500 / Tape & Reel
LM385D−1.2R2G			SOIC−8 (Pb−Free)	2500 / Tape & Reel
LM385D−2.5		2.500 V	SOIC−8	98 Units / Rail
LM385D−2.5G			SOIC−8 (Pb−Free)	98 Units / Rail
LM385D−2.5R2			SOIC−8	2500 / Tape & Reel
LM385D−2.5R2G			SOIC−8 (Pb−Free)	2500 / Tape & Reel
LM385Z−1.2		1.235 V	TO−92	2000 Units / Bag
LM385Z−1.2G			TO−92 (Pb−Free)	2000 Units / Bag
LM385Z−1.2RA			TO−92	2000 / Tape & Reel
LM385Z−1.2RAG			TO−92 (Pb−Free)	2000 / Tape & Reel
LM385Z−1.2RP			TO−92	2000 / Ammo Box
LM385Z−1.2RPG			TO−92 (Pb−Free)	2000 / Ammo Box
LM385Z−2.5		2.500 V	TO−92	2000 Units / Bag
LM385Z−2.5G			TO−92 (Pb−Free)	2000 Units / Bag
LM385Z−2.5RP			TO−92	2000 / Ammo Box
LM385Z−2.5RPG			TO−92 (Pb−Free)	2000 / Ammo Box

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

SCALE 1:1

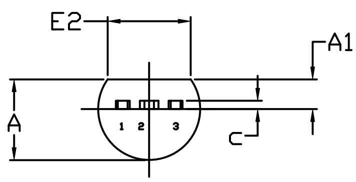


STRAIGHT LEAD BENT LEAD

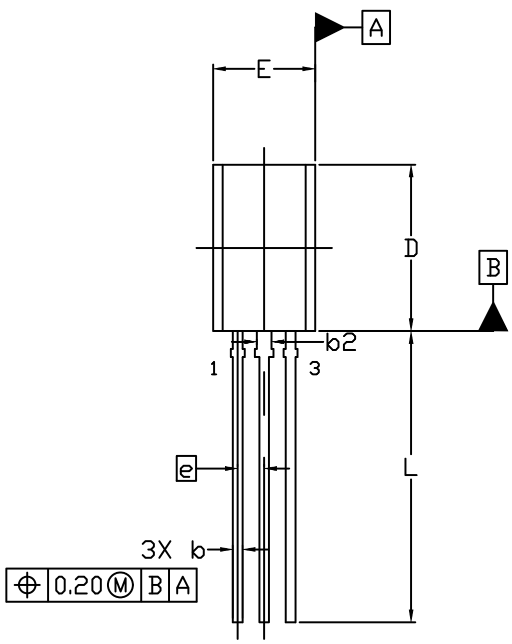
TO−92 (TO−226) 1 WATT
CASE 29−10
ISSUE D

DATE 05 MAR 2021

STRAIGHT LEAD



END VIEW



TOP VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS.
4. DIMENSION b AND b2 DOES NOT INCLUDE DAMBAR PROTRUSION. LEAD WIDTH INCLUDING PROTRUSION SHALL NOT EXCEED 0.20. DIMENSION b2 LOCATED ABOVE THE DAMBAR PORTION OF MIDDLE LEAD.

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	3.75	3.90	4.05
A1	1.28	1.43	1.58
b	0.38	0.465	0.55
b2	0.62	0.70	0.78
c	0.35	0.40	0.45
D	7.85	8.00	8.15
E	4.75	4.90	5.05
E2	3.90	---	---
e	1.27 BSC		
L	13.80	14.00	14.20

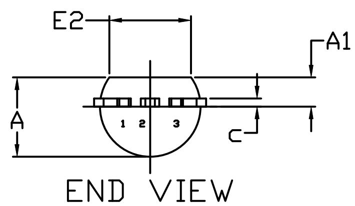
STYLES AND MARKING ON PAGE 3

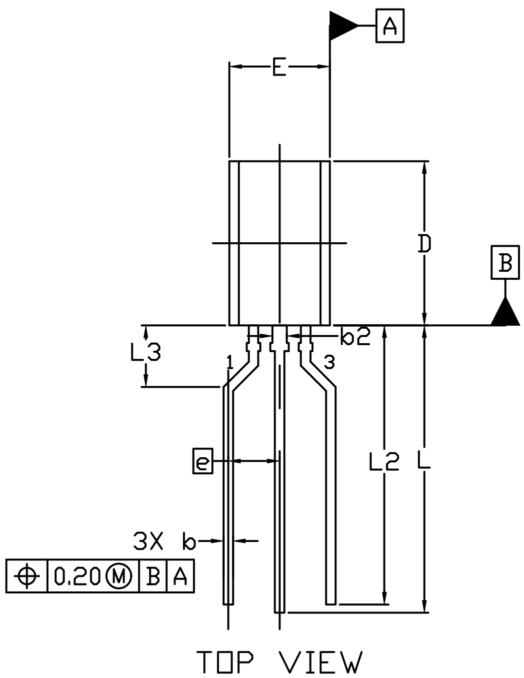
DOCUMENT NUMBER:	**98AON52857E**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**TO−92 (TO−226) 1 WATT**	**PAGE 1 OF 3**

TO−92 (TO−226) 1 WATT
CASE 29−10
ISSUE D

DATE 05 MAR 2021

FORMED LEAD





NOTES:
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2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS.
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	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	3.75	3.90	4.05
A1	1.28	1.43	1.58
b	0.38	0.465	0.55
b2	0.62	0.70	0.78
c	0.35	0.40	0.45
D	7.85	8.00	8.15
E	4.75	4.90	5.05
E2	3.90	---	---
e	2.50 BSC		
L	13.80	14.00	14.20
L2	13.20	13.60	14.00
L3	3.00 REF		

STYLES AND MARKING ON PAGE 3

DOCUMENT NUMBER:	**98AON52857E**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**TO−92 (TO−226) 1 WATT**	**PAGE 2 OF 3**

TO−92 (TO−226) 1 WATT
CASE 29−10
ISSUE D

DATE 05 MAR 2021

STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 3:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 5:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 6:
PIN 1. GATE
2. SOURCE & SUBSTRATE
3. DRAIN

STYLE 7:
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 8:
PIN 1. DRAIN
2. GATE
3. SOURCE & SUBSTRATE

STYLE 9:
PIN 1. BASE 1
2. EMITTER
3. BASE 2

STYLE 10:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 11:
PIN 1. ANODE
2. CATHODE & ANODE
3. CATHODE

STYLE 12:
PIN 1. MAIN TERMINAL 1
2. GATE
3. MAIN TERMINAL 2

STYLE 13:
PIN 1. ANODE 1
2. GATE
3. CATHODE 2

STYLE 14:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

STYLE 15:
PIN 1. ANODE 1
2. CATHODE
3. ANODE 2

STYLE 16:
PIN 1. ANODE
2. GATE
3. CATHODE

STYLE 17:
PIN 1. COLLECTOR
2. BASE
3. EMITTER

STYLE 18:
PIN 1. ANODE
2. CATHODE
3. NOT CONNECTED

STYLE 19:
PIN 1. GATE
2. ANODE
3. CATHODE

STYLE 20:
PIN 1. NOT CONNECTED
2. CATHODE
3. ANODE

STYLE 21:
PIN 1. COLLECTOR
2. EMITTER
3. BASE

STYLE 22:
PIN 1. SOURCE
2. GATE
3. DRAIN

STYLE 23:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 24:
PIN 1. EMITTER
2. COLLECTOR/ANODE
3. CATHODE

STYLE 25:
PIN 1. MT 1
2. GATE
3. MT 2

STYLE 26:
PIN 1. V_{CC}
2. GROUND 2
3. OUTPUT

STYLE 27:
PIN 1. MT
2. SUBSTRATE
3. MT

STYLE 28:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 29:
PIN 1. NOT CONNECTED
2. ANODE
3. CATHODE

STYLE 30:
PIN 1. DRAIN
2. GATE
3. SOURCE

STYLE 31:
PIN 1. GATE
2. DRAIN
3. SOURCE

STYLE 32:
PIN 1. BASE
2. COLLECTOR
3. EMITTER

STYLE 33:
PIN 1. RETURN
2. INPUT
3. OUTPUT

STYLE 34:
PIN 1. INPUT
2. GROUND
3. LOGIC

STYLE 35:
PIN 1. GATE
2. COLLECTOR
3. EMITTER

GENERIC MARKING DIAGRAM*

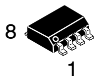
XXXXX
XXXXX
ALYW▪
▪

XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

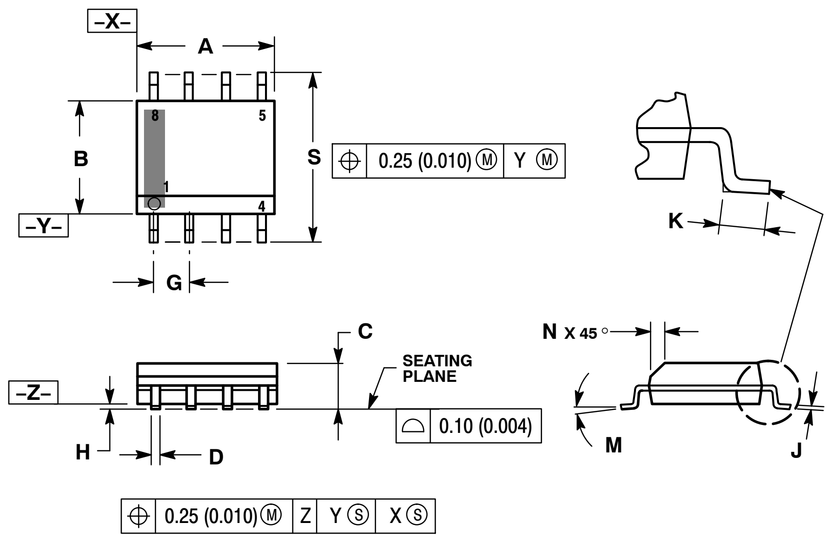
DOCUMENT NUMBER:	98AON52857E	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	TO−92 (TO−226) 1 WATT	PAGE 3 OF 3



SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

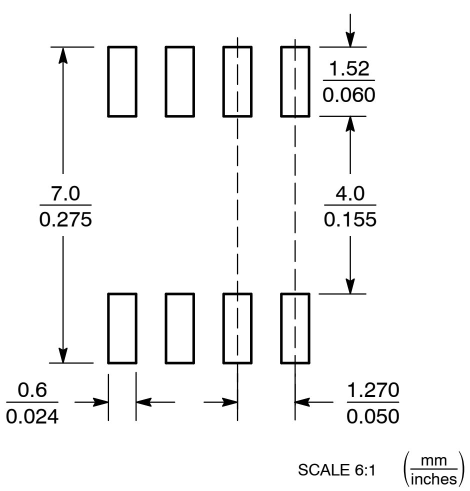
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

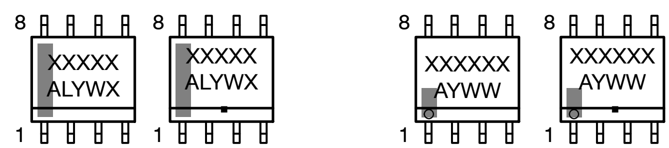
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



IC **IC (Pb−Free)** **Discrete** **Discrete (Pb−Free)**

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42564B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	SOIC−8 NB	PAGE 1 OF 2

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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