FAN23SV65AMPX

Buck Regulator, Synchronous, 15 A

Description

The FAN23SV65A is a highly efficient synchronous buck regulator. The regulator is capable of operating with an input range from 7 V to 24 V and supporting up to 15 A continuous load currents. The device can operate from a 5 V rail (±10%) if V_{IN}, P_{VIN}, and P_{VCC} are connected together to bypass the internal linear regulator.

The FAN23SV65A utilizes ON Semiconductor's constant on−time control architecture to provide excellent transient response and to maintain a relatively constant switching frequency. This device utilizes Pulse Frequency Modulation (PFM) mode to maximize light−load efficiency by reducing switching frequency when the inductor is operating in discontinuous conduction mode at light loads, while clamping the minimum frequency above the audible range with ultrasonic mode.

Switching frequency and over−current protection can be programmed to provide a flexible solution for various applications. Output over−voltage, under−voltage, over−current, and thermal shutdown protections help prevent damage to the device during fault conditions. After thermal shutdown is activated, a hysteresis feature restarts the device when normal operating temperature is reached.

Features

- V_{IN} Range: 7 V to 24 V Using Internal Linear Regulator for Bias
- V_{IN} Range: 4.5 V to 5.5 V with $V_{IN}/P_{VIN}/P_{VCC}$ Connected to Bypass Internal Regulator
- High Efficiency: Over to 96% Peak
- Continuous Output Current: 15 A
- Internal Linear Bias Regulator
- Accurate Enable Facilitates V_{IN} UVLO Functionality
- PFM Mode for Light−Load Efficiency
- Excellent Line and Load Transient Response
- Precision Reference: ±1% Over Temperature
- Output Voltage Range: 0.6 to 5.5 V
- Programmable Frequency: 200 kHz to 1 MHz
- Programmable Soft−Start
- Low Shutdown Current
- Adjustable Sourcing Current Limit
- Internal Boot Diode
- Thermal Shutdown
- Halogen and Lead Free, RoHS Compliant

Applications

- Mainstream Notebooks
- Servers and Desktop Computers
- Game Consoles
- Telecommunications
- Storage
- Base Stations

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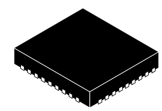
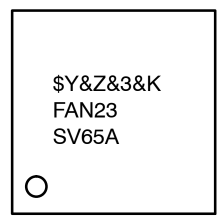


PQFN34
CASE 483AM

MARKING DIAGRAM



$Y	= Logo
&Z	= Assembly Plant Code
&3	= Numeric Date Code
&K	= Lot Code
FAN23SV65A	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

June, 2018 − Rev. 2

Publication Order Number:
FAN23SV65AMPX/D

ORDERING INFORMATION

Part Number	Configuration	Operating Temperature Range	Output Current (A)	Package
FAN23SV65AMPX	PFM with Ultrasonic Mode	−40 to 125°C	15	34−Lead, PQFN, 5.5 mm x 5.0 mm

TYPICAL APPLICATION DIAGRAMS

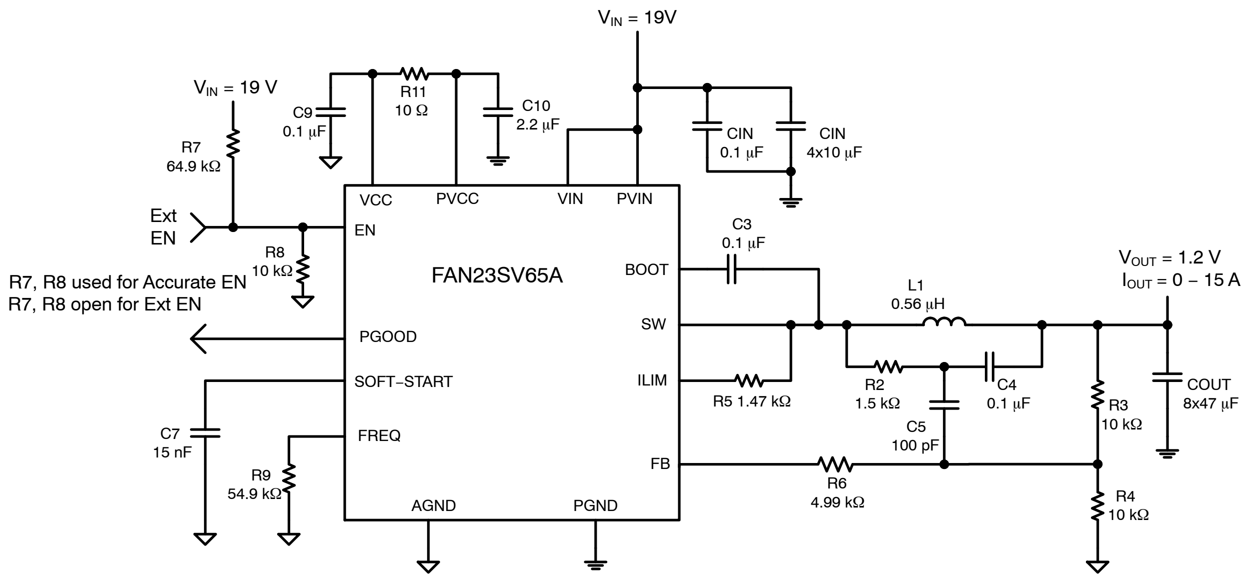


Figure 1. Typical Application with V_{IN} = 19 V

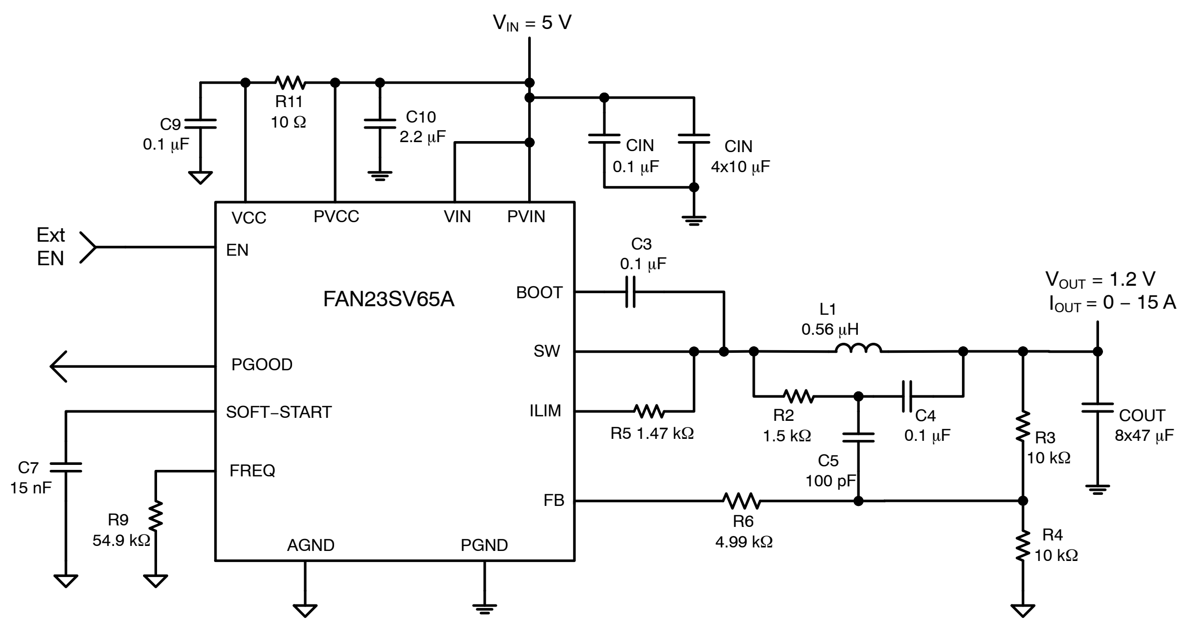


Figure 2. Typical Application with V_{IN} = 5 V

FUNCTIONAL BLOCK DIAGRAM

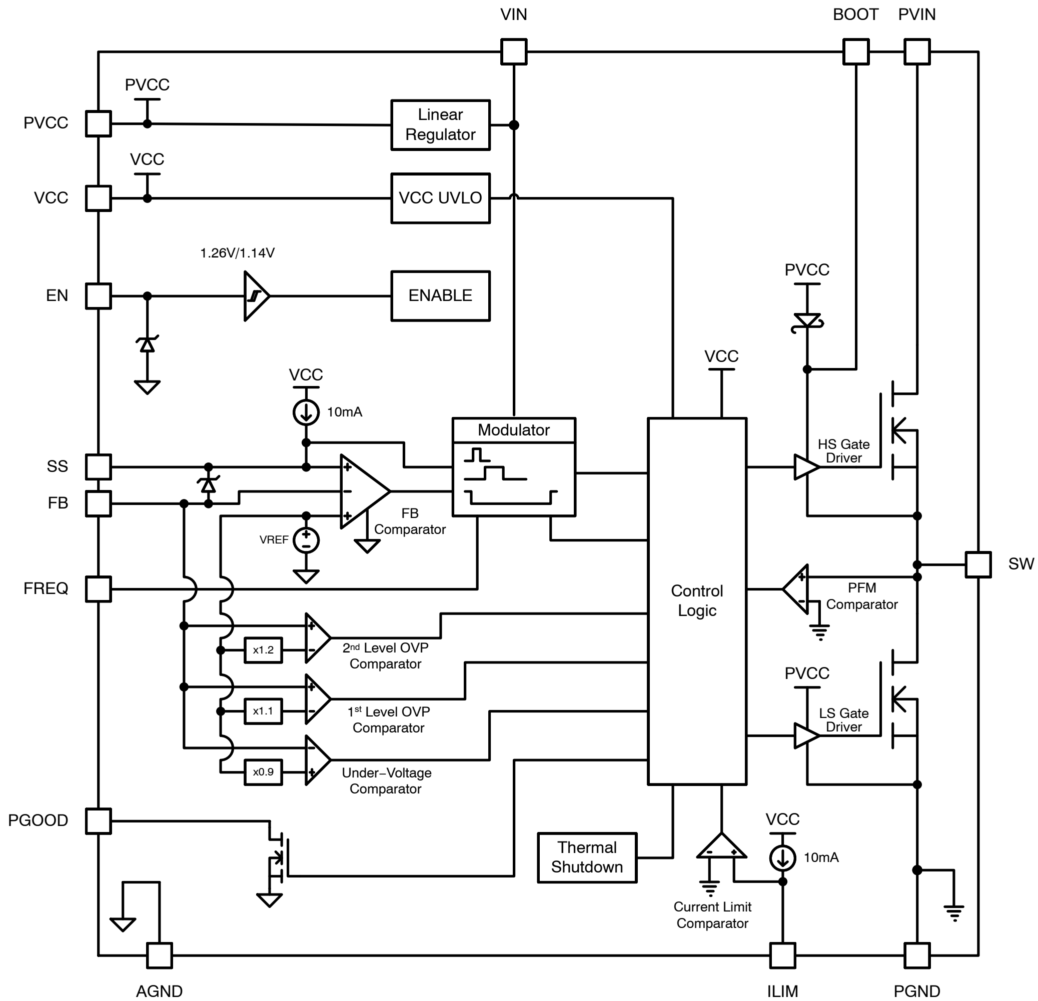


Figure 3. Block Diagram

PIN CONFIGURATION

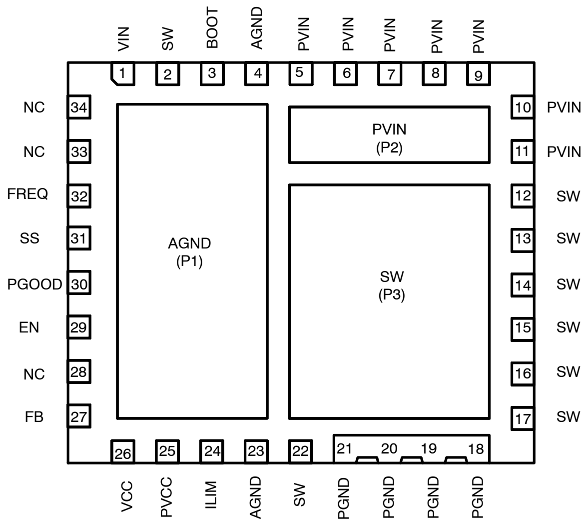


Figure 4. Pin Assignment (Bottom View)

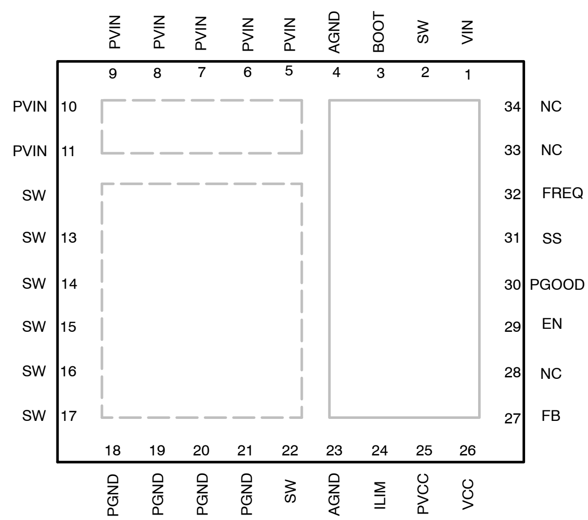


Figure 5. Pin Assignment (Top View)

PIN DEFINITIONS

Name	Pad / Pin	Description
PVIN	P2, 5–11	Power input for the power stage
VIN	1	Power input to the linear regulator; used in the modulator for input voltage feed–forward
PVCC	25	Power output of the linear regulator; directly supplies power for the low–side gate driver and boot diode. Can be connected to VIN and PVIN for operation from 5 V rail
VCC	26	Power supply input for the controller
PGND	18–21	Power ground for the low–side power MOSFET and for the low–side gate driver
AGND	P1, 4, 23	Analog ground for the analog portions of the IC and for substrate
SW	P3, 2, 12–17, 22	Switching node; junction between high–and low–side MOSFETs
BOOT	3	Supply for high–side MOSFET gate driver. A capacitor from BOOT to SW supplies the charge to turn on the N–channel high–side MOSFET. During the freewheeling interval (low–side MOSFET on), the high–side capacitor is recharged by an internal diode connected to PVCC
ILIM	24	Current limit. A resistor between ILIM and SW sets the current limit threshold
FB	27	Output voltage feedback to the modulator
EN	29	Enable input to the IC. Pin must be driven logic high to enable, or logic low to disable
SS	31	Soft–start input to the modulator
FREQ	32	On–time and frequency programming pin. Connect a resistor between FREQ and AGND to program on–time and switching frequency
PGOOD	30	Power good; open–drain output indicating V_{OUT} is within set limits
NC	28, 33–34	Leave pin open or connect to AGND

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, Unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{PVIN}	Power Input	Referenced to PGND	–0.3	30.0	V
V_{IN}	Modulator Input	Referenced to AGND	–0.3	30.0	V
V_{BOOT}	Boot Voltage	Referenced to PVCC	–0.3	30.0	V
		Referenced to PVCC, < 20 ns	–0.3	33.0	V
V_{SW}	SW Voltage to GND	Referenced to PGND, AGND	–1	30.0	V
		Referenced to PGND, AGND < 20 ns	–5	30.0	V
V_{BOOT}	Boot to SW Voltage	Referenced to SW	–0.3	6.0	V
	Boot to PGND	Referenced to PGND	–0.3	30	V
V_{PVCC}	Gate Drive Supply Input	Referenced to PGND, AGND	–0.3	6.0	V
V_{VCC}	Controller Supply Input	Referenced to PGND, AGND	–0.3	6.0	V
V_{ILIM}	Current Limit Input	Referenced to AGND	–0.3	6.0	V
V_{FB}	Output Voltage Feedback	Referenced to AGND	–0.3	6.0	V
V_{EN}	Enable Input	Referenced to AGND	–0.3	6.0	V
V_{SS}	Soft Start Input	Referenced to AGND	–0.3	6.0	V
V_{FREQ}	Frequency Input	Referenced to AGND	–0.3	6.0	V
V_{PGOOD}	Power Good Output	Referenced to AGND	–0.3	6.0	V
ESD	Electrostatic Discharge	Human Body Model, JESD22–A114		1000	V
		Charged Device Model, JESD22–C101		2500	V
T_J	Junction Temperature			+150	°C
T_{STG}	Storage Temperature		–55	+150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min	Max.	Unit
V_{PVIN}	Power Input	Referenced to PGND	7	24	V
V_{IN}	Modulator Input	Referenced to AGND	7	24	V
T_J	Junction Temperature		–40	+125	°C
I_{LOAD}	Load Current	T_A = 25°C, No Airflow		20	A
V_{PVIN}, V_{IN}, V_{PVCC}	PV_{IN}, V_{IN}, and Gate Drive Supply Input	V_{PVIN}, V_{IN}, V_{PVCC} Connected for 5 V Rail Operation and Referenced to PGND, AGND	4.5	5.5	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

THERMAL CHARACTERISTICS

(The thermal characteristics were evaluated on a 4−layer pcb structure (1 oz/1 oz/1 oz/1 oz) measuring 7 cm x 7 cm).

Symbol	Parameter	Typ.	Unit
θ_{JA}	Thermal Resistance, Junction−to−Ambient	35	°C/W
θ_{JC}	Thermal Characterization Parameter, Junction−to−Top of Case	2.7	°C/W
θ_{JPCB}	Thermal Characterization Parameter, Junction−to−PCB	2.3	°C/W

ELECTRICAL CHARACTERISTICS (Unless otherwise noted; V_{IN} = 12 V, V_{OUT}=1.2 V, and $T_A = T_J$ = −40 to +125°C. (Note 2)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
SUPPLY CURRENT						
$I_{VIN,SD}$	Shutdown Current	EN = 0 V			16	μA
$I_{VIN,Q}$	Quiescent Current	EN = 5 V, Not Switching			1.8	mA
$I_{VIN,GateCharge}$	Gate Charge Current	EN =5 V, f_{sw} = 500 kHz		22		mA
LINEAR REGULATOR						
V_{REG}	Regulator Output Voltage		4.75	5.05	5.25	V
I_{REG}	Regulator Current Limit		60			mA
REFERENCE, FEEDBACK COMPARATOR						
V_{FB}	FB Voltage Trip Point		590	596	602	mV
I_{FB}	FB Pin Bias Current		−100	0	100	nA
MODULATOR						
t_{ON}	On−Time Accuracy	R_{FREQ} = 56.2 kΩ, V_{IN}=10 V, t_{ON}=250 ns, No Load	−20		20	%
$t_{OFF,MIN}$	Minimum SW Off−Time			320	374	ns
$t_{ON,MIN}$	Minimum SW On−Time			45		ns
D_{MIN}	Minimum Duty Cycle	FB = 1 V		0		%
f_{MINF}	Minimum Frequency Clamp		18.2	25.4	32.7	kHz
SOFT−START						
I_{SS}	Soft−Start Current	SS = 0.5 V	7	10	13	μA
$t_{ON,SSMOD}$	SS On−Time Modulation	SS < 0.6 V	25		100	%
$V_{SSCLAMP,NOM}$	Nominal Soft−Start Voltage Clamp	V_{FB} = 0.6 V		400		mV
$V_{SSCLAMP,OVL}$	Soft−Start Voltage Clamp in Overload Condition	V_{FB}=0.3 V, OC Condition		40		mV
PFM ZERO−CROSSING DETECTION COMPARATOR						
V_{OFF}	ZCD Offset Voltage	$T_A = T_J$ = 25°C	−6		0	mV
CURRENT LIMIT						
I_{LIM}	Valley Current Limit Accuracy	$T_A = T_J$ = 25°C, I_{VALLEY}=18 A	−10		10	%
$V_{ILIM,OFFSET}$	Comparator Offset		−1		1	mV
K_{ILIM}	I_{LIM} Set−Point Scale Factor			85		
I_{LIMTC}	Temperature Coefficient			4000		ppm/°C

ELECTRICAL CHARACTERISTICS (Unless otherwise noted; V_{IN} = 12 V, V_{OUT}=1.2 V, and $T_A = T_J$ = −40 to +125°C. (Note 2)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
ENABLE						
V_{TH+}	Rising Threshold		1.11	1.26	1.43	V
V_{HYST}	Hysteresis			122		mV
V_{TH-}	Falling Threshold		1.00	1.14	1.28	V
$V_{ENCLAMP}$	Enable Voltage Clamp	IEN = 20 μA	4.3	4.5		V
$I_{ENCLAMP}$	Clamp Current				24	μA
I_{ENLK}	Enable Pin Leakage	EN = 1.2 V			100	nA
I_{ENLK}	Enable Pin Leakage	EN = 5 V			76	μA
UVLO						
V_{ON}	V_{CC} Good Threshold Rising				4.4	V
V_{HYS}	Hysteresis Voltage			160		mV
FAULT PROTECTION						
V_{UVP}	PGOOD UV Trip Point	On FB Falling	86	89	92	%
V_{VOP1}	PGOOD OV Trip Point	On FB Rising	108	111	115	%
V_{OVP2}	Second OV Trip Point	On FB Rising; LS = On	118	122	125	%
R_{PGOOD}	PGOOD Pull−Down Resistance	I_{PGOOD} = 2 mA			125	Ω
$t_{PG,SSDELAY}$	PGOOD Soft−Start Delay		0.82	1.42	2.03	ms
$I_{PG,LEAK}$	PGOOD Leakage Current				1	μA
THERMAL SHUTDOWN						
T_{OFF}	Thermal Shutdown Trip Point (Note 1)			155		°C
T_{HYS}	Hysteresis (Note 1)			15		°C
INTERNAL BOOTSTRAP DIODE						
V_{FBOOT}	Forward Voltage	I_F = 10 mA			0.6	V
I_R	Reverse Leakage	V_R = 24 V			1000	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
1. Guaranteed by design; not production tested.
2. Device is 100% production tested at T_A = 25°C. Limits over that temperature are guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

Tested using evaluation board circuit shown in Figure 1 with V_{IN} = 19 V, V_{OUT} = 1.2 V, F_{sw} = 500 kHz, T_A = 25°C, and no airflow; unless otherwise specified.

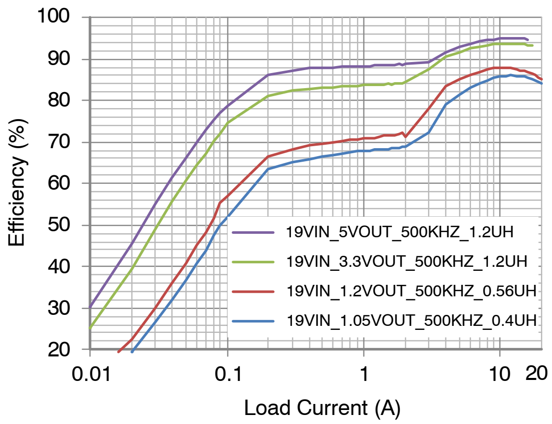


Figure 6. Efficiency vs. Load Current with V_{IN} = 19 V and f_{SW} = 500 kHz

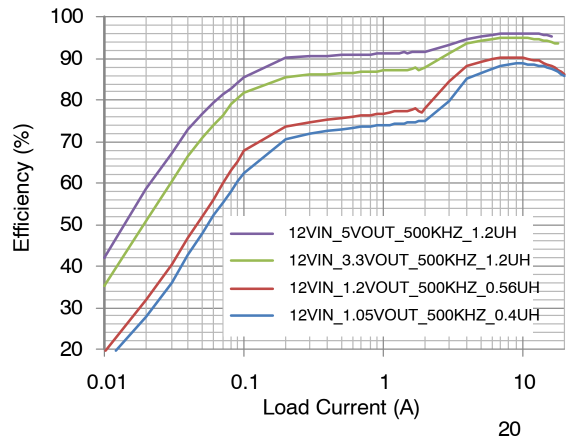


Figure 7. Efficiency vs. Load Current with V_{IN} = 12 V and f_{SW} = 500 kHz

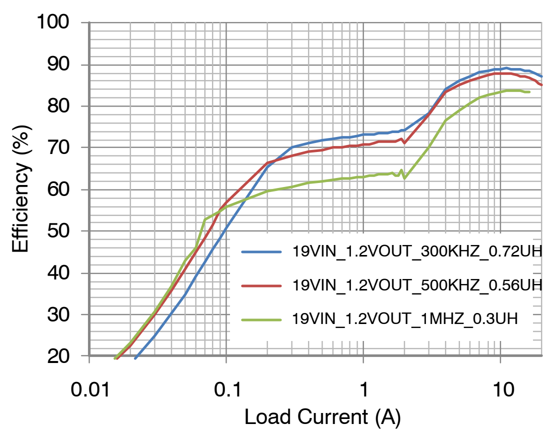


Figure 8. Efficiency vs. Load Current with V_{IN} = 19 V and V_{OUT} = 1.2 V

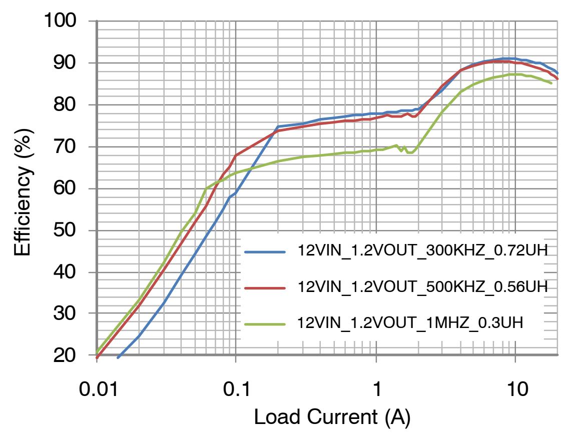


Figure 9. Efficiency vs. Load Current with V_{IN} = 12 V and V_{OUT} = 1.2 V

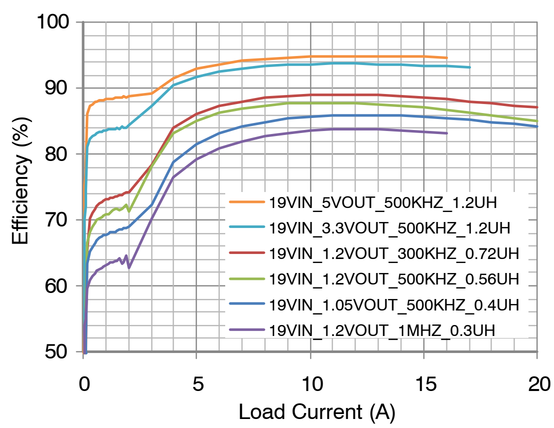


Figure 10. Efficiency vs. Load Current with V_{IN} = 19 V

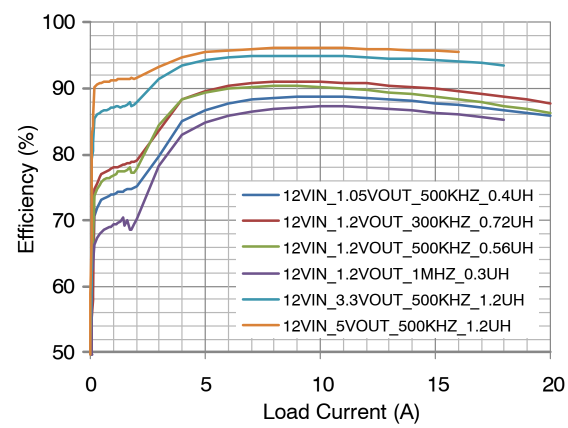


Figure 11. Efficiency vs. Load Current with V_{IN} = 12 V

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Tested using evaluation board circuit shown in Figure 1 with V_{IN} = 19 V, V_{OUT} = 1.2 V, F_{sw} = 500 kHz, T_A = 25°C, and no airflow; unless otherwise specified.

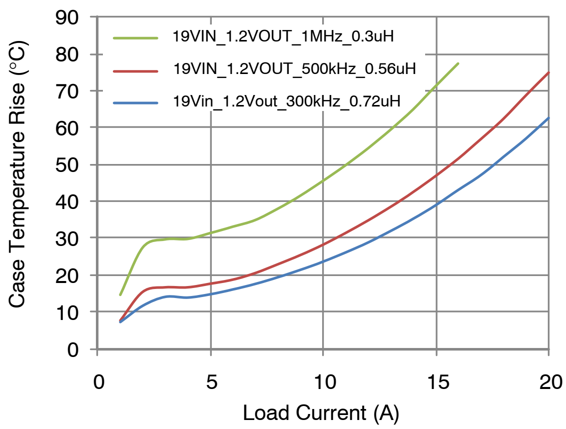


Figure 12. Case Temperature Rise vs. Load Current on 4 Layer PCB, 1 oz Copper, 7 cm x 7 cm

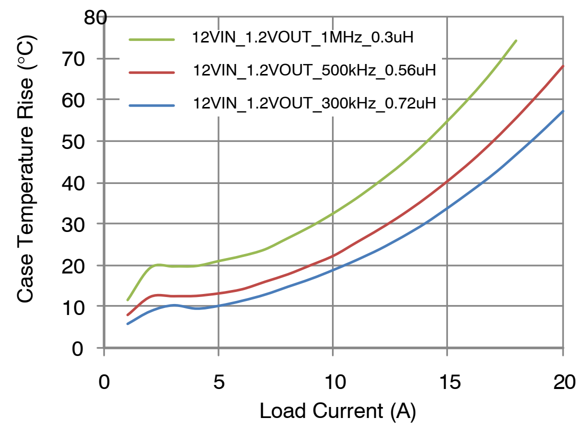


Figure 13. Case Temperature Rise vs. Load Current on 4 Layer PCB, 1 oz Copper, 7 cm x 7 cm

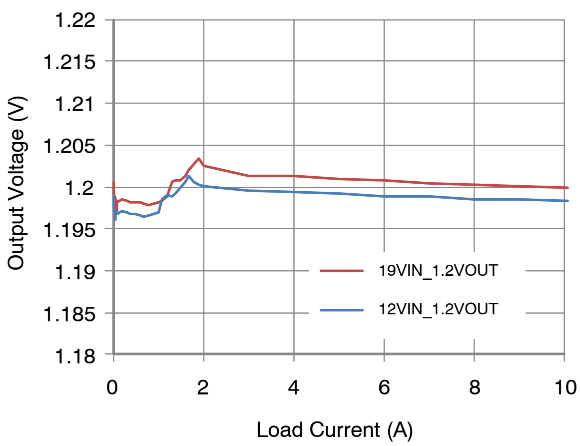


Figure 14. Load Regulation

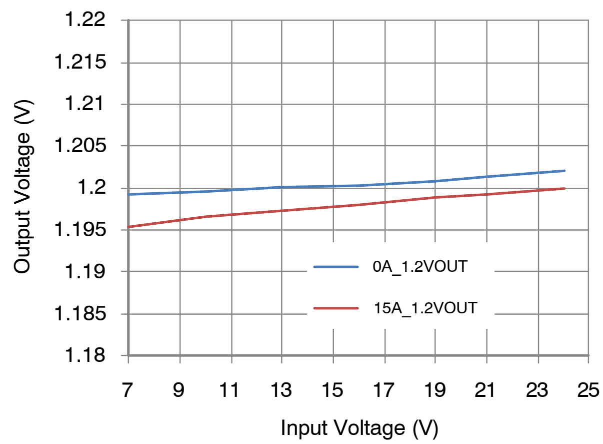


Figure 15. Line Regulation

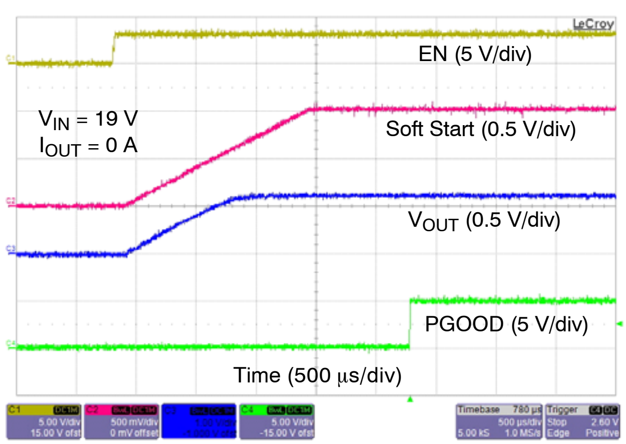


Figure 16. Startup Waveforms with 0 A Load Current

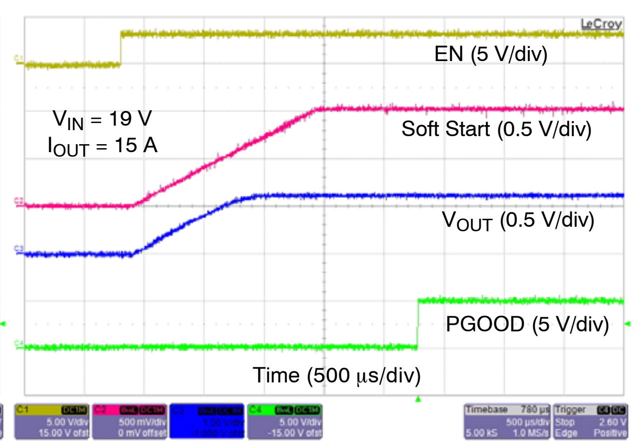


Figure 17. Startup Waveforms with 15 A Load Current

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Tested using evaluation board circuit shown in Figure 1 with V_{IN} = 19 V, V_{OUT} = 1.2 V, F_{sw} = 500 kHz, T_A = 25°C, and no airflow; unless otherwise specified.

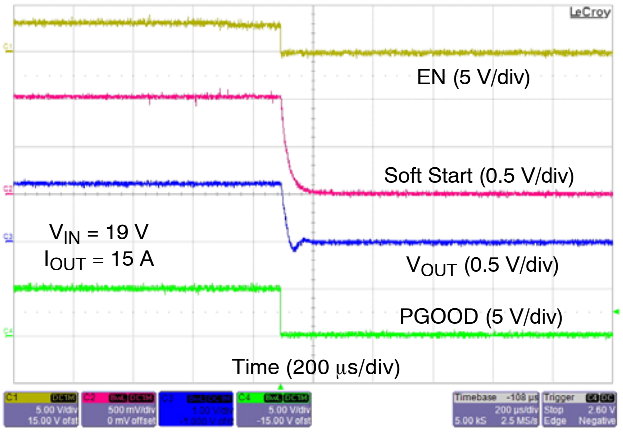


Figure 18. Shutdown Waveforms with 15 A Load Current

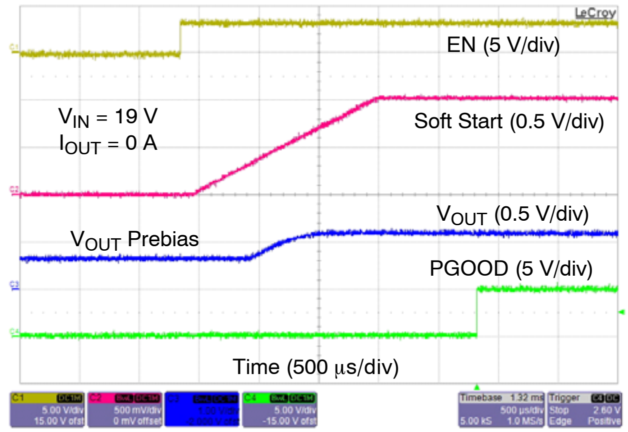


Figure 19. Startup Waveforms with Pre−Bias Voltage on Output

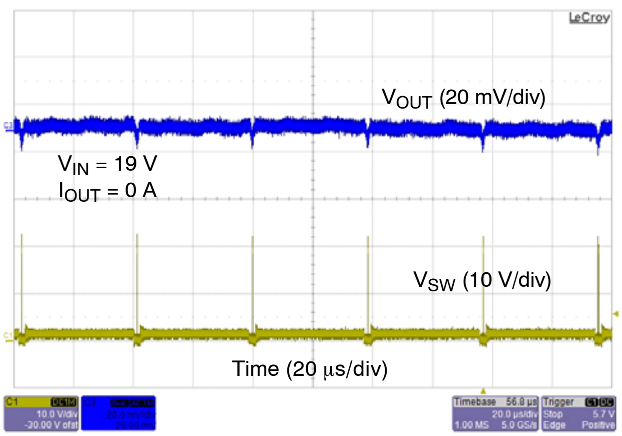


Figure 20. Static Load Ripple at No Load

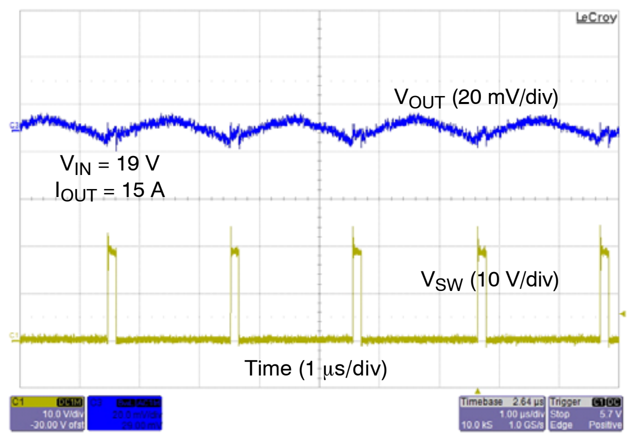


Figure 21. Static Load Ripple at Full Load

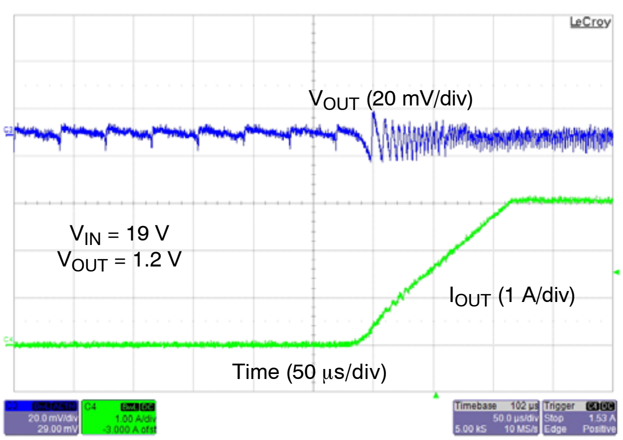


Figure 22. Operation as Load Changes from 0 A to 3 A

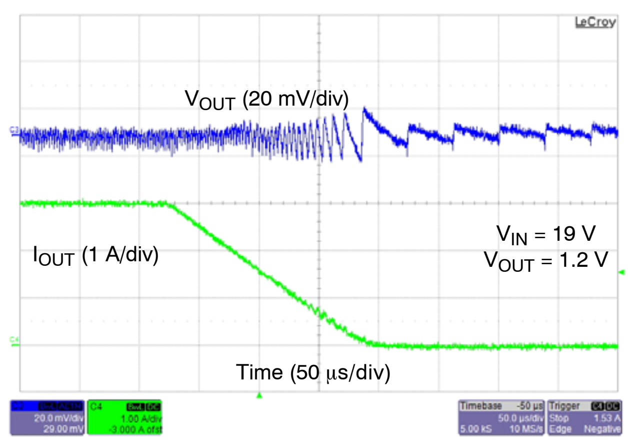


Figure 23. Operation as Load Changes from 3 A to 0 A

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Tested using evaluation board circuit shown in Figure 1 with V_{IN} = 19 V, V_{OUT} = 1.2 V, F_{sw} = 500 kHz, T_A = 25°C, and no airflow; unless otherwise specified.

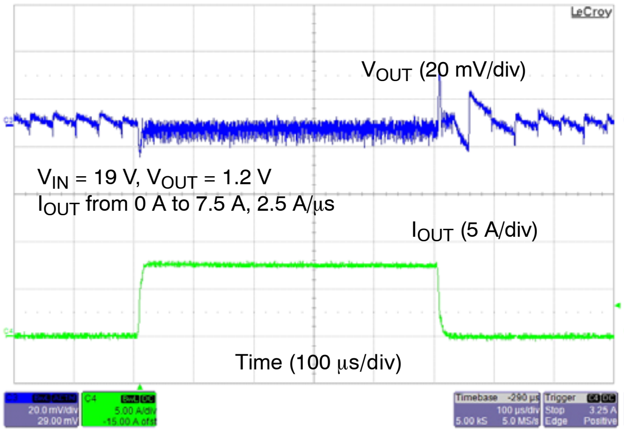


Figure 24. Load Transient from 0% to 50% Load Current

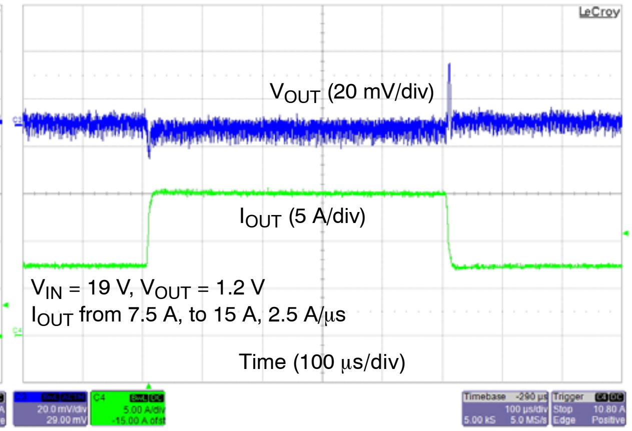


Figure 25. Load Transient from 50% to 100% Load Current

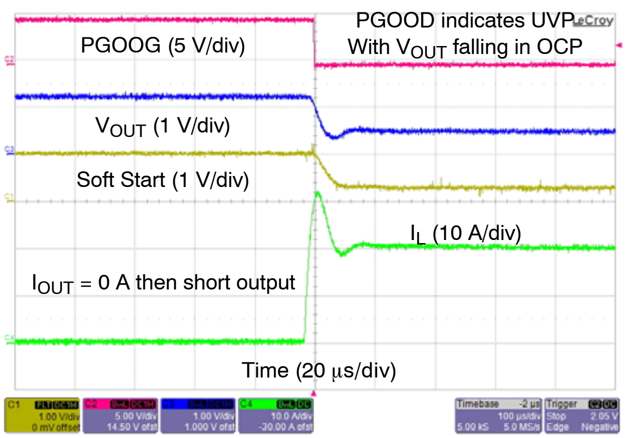


Figure 26. Over−Current Protection with Heavy Load

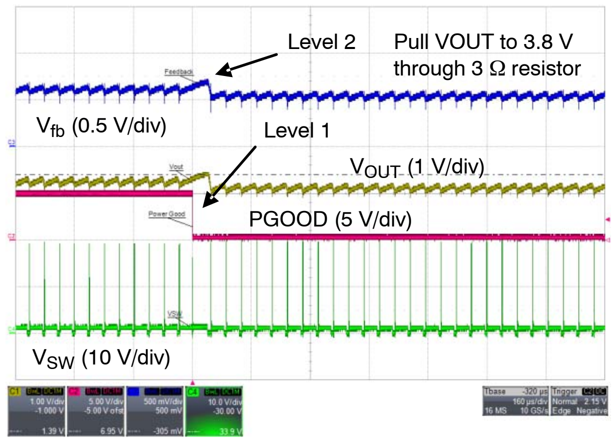


Figure 27. Over−Voltage Protection Level 1 and Level 2

CIRCUIT OPERATION

The FAN23SV65A uses a constant on−time modulation architecture with a VIN feed−forward input to accommodate a wide VIN range. This method provides fixed switching frequency (f_{SW}) operation when the inductor operates in Continuous Conduction Mode (CCM) and variable frequency when operating in Pulse Frequency Mode (PFM) at light loads. Additional benefits include excellent line and load transient response, cycle−by−cycle current limiting, and no loop compensation is required.

At the beginning of each cycle, FAN23SV65A turns on the high−side MOSFET (HS) for a fixed duration (t_{ON}). At the end of t_{ON}, HS turns off for a duration (t_{OFF}) determined by the operating conditions. Once the FB voltage (V_{FB}) falls below the reference voltage (V_{REF}), a new switching cycle begins.

The modulator provides a minimum off−time ($t_{OFF-MIN}$) of 320 ns to provide a guaranteed interval for low−side MOSFET (LS) current sensing and PFM operation. T_{offmin} is also used to provide stability against multiple pulsing and limits maximum switching frequency during transient events.

Enable

The enable pin can be driven with an external logic signal, connected to a resistive divider from PVIN/Vin to ground to create an Under−Voltage Lockout (UVLO) based on the PVIN/VIN supply, or connected to PVIN/VIN through a single resistor to auto−enable while operating within the EN pin internal clamp current sink capability.

The EN pin can be directly driven by logic voltages of 5 V, 3.3 V, 2.5 V, etc. If the EN pin is driven by 5 V logic, a small current flows into the pin when the EN pin voltage exceeds the internal clamp voltage of 4.3 V. To eliminate clamp current flowing into the EN pin use a voltage divider to limit the EN pin voltage to < 4 V.

To implement the UVLO function based on PVIN/VIN voltage level, select values for R7 and R8 in Figure 1 such that the tap point reaches 1.26 V when V_{IN} reaches the desired startup level using the following equation:

$$R7 = R8\left(\frac{V_{IN,on}}{V_{EN,on}} - 1\right) \qquad \text{(eq. 1)}$$

where $V_{IN,on}$ is the input voltage for startup and $V_{EN,on}$ is the EN pin rising threshold of 1.26 V. With R8 selected as 10 kΩ, and $V_{IN,on}$ = 9 V the value of R7 is 61.9 kΩ.

The EN pin can be pulled high with a single resistor connected from VIN to the EN pin. With VIN > 5.5 V a series resistor is required to limit the current flow into the EN pin clamp to less than 24 μA to keep the internal clamp within normal operating range. The resistor value can be calculated from the following equation:

$$R_{EN} > \frac{V_{IN,max} - V_{EN,Clamp,min}}{22\ \mu A} \qquad \text{(eq. 2)}$$

Constant On−time Modulation

The FAN23SV65A uses a constant on−time modulation technique, in which the HS MOSFET is turned on for a fixed time, set by the modulator, in response to the input voltage and the frequency setting resistor. This on−time is proportional to the desired output voltage, divided by the input voltage. With this proportionality, the frequency is essentially constant over the load range where inductor current is continuous.

For buck converter in Continuous−Conduction Mode (CCM), the switching frequency f_{SW} is expressed as:

$$f_{SW} = \frac{V_{OUT}}{V_{IN} \times t_{ON}} \qquad \text{(eq. 3)}$$

The on−time generator sets the on−time (t_{ON}) for the high−side MOSFET, which results in the switching frequency of the regulator during steady−state operation. To maintain a relatively constant switching frequency over a wide range of input conditions, the input voltage information is fed into the on−time generator.

t_{ON} is determined by:

$$t_{ON} = \frac{C_{tON}}{I_{tON}} \times 2\ V \qquad \text{(eq. 4)}$$

where I_{tON} is:

$$I_{tON} = \frac{1}{10} \times \frac{V_{IN}}{R_{FREQ}} \qquad \text{(eq. 5)}$$

where R_{FREQ} is the frequency−setting resistor described in the Setting Switching Frequency section; C_{tON} is the internal 2.2 pF capacitor; and I_{tON} is the V_{IN} feed−forward current that generates the on−time.

The FAN23SV65A implements open−circuit detection on the FREQ pin to protect the output from an infinitely long on−time. In the event the FREQ pin is left floating, switching of the regulator is disabled. The FAN23SV65A is designed for V_{IN} input range 7 to 24 V, f_{SW} 200 kHz to 1 MHz, resulting in an I_{tON} ratio exceeding 1 to 15.

As the ratio of V_{OUT} to V_{IN} increases, $t_{OFF,min}$ introduces a limit on the maximum switching frequency as calculated in the following equation, where the factor 1.2 is included in the denominator to provide some headroom for transient operation:

$$f_{SW} =< \frac{\left(1 - \frac{V_{OUT}}{V_{in,min}}\right)}{1.2 \times t_{OFF,min}} \qquad \text{(eq. 6)}$$

Soft−Start (SS)

A conventional soft−start ramp is implemented to provide a controlled startup sequence of the output voltage. A current is generated on the *SS* pin to charge an external capacitor. The lesser of the voltage on the *SS* pin and the reference voltage is used for output regulation.

To reduce V_{OUT} ripple and achieve a smoother ramp of the output voltage, t_{ON} is modulated during soft−start. T_{ON} starts at 50% of the steady−state on−time (PWM Mode) and ramps up to 100% gradually.

During normal operation, the SS voltage is clamped to 400 mV above the FB voltage. The clamp voltage drops to 40 mV during an overload condition to allow the converter to recover using the soft−start ramp once the overload condition is removed. On−time modulation during SS is disabled when an overload condition exists.

To maintain a monotonic soft−start ramp, the regulator is forced into PFM Mode during soft−start. The minimum frequency clamp is disabled during soft−start.

The nominal startup time is programmable through an internal current source charging the external soft−start capacitor C_{SS}:

$$C_{SS} = \frac{I_{SS} \times t_{SS}}{V_{REF}} \qquad \text{(eq. 7)}$$

where:
C_{SS} = External soft−start programming capacitor;
I_{SS} = Internal soft−start charging current source, 10 μA;
t_{SS} = Soft−start time; and
V_{REF} = 600 mV

For example; for 1ms startup time, C_{SS} = 15 nF. The soft−start option can be used for ratiometric tracking. When EN is LOW, the soft−start capacitor is discharged.

Startup on Pre−Bias

FAN23SV65A allows the regulator to start on a pre−bias output, V_{OUT}, and ensures V_{OUT} is not discharged during the soft−start operation.

To guarantee no glitches on V_{OUT} at the beginning of the soft−start ramp, the LS is disabled until the first positivegoing edge of the PWM signal. The regulator is also forced into PFM Mode during soft−start to ensure the inductor current remains positive, reducing the possibility of discharging the output voltage.

Internal Linear Regulator

The FAN23SV65A includes a linear regulator to facilitate single−supply operation for self−biased applications. PVCC is the linear regulator output and supplies power to the internal gate drivers. The PVCC pin should be bypassed with a 2. 2 μF ceramic capacitor. The device can operate from a 5 V rail if the V_{IN}, P_{VIN}, and P_{VCC} pins are connected together to bypass the internal linear regulator.

VCC Bias Supply and UVLO

The V_{CC} rail supplies power to the controller. It is generally connected to the PVCC rail through a lowpass filter of a 10 Ω resistor and 0.1 μF capacitor to minimize any noise sources from the driver supply.

An Under−Voltage Lockout (UVLO) circuit monitors the V_{CC} voltage to ensure proper operation. Once the V_{CC} voltage is above the UVLO threshold, the part begins operation after an initialization routine of 50 μs. There is no UVLO circuitry on either the PVCC or V_{IN} rails.

Pulse Frequency Modulation (PFM)

One of the key benefits of using a constant on−time modulation scheme is the seamless transitions in and out of Pulse Frequency Modulation (PFM) Mode. The PWM signal is not slave to a fixed oscillator and, therefore, can operate at any frequency below the target steady−state frequency. By reducing the frequency during light−load conditions, the efficiency can be significantly improved.

The FAN23SV65A provides a Zero−Crossing Detector (ZCD) circuit to identify when the current in the inductor reverses direction. To improve efficiency at light load, the LS MOSFET is turned off around the zero crossing to eliminate negative current in the inductor. For predictable operation entering PFM mode the controller waits for nine consecutive zero crossings before allowing the LS MOSFET to turn off.

In PFM Mode, f_{SW} varies or modulates proportionally to the load; as load decreases, f_{SW} also decreases. The switching frequency, while the regulator is operating in PFM, can be expressed as:

$$f_{SW} = \frac{2 \times L \times I_{OUT}}{t^2{}_{ON} \times (V_{IN} - V_{OUT})} \times \frac{V_{OUT}}{V_{IN}} \qquad \text{(eq. 8)}$$

where L is inductance and I_{OUT} is output load current.

Minimum Frequency Clamp

To maintain a switching frequency above the audible range, the FAN23SV65A clamps the switching frequency to a minimum value of 18 kHz. The LS MOSFET is turned on to discharge the output and trigger a new PWM cycle. The minimum frequency clamp is disabled during soft−start.

Protection Features

The converter output is monitored and protected against over−current, over−voltage, under−voltage, and hightemperature conditions.

Over−Current Protection (OCP)

The FAN23SV65A uses current information through the LS to implement valley−current limiting. While an OC event is detected, the HS is prevented from turning on and the LS is kept on until the current falls below the user−defined set point. Once the current is below the set point, the HS is allowed to turn on.

During an OC event, the output voltage may droop if the load current is greater than the current the converter is providing. If the output voltage drops below the UV threshold, an overload condition is triggered. During an overload condition, the SS clamp voltage is reduced to

40 mV and the on−time is fixed at the steady−state duration. By nature of the control method; as V_{OUT} drops, the switching frequency is lower due to the reduced rate of inductor current decay during the off−time.

The ILIM pin has an open−detection circuit to provide protection against operation without a current limit.

Under−Voltage Protection (UVP)

If V_{FB} is below the under−voltage threshold of −11% V_{REF} (534 mV), the part enters UVP and PGOOD pulls LOW.

Over−Voltage Protection (OVP)

There are two levels of OV protection: +11% and +22%. During an OV event, PGOOD pulls LOW.

When V_{FB} is > +11% of V_{REF} (666 mV), both HS and LS turn off. By turning off the LS during an OV event, V_{OUT} overshoot can be reduced when there is positive inductor current by increasing the rate of discharge. Once the V_{FB} voltage falls below V_{REF}, the latched OV signal is cleared and operation returns to normal.

A second over−voltage detection is implemented to protect the load from more serious failure. When V_{FB} rises +22% above the V_{REF} (732 mV), the HS turns off until a power cycle on VCC and the LS is forced on until 530 mV of V_{FB}.

Over−Temperature Protection (OTP)

FAN23SV65A incorporates an over−temperature protection circuit that disables the converter when the controller die temperature reaches 155°C. The IC restarts when the die temperature falls below 140°C.

Power Good (PGOOD)

The PGOOD pin serves as an indication to the system that the output voltage of the regulator is stable and within regulation. Whenever V_{OUT} is outside the regulation window or the regulator is at overtemperature (UV, OV, and OT), the PGOOD pin is pulled LOW.

PGOOD is an open−drain output that asserts LOW when V_{OUT} is out of regulation or when OT is detected.

APPLICATION INFORMATION

Stability

Constant on−time stability consists of two parameters: stability criterion and sufficient signal at V_{FB}.

Stability criterion is given by:

$$R_{ESR} \times C_{OUT} >> \frac{t_{ON}}{2} \qquad \text{(eq. 9)}$$

Sufficient signal requirement is given by:

$$\Delta I_{IND} \times R_{ESR} > \Delta V_{FB} \qquad \text{(eq. 10)}$$

where ΔI_{IND} is the inductor current ripple and ΔV_{FB} is the ripple voltage on V_{FB}, which should be ≥ 12 mV.

In certain applications, especially designs utilizing only ceramic output capacitors, there may not be sufficient ripple magnitude available on the feedback pin for stable operation. In this case, an external circuit consisting of 2 resistors (R2 and R6) and 2 capacitors (C4 and C5) can be added to inject ripple voltage into the FB pin (see Figure 1).

There are some specific considerations when selecting the RCC ripple injector circuit. For typical applications, use 4.99 kΩ for R6, the value of C4 can be selected as 0.1 μF and approximate values for R2 and C5 can be determined using the following equations.

R2 must be small enough to develop 12 mV of ripple:

$$R2 < \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times 0.012\ V \times C4 \times f_{SW}} \qquad \text{(eq. 11)}$$

R2 must be selected such that the R2C4 time constant enables stable operation:

$$R2 < \frac{0.33 \times 2\pi \times f_{SW} \times L_{OUT} \times C_{OUT}}{C4} \qquad \text{(eq. 12)}$$

The minimum value of C5 can be selected to minimize the capacitive component of ripple appearing on the feedback pin:

$$C5_{min} = \frac{L_{OUT} \times C_{OUT} \times (R3 + R4)}{R2 \times R3 \times R4 \times C4} \qquad \text{(eq. 13)}$$

Using the minimum value of C5 generally offers the best transient response, and 100 pF is a good initial value in many applications. However, under some operating conditions excessive pulse jitter may be observed. To reduce jitter and improve stability, the value of C5 can be increased:

$$C5 \geq 2 \times C5_{min} \qquad \text{(eq. 14)}$$

5 V PVcc

The PV_{CC} is the output of the internal regulator that supplies power to the drivers and V_{CC}. It is crucial to keep this pin decoupled to PGND with a ≥ 1 μF X5R or X7R ceramic capacitor. Because V_{CC} powers internal analog circuit, it is filtered from PV_{CC} with a 10 Ω resistor and 0.1 μF X7R decoupling ceramic capacitor to AGND.

Setting the Output Voltage (VOUT)

The output voltage V_{OUT} is regulated by initiating a highside MOSFET on−time interval when the valley of the divided output voltage appearing at the FB pin reaches V_{REF}. Since this method regulates at the valley of the output ripple voltage, the actual DC output voltage on V_{OUT} is offset from the programmed output voltage by the average value of the output ripple voltage. The initial V_{OUT} setting of the regulator can be programmed from 0.6 V to 5.5 V by an external resistor divider (R3 and R4):

$$R4 = \frac{R3}{\left(\frac{V_{OUT}}{V_{REF}}\right) - 1} \qquad \text{(eq. 15)}$$

where V_{REF} is 600 mV.

For example; for 1.2 V V_{OUT} and 10 kΩ R3, then R4 is 10 kΩ. For 600 mV V_{OUT}, R4 is left open. V_{FB} is trimmed to a value of 596 mV when V_{REF} = 600 mV, so the final output voltage, including the effect of the output ripple voltage, can be approximated by the equation:

$$V_{OUT} = V_{FB} \times \left[1 + \frac{R3}{R4}\right] + \left[\frac{V_{rip}}{2}\right] \qquad \text{(eq. 16)}$$

Setting the Switching Frequency (fsw)

f_{SW} is programmed through external R_{FREQ} as follows:

$$R_{FREQ} = \frac{V_{OUT}}{20 \times V_{tON} \times f_{SW}} \qquad \text{(eq. 17)}$$

where C_{tON} = 2.2 pF internal capacitor that generates t_{ON}. For example; for f_{SW} = 500 kHz and V_{OUT} = 1.2 V, select a standard value for R_{FREQ} = 54.9 kΩ.

Inductor Selection

The inductor is typically selected based on the ripple current (ΔI_L), which is usually selected as 25% to 45% of the maximum DC load. The inductor current rating should be selected such that the saturation and heating current ratings exceed the intended currents encountered in the application over the expected temperature range of operation. Regulators that require fast transient response use smaller inductance and higher current ripple; while regulators that require higher efficiency keep ripple current on the low side.

The inductor value is given by:

$$L = \frac{(V_{IN} - V_{OUT})}{\Delta I_L \times f_{SW}} \times \frac{V_{OUT}}{V_{IN}} \qquad \text{(eq. 18)}$$

For example: for 19 V V_{IN}, 1.2 V V_{OUT}, 15 A load, 25% ΔI_L, and 500 kHz f_{SW}; L is 576 nH, and a standard value of 560 nH is selected.

Input Capacitor Selection

Input capacitor C_{IN} is selected based on voltage rating, RMS current $I_{CIN(RMS)}$ rating, and capacitance. For capacitors having DC voltage bias derating, such as ceramic capacitors, higher rating is strongly recommended. RMS current rating is given by:

$$I_{CIN(RMS)} = I_{LOAD-MAX} \times \sqrt{D \times (1 - D)} \qquad \text{(eq. 19)}$$

where $I_{LOAD-MAX}$ is the maximum load current and D is the duty cycle V_{OUT}/V_{IN}. The maximum $I_{CIN(RMS)}$ occurs at 50% duty cycle.

The capacitance is given by:

$$C_{IN} = \frac{I_{LOAD-MAX} \times D \times (1 - D)}{f_{SW} \times \Delta V_{IN}} \qquad \text{(eq. 20)}$$

where ΔV_{IN} is the input voltage ripple, normally 1% of V_{IN}.

For example; for V_{IN} = 19 V, ΔV_{IN} = 120 mV, V_{OUT} = 1.2 V, 15 A load, and f_{SW} = 500 kHz; C_{IN} is 14.8 µF and $I_{CIN(RMS)}$ is 3.64 A_{RMS}. Select a minimum of three 10 µF 25 V rated ceramic capacitors with X7R or similar dielectric, recognizing that the capacitor DC bias characteristic indicates that the capacitance value falls approximately 60% at V_{IN} = 19 V, with a resultant small increase in ġV_{IN} ripple voltage above 120 mV used in the calculation. Also, each 10 µF can carry over 3 A_{RMS} in the frequency range from 100 kHz to 1 MHz, exceeding the input capacitor current rating requirements. An additional 0.1 µF capacitor may be needed to suppress noise generated by high frequency switching transitions.

Output Capacitor Selection

Output capacitor C_{OUT} is selected based on voltage rating, RMS current $I_{COUT(RMS)}$ rating, and capacitance. For capacitors having DC voltage bias derating, such as ceramic capacitors, higher rating is highly recommended.

When calculating C_{OUT}, usually the dominant requirement is the current load step transient. If the unloading transient requirement (I_{OUT} transitioning from HIGH to LOW), is satisfied, then the load transient (I_{OUT} transitioning LOW to HIGH), is also usually satisfied. The unloading C_{OUT} calculation, assuming C_{OUT} has negligible parasitic resistance and inductance in the circuit path, is given by:

$$C_{OUT} = L \times \frac{I^2_{MAX} - I^2_{MIN}}{(V_{OUT} + \Delta V_{OUT})^2 - V^2_{OUT}} \qquad \text{(eq. 21)}$$

where I_{MAX} and I_{MIN} are maximum and minimum load steps, respectively and ΔV_{OUT} is the voltage overshoot, usually specified at 3 to 5%.

For example: for V_I = 12 V, V_{OUT} = 1.2 V, 10 A I_{MAX}, 5 A I_{MIN}, f_{SW} = 500 kHz, L_{OUT} = 560 nH, and 4% ΔV_{OUT} deviation of 48 mV; the C_{OUT} value is calculated to be 356 µF. This capacitor requirement can be satisfied using eight 47 µF, 6.3 V−rated X5R ceramic capacitors. This calculation applies for load current slew rates that are faster than the inductor current slew rate, which can be defined as V_{OUT}/L during the load current removal.

Setting the Current Limit

Current limit is implemented by sensing the inductor valley current across the LS MOSFET V_{DS} during the LS on−time. The current limit comparator prevents a new on−time from being started until the valley current is less than the current limit.

The set point is configured by connecting a resistor from the ILIM pin to the SW pin. A trimmed current is output onto the ILIM pin, which creates a voltage across the resistor. When the voltage on ILIM goes negative, an over−current condition is detected.

R_{ILIM} is calculated by:

$$R_{ILIM} = 1.08 \times K_{ILIM} \times I_{VALLEY} \qquad \text{(eq. 22)}$$

where K_{ILIM} is the current source scale factor, and I_{VALLEY} is the inductor valley current when the current limit threshold is reached. The factor 1.08 accounts for the temperature offset of the LS MOSFET compared to the control circuit.

With the constant on−time architecture, HS is always turned on for a fixed on−time; this determines the peak−to−peak inductor current.

Current ripple ΔI is given by:

$$\Delta I_L = \frac{\left(V_{IN} - V_{OUT}\right) \times t_{ON}}{L} \qquad \text{(eq. 23)}$$

From the equation above, the worst−case ripple occurs during an output short circuit (where V_{OUT} is 0 V). This should be taken into account when selecting the current limit set point.

The FAN23SV15M uses valley−current sensing; the current limit (I_{ILIM}) set point is the valley (I_{VALLEY}).

The valley current level for calculating R_{ILIM} is given by:

$$I_{VALLEY} = I_{LOAD(CL)} - \frac{\Delta I_L}{2} \qquad \text{(eq. 24)}$$

where $I_{LOAD\,(CL)}$ is the DC load current when the current limit threshold is reached.

For example: In a converter designed for 15 A steadystate operation and 4.5 A current ripple, the current−limit threshold could be selected at 120% of $I_{LOAD,(SS)}$ to accommodate transient operation and inductor value decrease under loading. As a result, $I_{LOAD,(CL)}$ is 18 A, I_{VALLEY} = 15.75 A, and R_{ILIM} is selected as the standard value of 1.47 kΩ.

Boot Resistor

In some applications, especially with higher input voltage, the V_{SW} ring voltage may exceed derating guidelines of 80% to 90% of absolute rating for V_{SW}. In this situation a resistor can be connected in series with boot capacitor (C3 in Figure 1) to reduce the turn−on speed of the high side MOSFET to reduce the amplitude of the V_{SW} ring voltage. If necessary, a resistor and capacitor snubber can be added from VSW to PGND to reduce the magnitude of the ringing voltage. Please contact ON Semiconductor Customer Support for assistance selecting a boot resistor or snubber circuit in applications that operate above a 21 V typical input voltage.

PRINTED CIRCUIT BOARD (PCB) LAYOUT GUIDELINES

The following points should be considered before beginning a PCB layout using the FAN23SV65A. A sample PCB layout from the evaluation board is shown in Figure 28 – Figure 31 following these layout guidelines.

Power components (input capacitors, output capacitors, inductor, and FAN23SV65A device) should be placed on a common side of the PCB in close proximity to each other and connected using surface copper.

Sensitive analog components including SS, FB, ILIM, FREQ, and EN should be placed away from the highvoltage switching circuits such as SW and BOOT and connected to their respective pins with short traces. The inner PCB layer closest to the FAN23SV65A device should have power ground (PGND) under the power processing portion of the device (PVIN, SW, and PGND). This inner PCB layer should have a separate analog ground (AGND) under the P1 pad and the associated analog components. AGND and PGND should be connected together near the IC between PGND pins 18−21 and AGND pin 23, which connects to P1 thermal pad.

The AGND thermal pad (P1) should be connected to AGND plane on inner layer using four 0.25 mm vias spread under the pad. No vias are included under PVIN (P2) and SW (P3) to maintain the PGND plane under the power circuitry intact.

Power circuit loops that carry high currents should be arranged to minimize the loop area. Primary focus should be to minimize the loop for current flow from the input capacitor to PVIN, through the internal MOSFETs, and returning to the input capacitor. The input capacitor should be as close to the PVIN terminals as possible.

The current return path from PGND at the low−side MOSFET source to the negative terminal of the input capacitor can be routed under the inductor and also through vias that connect the input capacitor and lowside MOSFET source to the PGND region under the power portion of the IC.

The SW node trace that connects the source of the high−side MOSFET and the drain of the low−side MOSFET to the inductor should be short and wide.

To control the voltage across the output capacitor, the output voltage divider should be located close to the FB pin, with the upper FB voltage divider resistor connected to the positive side of the output capacitor and the bottom resistor connected to the AGND portion of the FAN23SV65A device.

When using ceramic capacitors with external ramp injection circuitry (R2, C4, C5 in Figure 1), R2 and C4 should be connected near the inductor and coupling capacitor C5 should be placed near FB pin to minimize FB pin trace length.

Decoupling capacitors for PVCC and VCC should be located close to their respective device pins.

SW node connections to BOOT, ILIM, and ripple injection resistor R2 should be through separate traces.

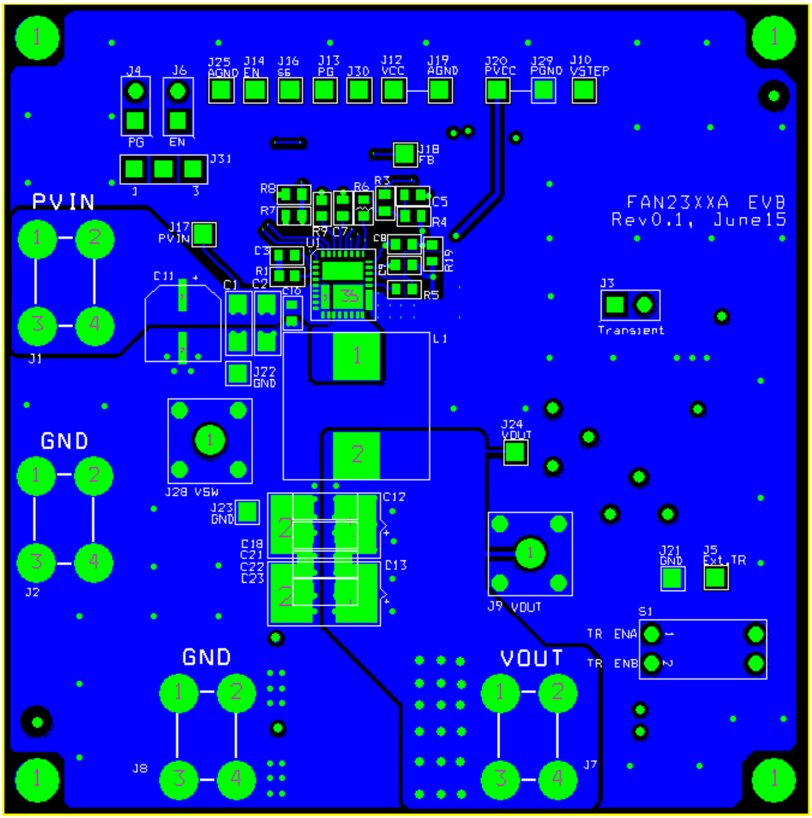


Figure 28. Evaluation Board Top Layer Copper

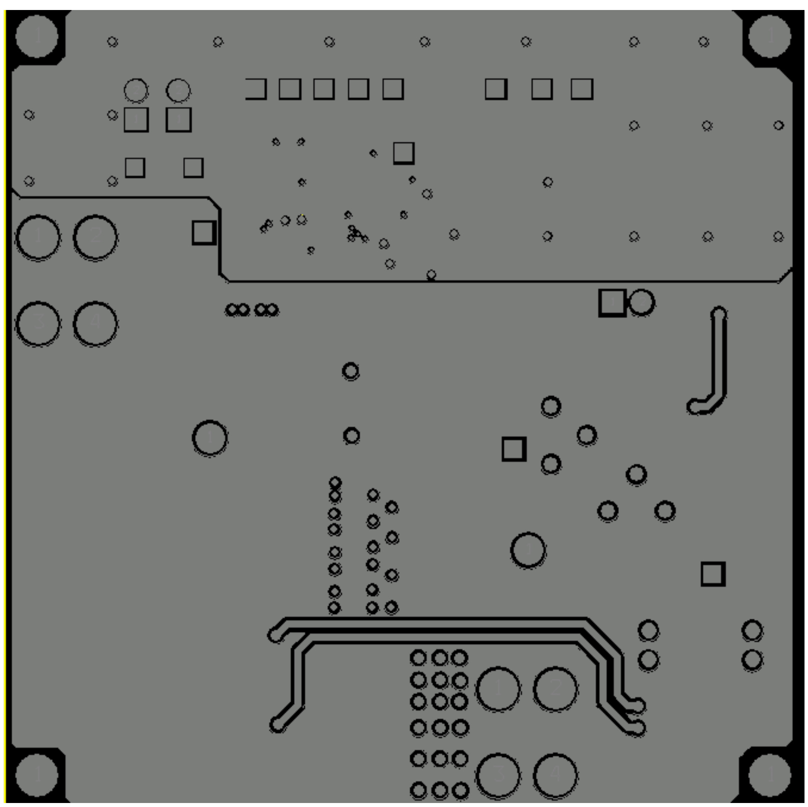


Figure 29. Evaluation Board Inner Layer 1 Copper

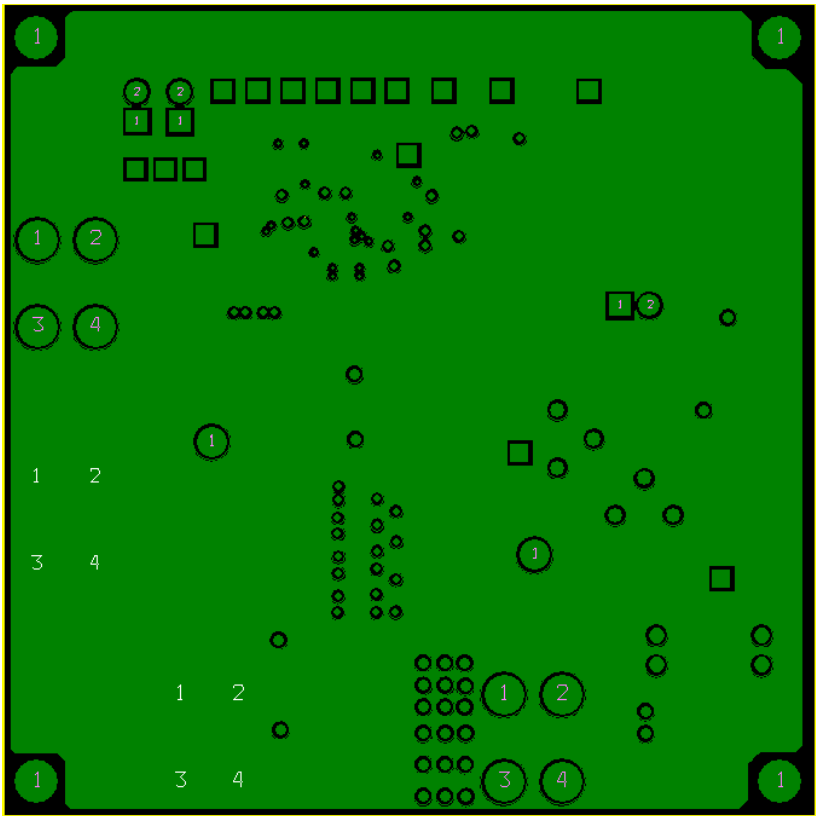


Figure 30. Evaluation Board Top Layer Copper

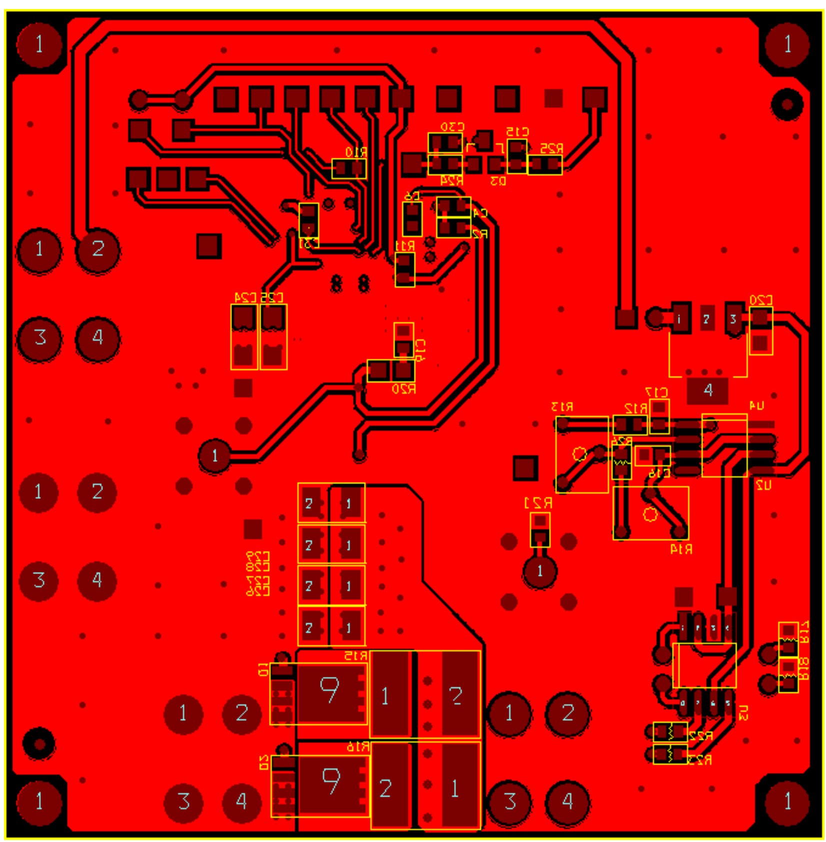


Figure 31. Evaluation Board Inner Layer 1 Copper

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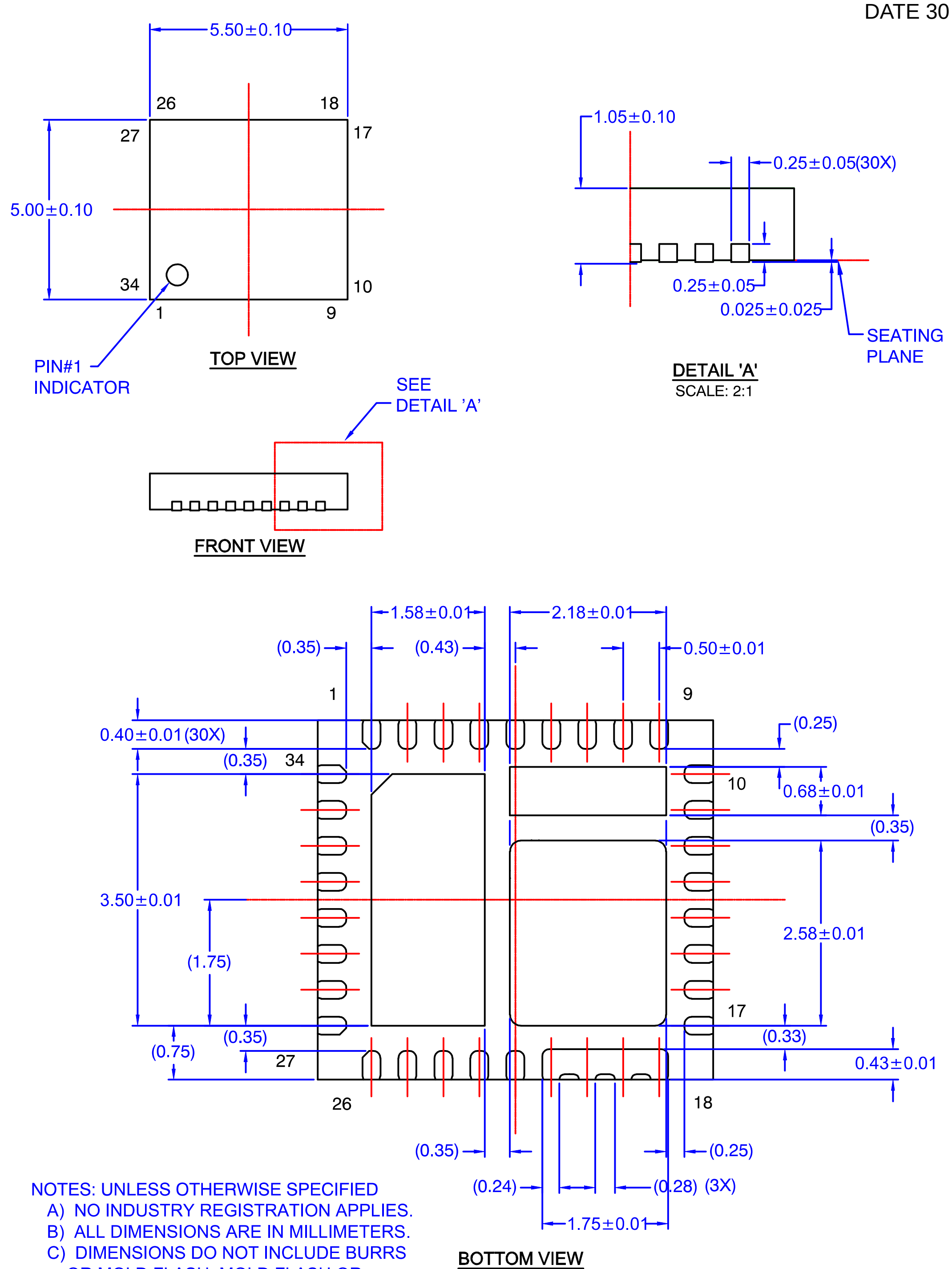

NOTES: UNLESS OTHERWISE SPECIFIED
A) NO INDUSTRY REGISTRATION APPLIES.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.

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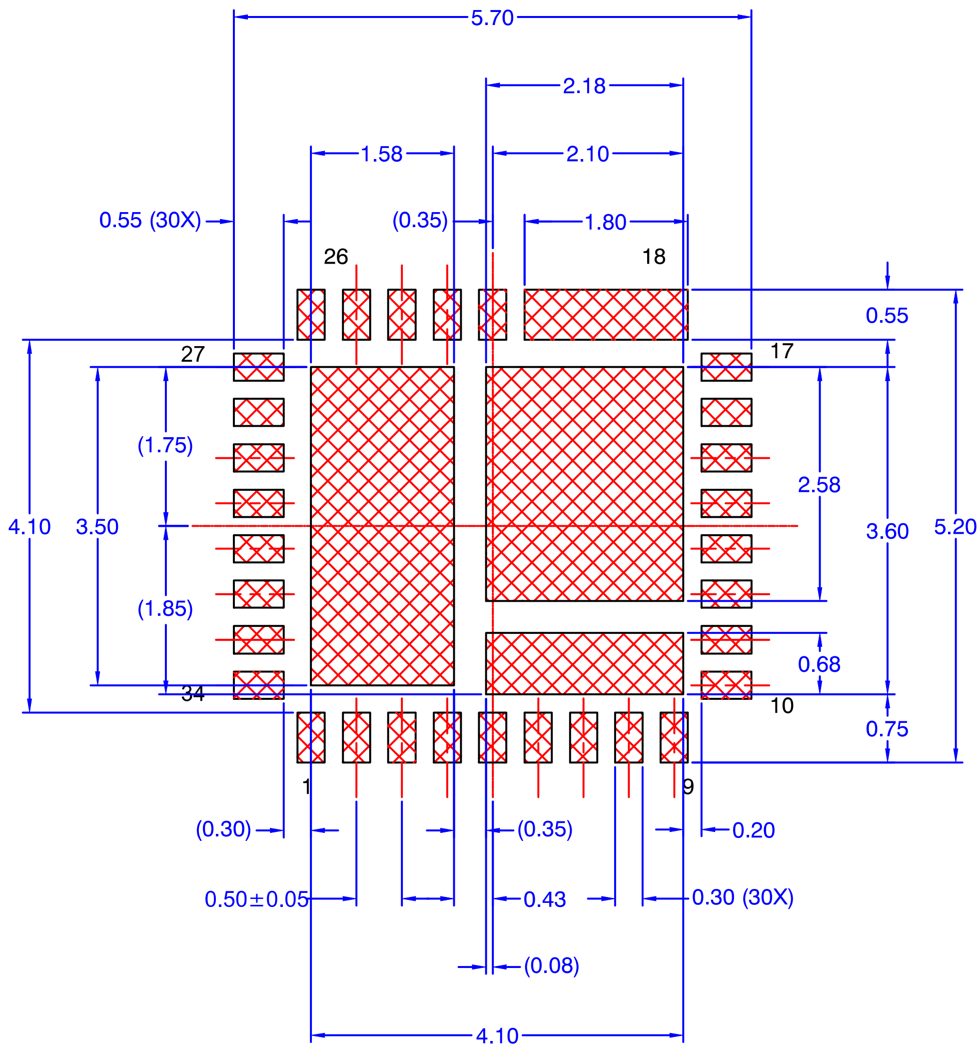

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