NIF62514

Self-protected FET, Temp and Current Limit, Voltage Clamp, ESD, SOT-223

HDPlus devices are an advanced series of power MOSFETs which utilize ON Semiconductor's latest MOSFET technology process to achieve the lowest possible on−resistance per silicon area while incorporating smart features. Integrated thermal and current limits work together to provide short circuit protection. The devices feature an integrated Drain−to−Gate Clamp that enables them to withstand high energy in the avalanche mode. The Clamp also provides additional safety margin against unexpected voltage transients. Electrostatic Discharge (ESD) protection is provided by an integrated Gate−to−Source Clamp.

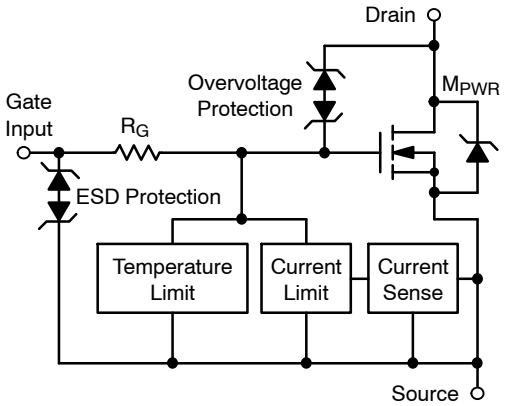
Features

- Current Limitation
- Thermal Shutdown with Automatic Restart
- Short Circuit Protection
- Low $R_{DS(on)}$
- I_{DSS} Specified at Elevated Temperature
- Avalanche Energy Specified
- Slew Rate Control for Low Noise Switching
- Overvoltage Clamped Protection
- This is a Pb−Free Device

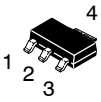
ON Semiconductor®

http://onsemi.com

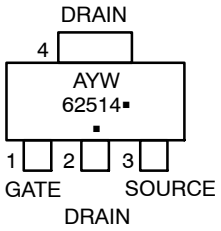
6.0 AMPERES*
40 VOLTS CLAMPED
$R_{DS(on)}$ = 90 mΩ



MARKING DIAGRAM



SOT−223
CASE 318E
STYLE 3



A = Assembly Location
Y = Year
W = Work Week
62514 = Specific Device Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NIF62514T1G	SOT−223 (Pb−Free)	1000/Tape & Reel
NIF62514T3G	SOT−223 (Pb−Free)	4000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

*Limited by the current limit circuit.

MOSFET MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage Internally Clamped	V_{DSS}	40	Vdc
Drain–to–Gate Voltage Internally Clamped (R_{GS} = 1.0 MΩ)	V_{DGR}	40	Vdc
Gate–to–Source Voltage	V_{GS}	±16	Vdc
Drain Current – Continuous @ T_A = 25°C – Continuous @ T_A = 100°C – Pulsed ($t_p \le 10$ μs)	 I_D I_D I_{DM}	Internally Limited	
Total Power Dissipation @ T_A = 25°C (Note 1) @ T_A = 25°C (Note 2) @ T_A = 25°C (Note 3)	P_D	 1.1 1.73 8.93	W
Thermal Resistance, Junction–to–Tab Junction–to–Ambient (Note 1) Junction–to–Ambient (Note 2)	 $R_{\theta JT}$ $R_{\theta JA}$ $R_{\theta JA}$	 14 114 72.3	°C/W
Single Pulse Drain–to–Source Avalanche Energy (V_{DD} = 25 Vdc, V_{GS} = 5.0 Vdc, V_{DS} = 40 Vdc, I_L = 2.8 Apk, L = 80 mH, R_G = 25 Ω)	E_{AS}	300	mJ
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Mounted onto min pad board.
2. Mounted onto 1″ pad board.
3. Mounted onto large heatsink.

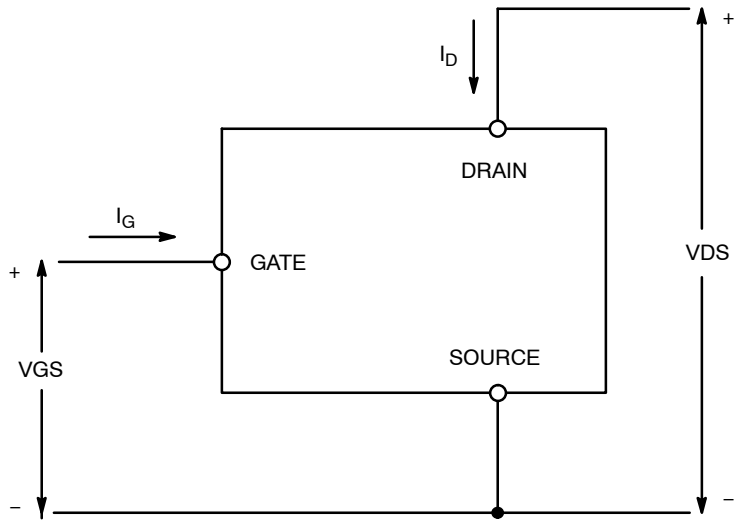


Figure 1. Voltage and Current Convention

MOSFET ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain−to−Source Clamped Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc) (V_{GS} = 0 Vdc, I_D = 250 μAdc, T_J = 150°C) (Note 4)	$V_{(BR)DSS}$	 42 42	 46 45	 50 50	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc, T_J = 150°C) (Note 4)	I_{DSS}	 − −	 0.5 2.0	 2.0 10	μAdc
Gate Input Current (V_{GS} = 5.0 Vdc, V_{DS} = 0 Vdc) (V_{GS} = −5.0 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	 − −	 50 550	 100 1000	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 150 μAdc) Threshold Temperature Coefficient (Negative)	$V_{GS(th)}$	1.0 −	1.7 4.0	2.0 −	Vdc mV/°C
Static Drain−to−Source On−Resistance (Note 5) (V_{GS} = 10 Vdc, I_D = 1.4 Adc, T_J @ 25°C) (V_{GS} = 10 Vdc, I_D = 1.4 Adc, T_J @ 150°C) (Note 4)	$R_{DS(on)}$	 − −	 90 165	 100 190	mΩ
Static Drain−to−Source On−Resistance (Note 5) (V_{GS} = 5.0 Vdc, I_D = 1.4 Adc, T_J @ 25°C) (V_{GS} = 5.0 Vdc, I_D = 1.4 Adc, T_J @ 150°C) (Note 4)	$R_{DS(on)}$	 − −	 105 185	 120 210	mΩ
Source−Drain Forward On Voltage (I_S = 7 A, V_{GS} = 0 V)	V_{SD}	−	1.05	−	V

SWITCHING CHARACTERISTICS (Note 4)

Turn−on Delay Time	10% V_{in} to 10% I_D R_L = 4.7 Ω, V_{in} = 0 to 10 V, V_{DD} = 12 V	$t_{d(on)}$	−	4.0	8.0	μs
Turn−on Rise Time	10% I_D to 90% I_D R_L = 4.7 Ω, V_{in} = 0 to 10 V, V_{DD} = 12 V	t_{rise}	−	11	20	μs
Turn−off Delay Time	90% V_{in} to 90% I_D R_L = 4.7 Ω, V_{in} = 10 to 0 V, V_{DD} = 12 V	$t_{d(off)}$	−	32	50	μs
Turn−off Fall Time	90% I_D to 10% I_D R_L = 4.7 Ω, V_{in} = 10 to 0 V, V_{DD} = 12 V	t_{fall}	−	27	50	μs
Slew−Rate On	R_L = 4.7 Ω, V_{in} = 0 to 10 V, V_{DD} = 12 V	$-dV_{DS}/dt_{on}$	−	1.5	2.5	μs
Slew−Rate Off	R_L = 4.7 Ω, V_{in} = 10 to 0 V, V_{DD} = 12 V	dV_{DS}/dt_{off}	−	0.6	1.0	μs

SELF PROTECTION CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Current Limit	(V_{GS} = 5.0 Vdc) (V_{GS} = 5.0 Vdc, T_J = 150°C) (Note 4)	I_{LIM}	6.0 3.0	9.0 5.0	11 8.0	Adc
Current Limit	(V_{GS} = 10 Vdc) (V_{GS} = 10 Vdc, T_J = 150°C) (Note 4)	I_{LIM}	7.0 4.0	10.5 7.5	13 10	Adc
Temperature Limit (Turn−off) (Note 4)	V_{GS} = 5.0 Vdc	$T_{LIM(off)}$	150	175	200	°C
Temperature Hysteresis (Note 4)	V_{GS} = 5.0 Vdc	$\Delta T_{LIM(on)}$	−	15	−	°C
Temperature Limit (Turn−off) (Note 4)	V_{GS} = 10 Vdc	$T_{LIM(off)}$	150	165	185	°C
Temperature Hysteresis (Note 4)	V_{GS} = 10 Vdc	$\Delta T_{LIM(on)}$	−	15	−	°C

ESD ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Electro−Static Discharge Capability	Human Body Model (HBM)	ESD	4000	−	−	V
Electro−Static Discharge Capability	Machine Model (MM)	ESD	400	−	−	V

4. Not subject to production testing.
5. Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

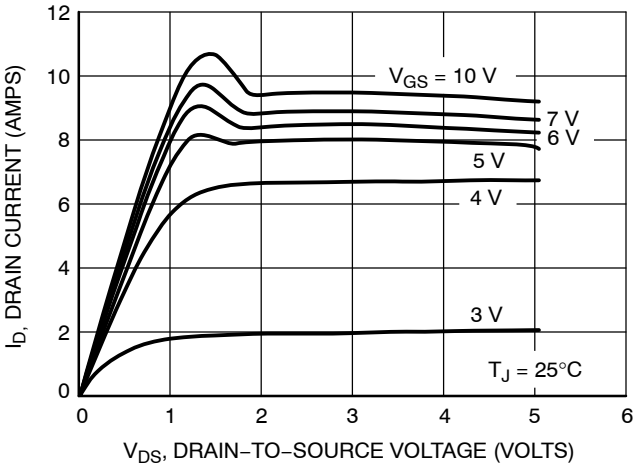


Figure 1. Output Characteristics

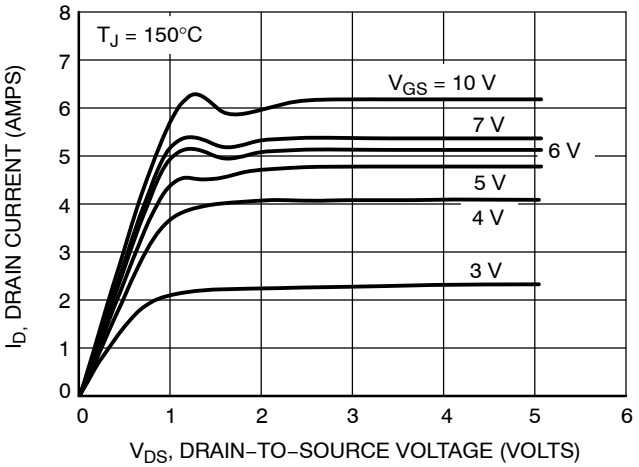


Figure 2. Output Characteristics

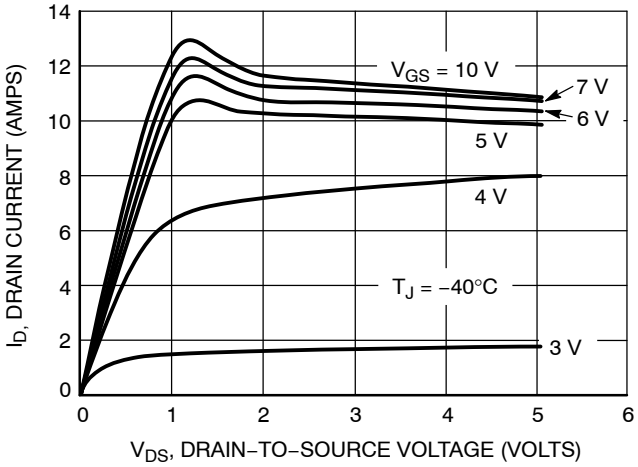


Figure 3. Output Characteristics

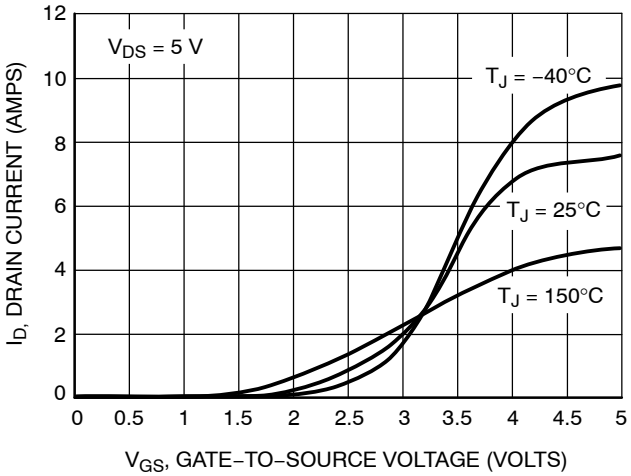


Figure 4. Transfer Characteristics

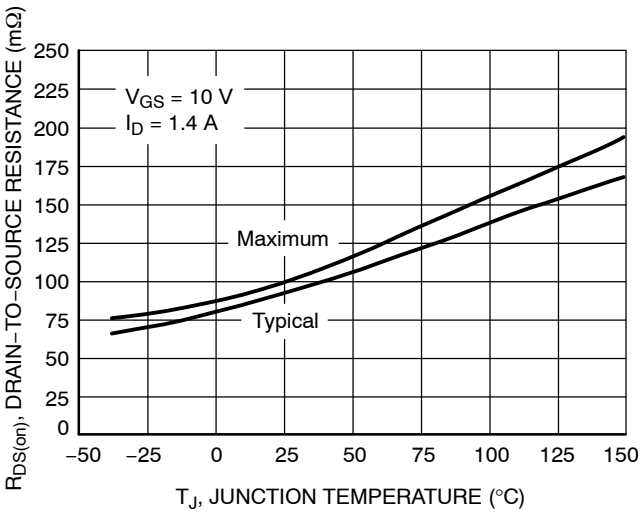


Figure 5. Drain−to−Source Resistance versus Junction Temperature

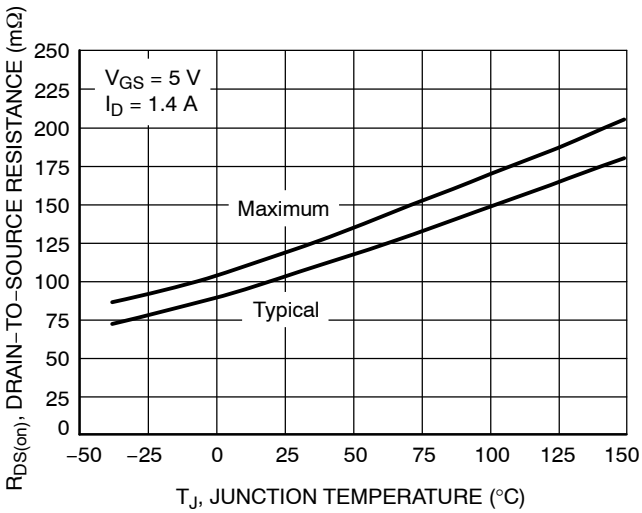


Figure 6. Drain−to−Source Resistance versus Junction Temperature

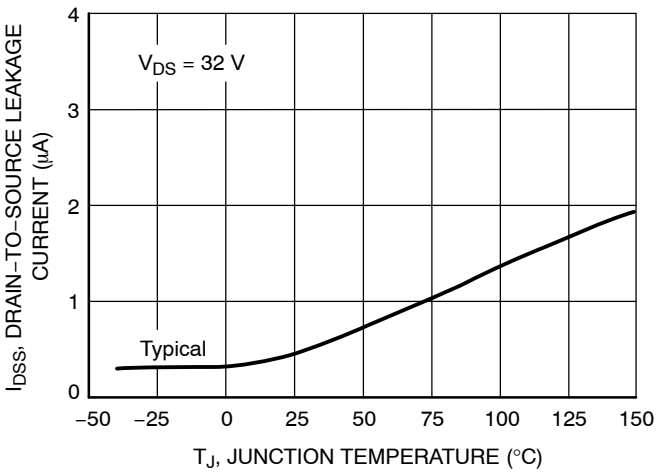


Figure 7. Drain−to−Source Resistance versus Junction Temperature

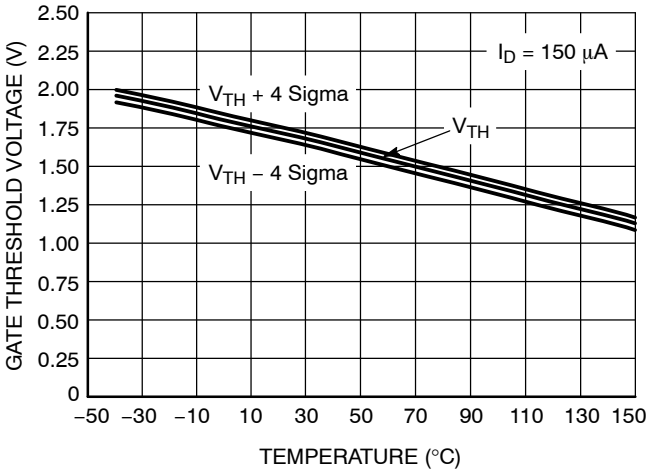


Figure 8. Gate Threshold Voltage versus Temperature

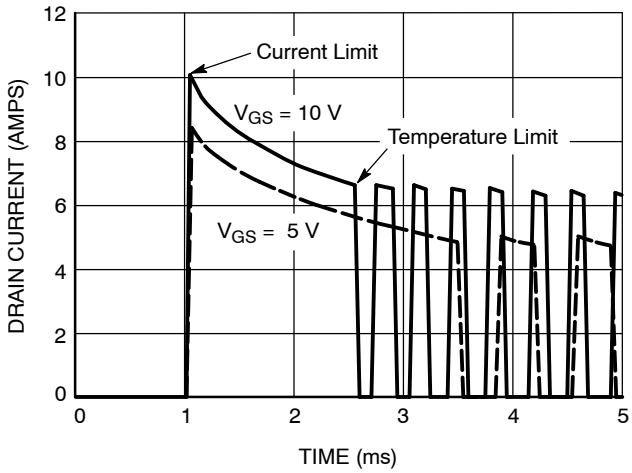


Figure 9. Short−circuit Response

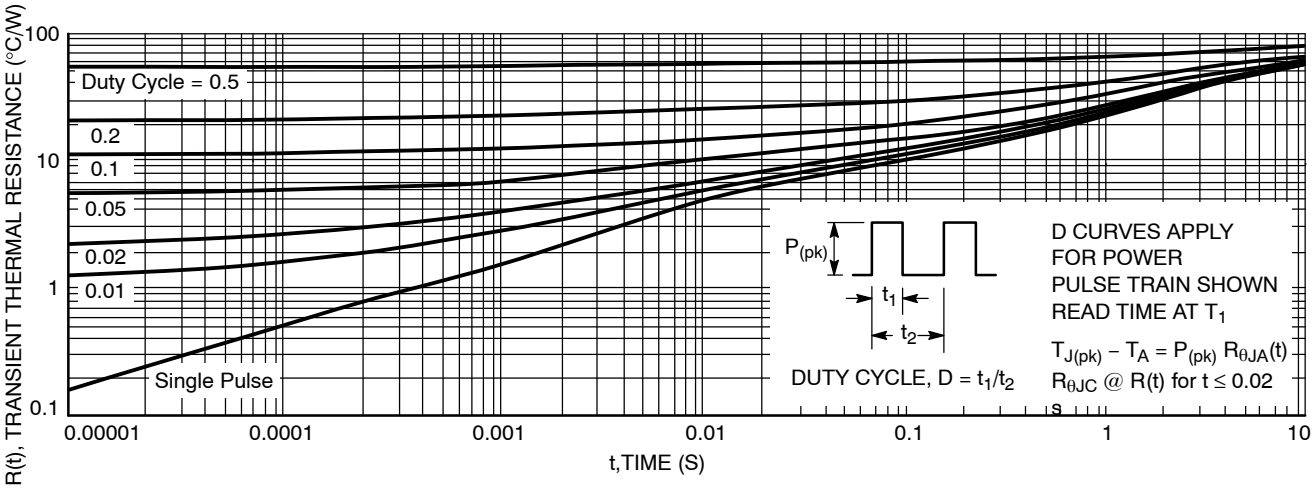


Figure 10. Transient Thermal Resistance (Non−normalized Junction−to−Ambient mounted on minimum pad area)

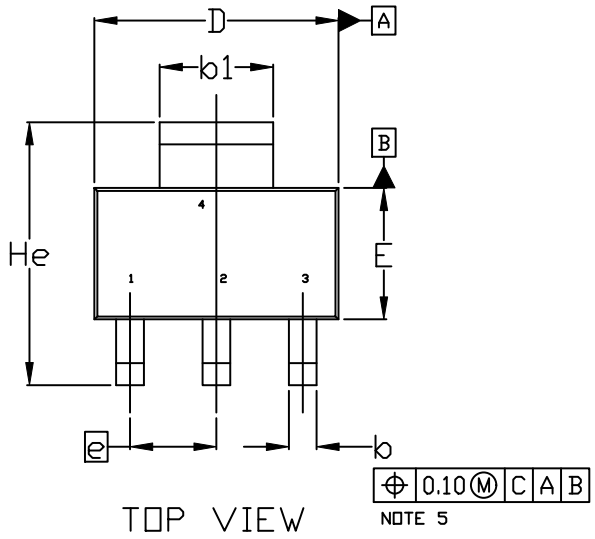
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

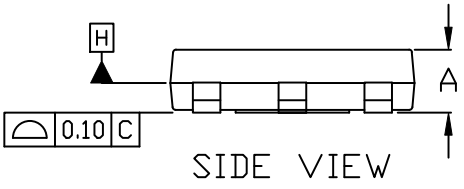
ON Semiconductor®

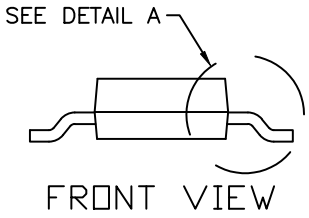
SCALE 1:1

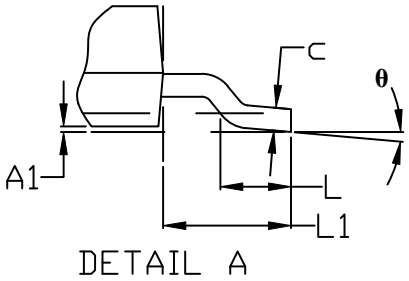
SOT−223 (TO−261)
CASE 318E−04
ISSUE R

DATE 02 OCT 2018



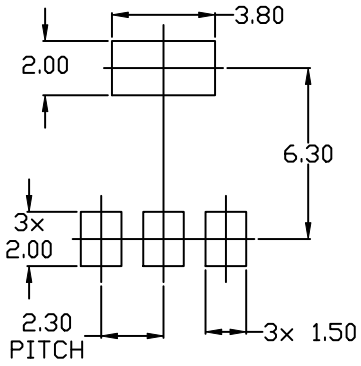






NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.200MM PER SIDE.
4. DATUMS A AND B ARE DETERMINED AT DATUM H.
5. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
6. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	1.50	1.63	1.75
A1	0.02	0.06	0.10
b	0.60	0.75	0.89
b1	2.90	3.06	3.20
c	0.24	0.29	0.35
D	6.30	6.50	6.70
E	3.30	3.50	3.70
e	2.30 BSC		
L	0.20	---	---
L1	1.50	1.75	2.00
He	6.70	7.00	7.30
θ	0°	---	10°



RECOMMENDED MOUNTING FOOTPRINT

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DESCRIPTION:	**SOT−223 (TO−261)**	**PAGE 1 OF 2**

SOT−223 (TO−261)
CASE 318E−04
ISSUE R

DATE 02 OCT 2018

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. CATHODE
3. NC
4. CATHODE

STYLE 3:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 4:
PIN 1. SOURCE
2. DRAIN
3. GATE
4. DRAIN

STYLE 5:
PIN 1. DRAIN
2. GATE
3. SOURCE
4. GATE

STYLE 6:
PIN 1. RETURN
2. INPUT
3. OUTPUT
4. INPUT

STYLE 7:
PIN 1. ANODE 1
2. CATHODE
3. ANODE 2
4. CATHODE

STYLE 8:
CANCELLED

STYLE 9:
PIN 1. INPUT
2. GROUND
3. LOGIC
4. GROUND

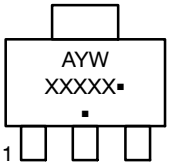
STYLE 10:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 11:
PIN 1. MT 1
2. MT 2
3. GATE
4. MT 2

STYLE 12:
PIN 1. INPUT
2. OUTPUT
3. NC
4. OUTPUT

STYLE 13:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

GENERIC MARKING DIAGRAM*



A = Assembly Location
Y = Year
W = Work Week
XXXXX = Specific Device Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	SOT−223 (TO−261)	PAGE 2 OF 2

PUBLICATION ORDERING INFORMATION

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onsemi Website: www.onsemi.com

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Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:
Phone: 00421 33 790 2910
For additional information, please contact your local Sales Representative

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