NUS3065MU

Low Profile Overvoltage Protection IC with Integrated MOSFET

This device represents a new level of safety and integration by combining the NCP345 overvoltage protection circuit (OVP) with a 30 V P−channel power MOSFET. It is specifically designed to protect sensitive electronic circuitry from overvoltage transients and power supply faults. During such hazardous events, the IC quickly disconnects the input supply from the load, thus protecting the load before any damage can occur.

The OVP IC is optimized for applications that use an external AC−DC adapter or a car accessory charger to power a portable product or recharge its internal batteries. It has a nominal overvoltage threshold of 6.85 V which makes them ideal for single cell Li−Ion as well as 3/4 cell NiCD/NiMH applications.

Features

- OvervoltageTurn−Off Time of Less Than 1.0 μs
- Accurate Voltage Threshold of 6.85 V, Nominal
- Undervoltage Lockout Protection; 2.8 V, Nominal
- High Accuracy Undervoltage Threshold of 2.0%
- −30 V Integrated P−Channel Power MOSFET
- Low $R_{DS(on)}$ = 66 mΩ @ −4.5 V
- Low Profile 0.55 mm height, 2.5 X 3.0 mm LLGA Package Suitable for Portable Applications
- Maximum Solder Reflow Temperature @ 260°C
- This device is manufactured with a Pb−Free external lead finish only.
- This is a Pb−Free Device

Benefits

- Provide Battery Protection
- Integrated Solution Offers Cost and Space Savings
- Integrated Solution Improves System Reliability

Applications

- Portable Computers and PDAs
- Cell Phones and Handheld Products
- Digital Cameras

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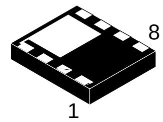
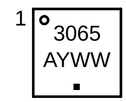
http://onsemi.com

MARKING DIAGRAM

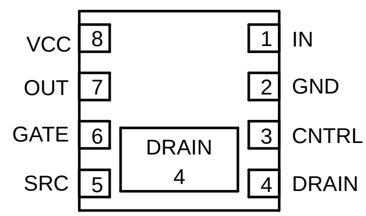


TLLGA8
CASE 517AH



3065	= Specific Device Code
A	= Assembly Location
Y	= Year
WW	= Work Week
▪	= Pb−Free Package

PIN CONNECTIONS



(Bottom View)

ORDERING INFORMATION

Device	Package	Shipping†
NUS3065MUTAG	TLLGA8 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

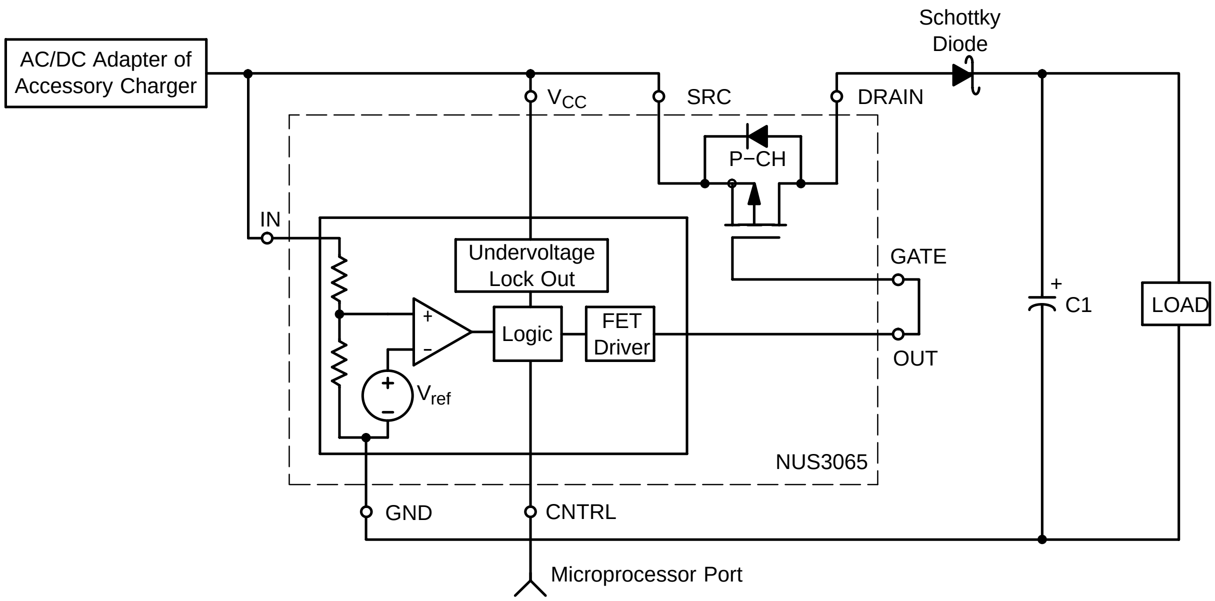


Figure 1. Simplified Schematic

PIN FUNCTION DESCRIPTIONS

Pin #	Symbol	Pin Description
1	IN	This pin senses an external voltage point. If the voltage on this input rises above the overvoltage threshold (V_{TH}), the OUT pin will be driven to within 1.0 V of V_{CC}, thus disconnecting the P−Channel Power MOSFET. The nominal threshold level is 6.85 V and this threshold level can be increased with the addition of an external resistor between IN and V_{CC}.
2	GND	Circuit Ground
3	CNTRL	This logic signal is used to control the state of OUT and turn−on/off the P−Channel Power MOSFET. A logic High results in the OUT signal being driven to within 1.0 V of V_{CC} which disconnects the FET. If this pin is not used, the input should be connected to ground.
4	DRAIN	Drain pin of the P−Channel Power MOSFET
5	SRC	Source pin of the P−Channel Power MOSFET
6	GATE	Gate pin of the P−Channel Power MOSFET
7	OUT	This signal drives the gate of a P−Channel Power MOSFET. It is controlled by the voltage level on IN or the logic state of the CNTRL input. When an overvoltage event is detected, the OUT pin is driven to within 1.0 V of V_{CC} in less than 1.0 _sec provided that gate and stray capacitance is less than 12 nF.
8	V_{CC}	Positive Voltage supply. If V_{CC} falls below 2.8 V (nom), the OUT pin will be driven to within 1.0 V of V_{CC}, thus disconnecting the P−channel FET.

OVERVOLTAGE PROTECTION CIRCUIT TRUTH TABLE

IN	CNTRL	OUT
$<V_{th}$	L	GND
$<V_{th}$	H	V_{CC}
$>V_{th}$	L	V_{CC}
$>V_{th}$	H	V_{CC}

MAXIMUM RATINGS (T_A = 25°C unless otherwise stated)

Rating	Pin	Symbol	Min	Max	Unit
OUT Voltage to GND	7	V_O	−0.3	30	V
Input and CNTRL Pin Voltage to GND	1 3	V_{input} V_{CNTRL}	−0.3 −0.3	30 13	V
VCC Maximum Range	8	$V_{CC(max)}$	−0.3	30	V
Maximum Power Dissipation (Note 1)	−	P_D	−	1.0	W
Thermal Resistance Junction−to−Air (Note 1) OVP IC P−Channel FET	−	$R_{\theta JA}$	−	342 124	°C/W
Junction Temperature	−	T_J	−	150	°C
Operating Ambient Temperature	−	T_A	−40	85	°C
V_{CNTRL} Operating Voltage	3	−	0	5.0	V
Storage Temperature Range	−	T_{stg}	−65	150	°C
ESD Performance (HBM) (Note 2)	1, 2, 3, 7, 8	−	2.5	−	kV
Drain−to−Source Voltage		V_{DSS}		−30	V
Gate−to−Source Voltage		V_{GS}	−20	20	V
Continuous Drain Current, Steady State, T_A = 25°C (Note 1)		I_D		−1.0	A
Drain Current, Peak (Note 1) P_W = 500 μs, T_A = 80°C		I_{DPK}		−4.0	A

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface−mounted on FR4 board using 1 inch sq pad size (Cu area = 1.127 in sq [1 oz] including traces).
2. Human body model (HBM): MIL STD 883C Method 3015−7, (R = 1500 Ω, C = 100 pF, F = 3 pulses delay 1 s).

ELECTRICAL CHARACTERISTICS (T_A = 25°C, Vcc = 6.0 V, unless otherwise specified)

Characteristic	Symbol	Pin	Min	Typ	Max	Unit
V_{CC} Operating Voltage Range	$V_{CC(opt)}$	8	3.0	4.8	25	V
Supply Current (I_{CC} + I_{Input}; V_{CC} = 6.0 V Steady State)	−	1, 8	−	0.75	1.0	mA
Input Threshold (V_{Input} connected to V_{CC}; V_{Input} increasing)	V_{Th}	1	6.65	6.85	7.08	V
Input Hysteresis (V_{Input} connected to V_{CC}; V_{Input} decreasing)	V_{Hyst}	1	50	100	200	mV
Input Impedance (Input = V_{Th})	R_{in}	1	70	150	−	kΩ
CNTRL Voltage High	V_{ih}	3	1.5	−	−	V
CNTRL Voltage Low	V_{il}	3	−	−	0.5	V
CNTRL Current High (V_{ih} = 5.0 V)	I_{ih}	3	−	95	200	μA
CNTRL Current Low (V_{il} = 0.5 V)	I_{il}	3	−	10	20	μA
Undervoltage Lockout (V_{CC} decreasing)	V_{Lock}	3	2.5	2.8	3.0	V
Output Sink Current (V_{CC} < V_{Th}, V_{OUT} = 1.0 V)	I_{Sink}	7	10	33	50	μA
Output Voltage High (V_{CC} = V_{in} = 8.0 V; I_{Source} = 10 mA) Output Voltage High (V_{CC} = V_{in} = 8.0 V; I_{Source} = 0.25 mA) Output Voltage High (V_{CC} = V_{in} = 8.0 V; I_{Source} = 0 mA)	V_{oh}	7	V_{CC}−1.0 V_{CC}−0.25 V_{CC}−0.1	−	−	V
Output Voltage Low (Input < 6.5 V; I_{Sink} = 0 mA; V_{CC} = 6.0 V, CNTRL = 0 V)	V_{ol}	7	−	−	0.1	V
Turn ON Delay − Input (Note 3) (V_{Input} connected to V_{CC}; V_{Input} step down signal from 8.0 to 6.0 V; measured to 50% point of OUT)*	$T_{ON\ IN}$	7	−	−	10	μs
Turn OFF Delay − Input (V_{Input} connected to V_{CC}; V_{Input} step up signal from 6.0 to 8.0 V; C_L = 12 nF Output > V_{CC} − 1.0 V)	$T_{OFF\ IN}$	7	−	0.5	1.0	μs
Turn ON Delay − CNTRL (CNTRL step down signal from 2.0 to 0.5 V; measured to 50% point of OUT) (Note 3)	$T_{ON\ CT}$	7	−	−	10	μs
Turn OFF Delay − CNTRL (CNTRL step up signal from 0.5 to 2.0 V; C_L = 12 nF Output > V_{CC} −1.0 V)	$T_{OFF\ CT}$	7	−	1.0	2.0	μs

3. Guaranteed by design.

P−CHANNEL MOSFET (T_A = 25°C unless otherwise specified)

Parameter	Symbol	Min	Typ	Max	Units
Drain to Source On Resistance (V_{GS} = −4.5 V, I_D = 600 mA) (V_{GS} = −4.5 V, I_D = 1.0 A)	$R_{DS(on)}$		 66 66	 100 100	mΩ
Zero Gate Voltage Drain Current (V_{GS} = 0 V, V_{DS} = −24 V)	I_{DSS}			−1.0	μA
Turn On Delay (Note 4) (V_{GS} = −4.5 V, I_D = −1.0 A, R_G = 6.0 Ω, V_{DS} = 15 V)	t_{on}		11		ns
Turn Off Delay (Note 4) (V_{GS} = −4.5 V, I_D = −1.0 A, R_G = 6.0 Ω, V_{DS} = 15 V)	t_{off}		28		ns
Input Capacitance (Note 3) (V_{GS} = 0 V, f = 1.0 MHz, V_{DS} = −15 V)	C_{in}		750		pF
Gate to Source Leakage Current (V_{GS} = ±20 V, V_{DS} = 0 V)	I_{GSS}		±10		nA
Drain to Source Breakdown Voltage (V_{GS} = 0 V, I_D = −250 μA)	$V_{(BR)DSS}$	30			V
Gate Threshold Voltage (V_{GS} = V_{DS}, I_D = −250 μA)	$V_{(GS)th}$	−3.0		−1.0	V

4. Switching characteristics are independent of operating junction temperature.

TYPICAL PERFORMANCE CURVES

(T_A= 25°C, unless otherwise specified)

OVERVOLTAGE PROTECTION IC

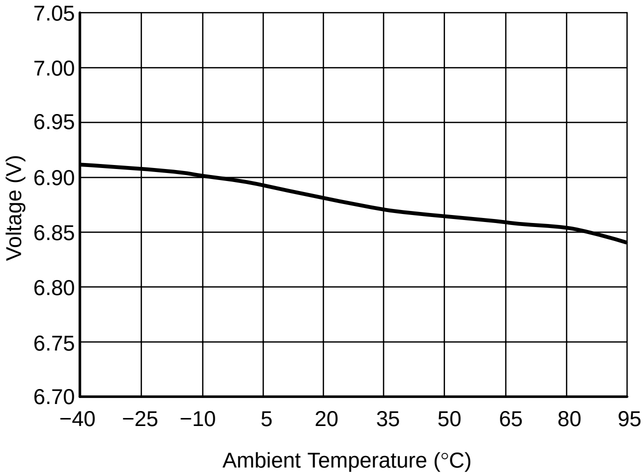


Figure 2. Typical V_{th} Threshold Variation vs. Temperature

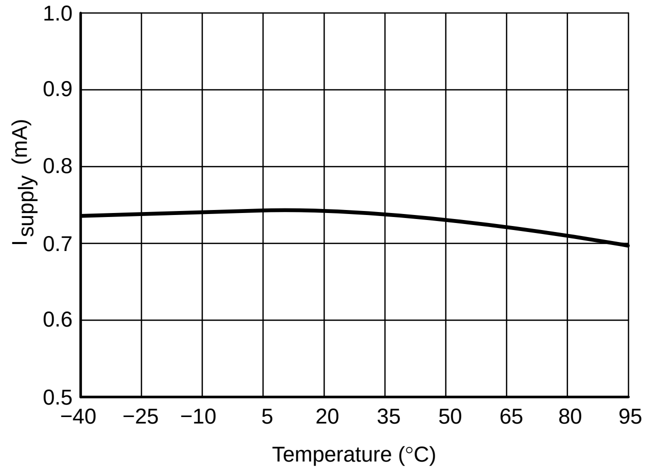


Figure 3. Typical Supply Current vs. Temperature $I_{cc} + I_{in}$, $V_{CC} = 6$ V

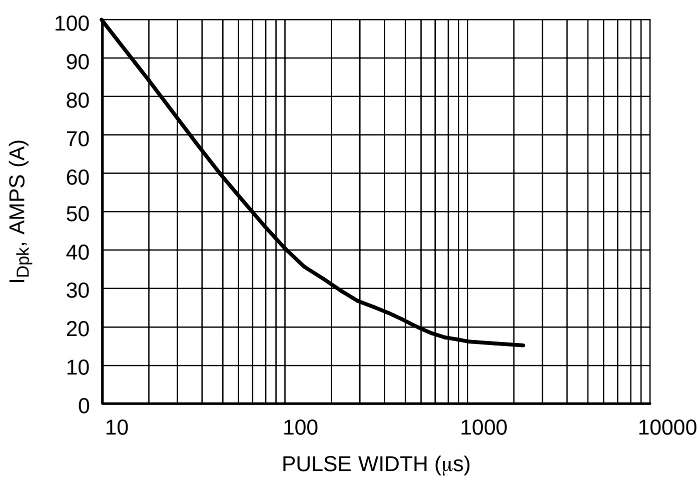


Figure 4. Typical Maximum Drain Peak Current vs Pulse Width (Non−repetitive Single Pulse, V_{GS} = 10 V, T_A = 25°C)

TYPICAL PERFORMANCE CURVES

(T_A= 25°C, unless otherwise specified)

30 V, P−CHANNEL MOSFET

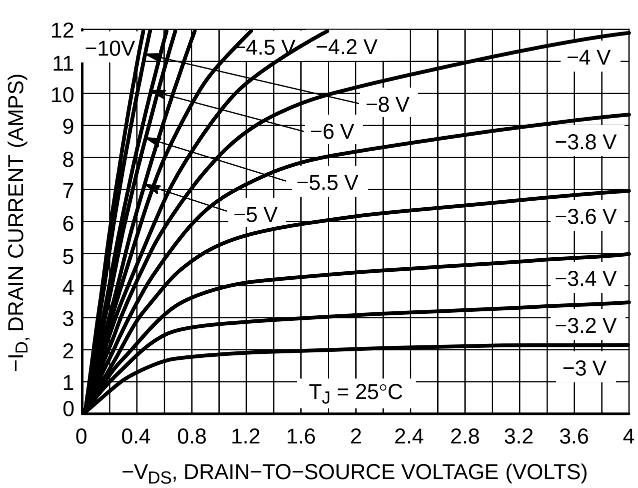


Figure 5. On−Region Characteristics

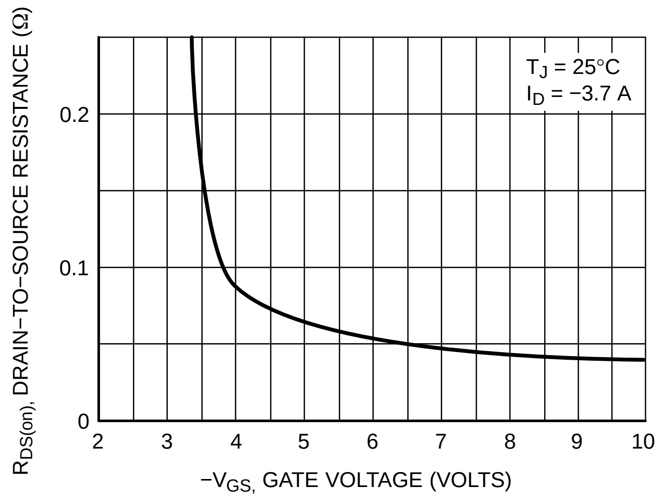


Figure 6. On−Resistance vs. Gate−to−Source Voltage

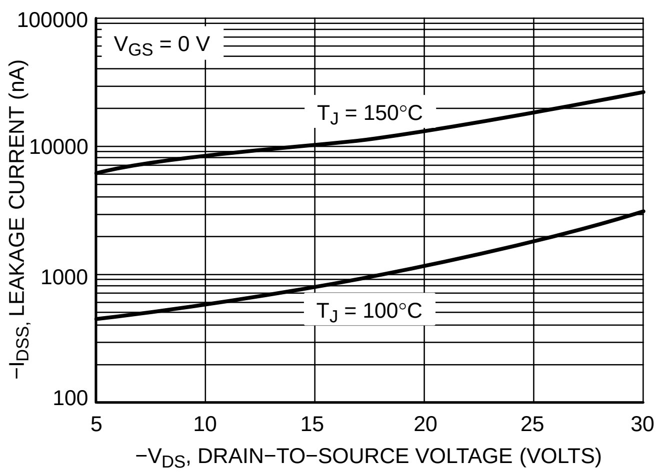


Figure 7. Drain−to−Source Leakage Current vs. Voltage

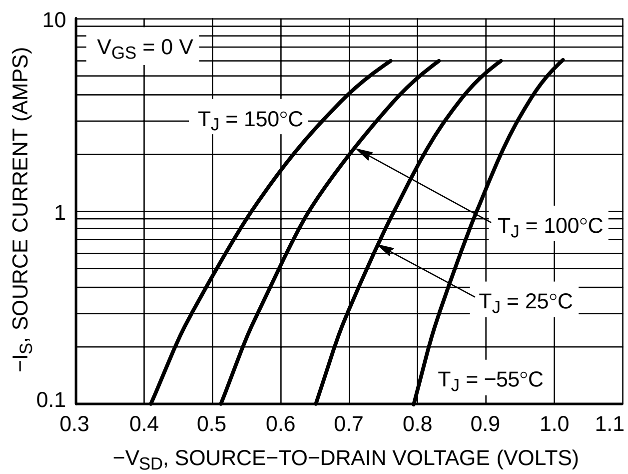


Figure 8. Diode Forward Voltage vs. Current

TYPICAL APPLICATION CIRCUITS & OPERATION WAVEFORMS

(T_A= 25°C, unless otherwise specified)

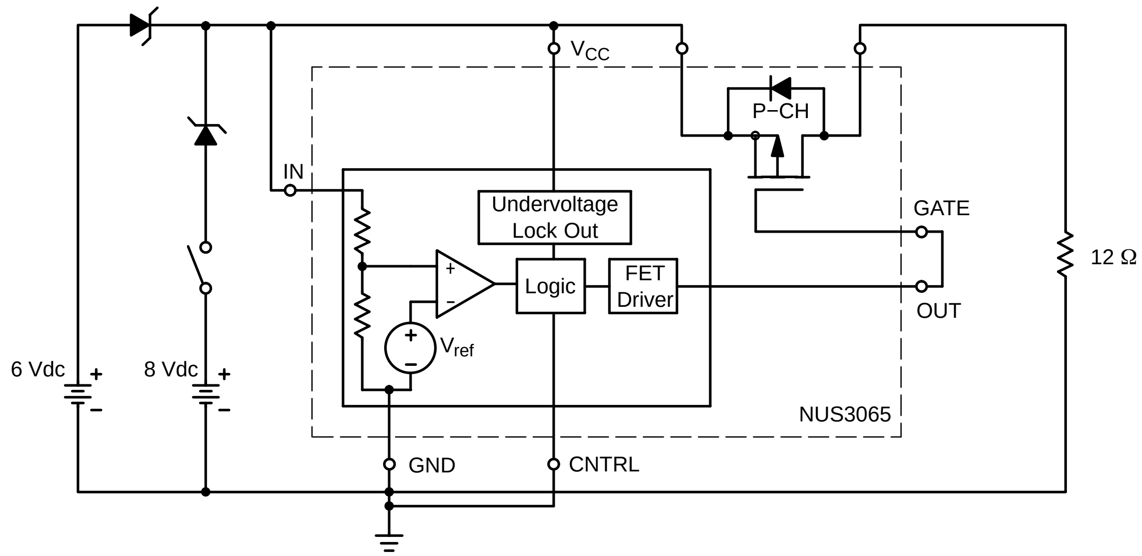


Figure 9. Test Circuit for $T_{ON\ IN}$ and $T_{OFF\ IN}$

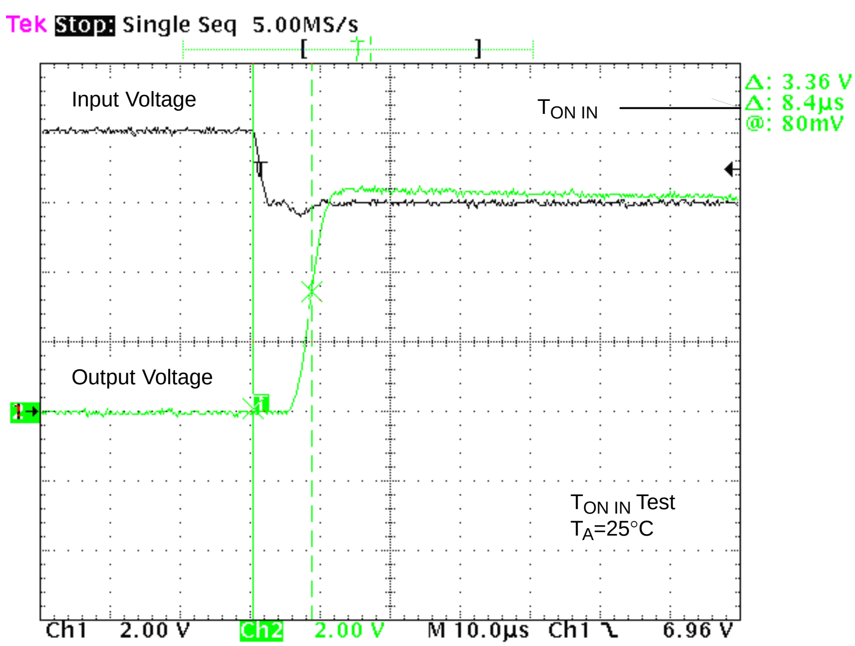


Figure 10. $T_{ON\ IN}$ Waveforms

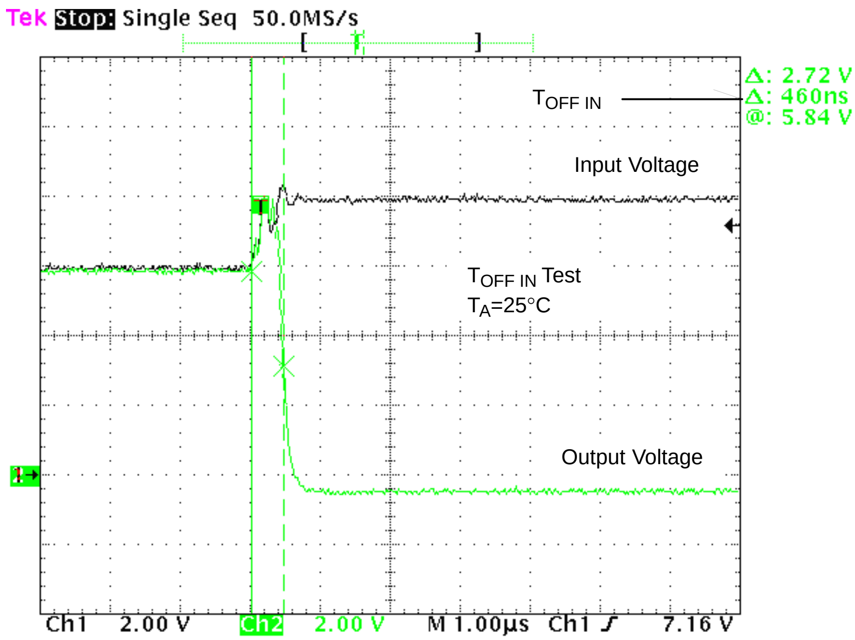


Figure 11. $T_{OFF\ IN}$ Waveforms

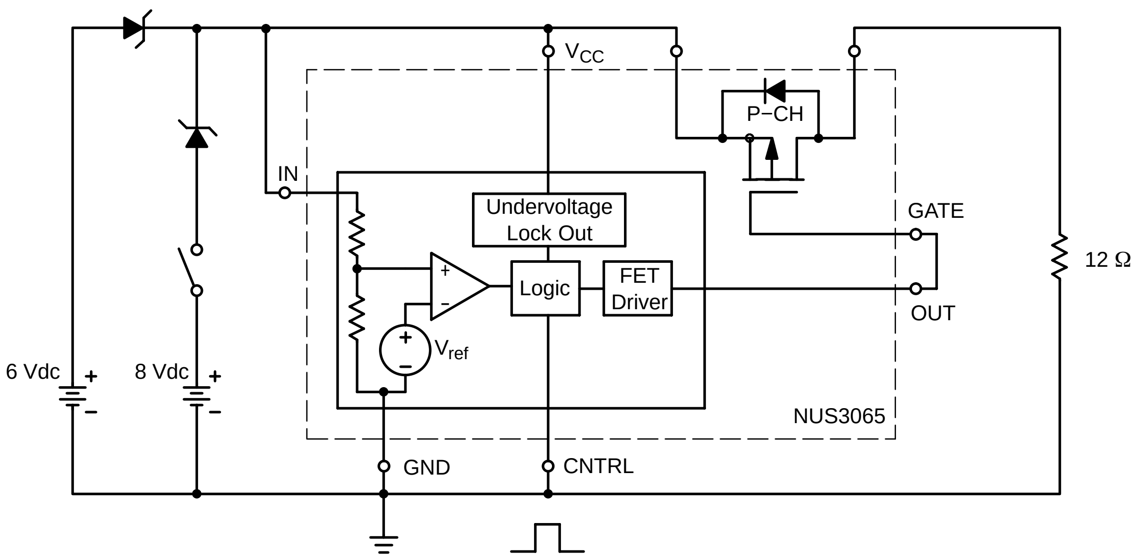


Figure 12. Test Circuit for $T_{ON\ CT}$ and $T_{OFF\ CT}$

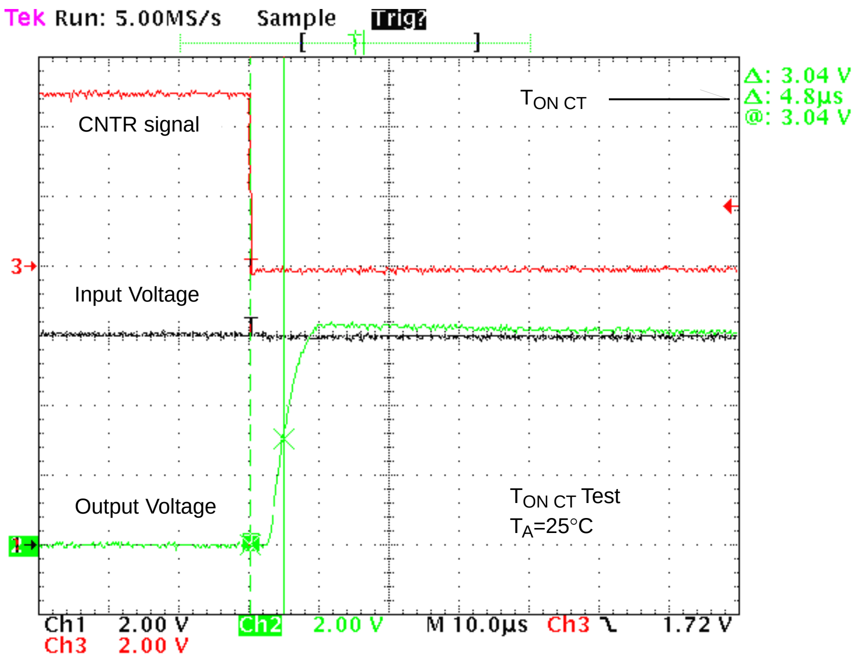


Figure 13. $T_{ON\ CT}$ Waveforms

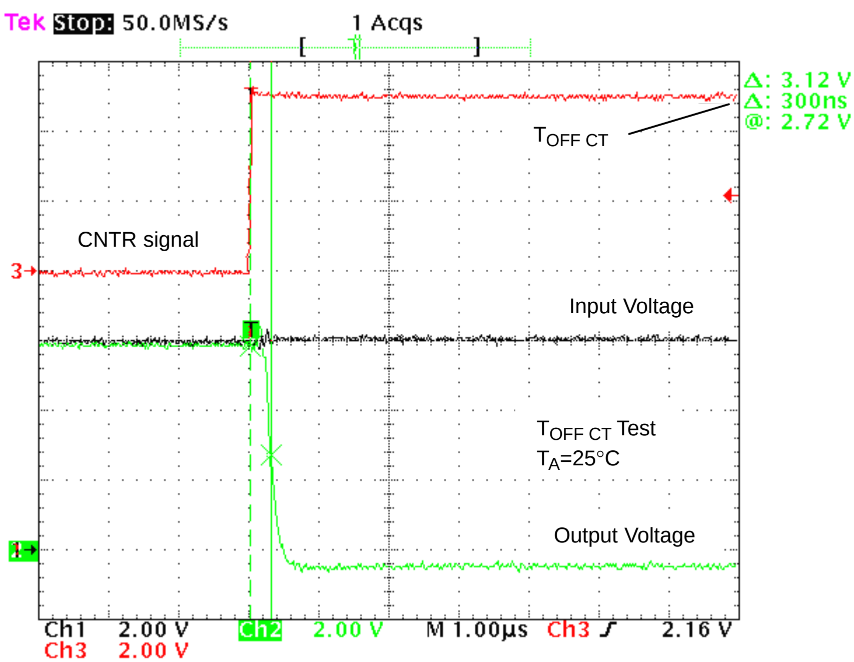
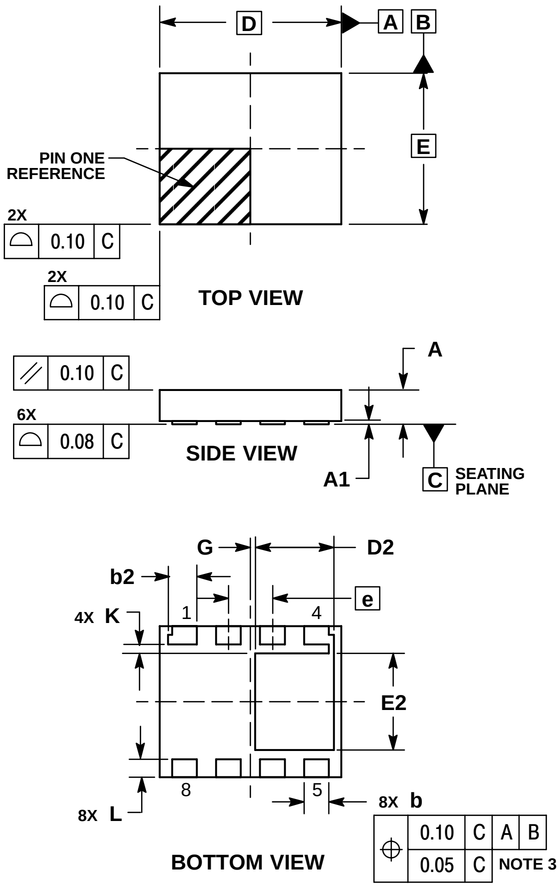


Figure 14. $T_{OFF\ CT}$ Waveforms

PACKAGE DIMENSIONS

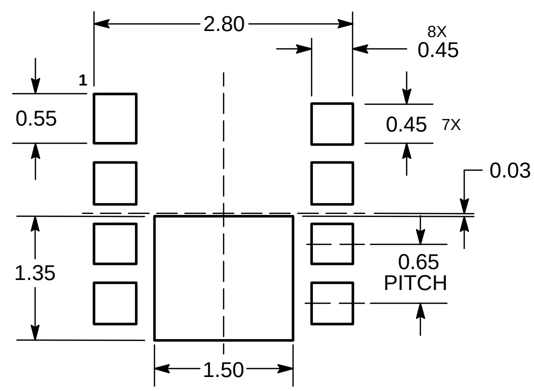
LLGA8 3x2.5, 0.65P
CASE 517AH
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20mm FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.50	0.60
A1	0.00	0.05
b	0.35	0.45
b2	0.45	0.55
D	3.00 BSC	
D2	1.25	1.35
E	2.50 BSC	
E2	1.55	1.65
e	0.65 BSC	
G	0.05 REF	
K	0.15 REF	
L	0.35	0.45

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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