# NCP57152, NCV57152

# Fast Transient Response Regulator, VLDO, 1.5 A

The NCP57152 is a high precision, very low dropout (VLDO), low minimum input voltage and low ground current positive voltage regulator that is capable of providing an output current in excess of 1.5 A with a typical dropout voltage of 330 mV at 1.5 A load current and input voltage from 1.8 V and up. The devices are stable with ceramic output capacitors.

The device can withstand up to 18 V max input voltage. Internal protection features consist of output current limiting, built−in thermal shutdown and reverse output current protection. Logic level enable and error flag pins are available.

The NCP57152 is an Adjustable Voltage device and is available in D2PAK−5 and DFN8 packages.

### Features

- Output Current in Excess of 1.5 A
- Minimum Operating Input Voltage 1.8 V for Full 1.5 A Output Current
- 330 mV Typical Dropout Voltage at 1.5 A
- Adjustable Output Voltage Range from 1.24 V to 13 V
- Low Ground Current
- Fast Transient Response
- Stable with Ceramic Output Capacitor
- Logic Compatible Enable and Error Flag Pins
- Current Limit, Reverse Current and Thermal Shutdown Protection
- Operation up to 13.5 V Input Voltage
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These are Pb−Free Devices

### Applications

- Consumer and Industrial Equipment Point of Regulation
- Servers and Networking Equipment
- FPGA, DSP and Logic Power Supplies
- Switching Power Supply Post Regulation
- Battery Chargers
- Functional Replacement for Industry Standard MIC29150, MIC39150, MIC37150 with Improved Minimum Input Voltage Specification

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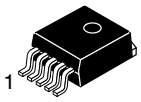
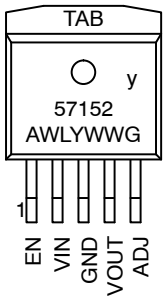
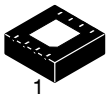
**MARKING DIAGRAMS**




**D²PAK**
**CASE 936A**




**DFN8**
**CASE 488AF**


| | |
|---|---|
| y | = P (NCP), V (NCV) |
| A | = Assembly Location |
| WL, L | = Wafer Lot |
| Y | = Year |
| WW, W | = Work Week |
| G, ▪ | = Pb−Free Package |

(*Note: Microdot may be in either location)

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

## TYPICAL APPLICATIONS

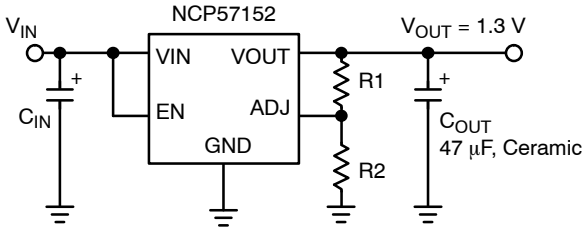



**Figure 1. Adjustable Regulator**

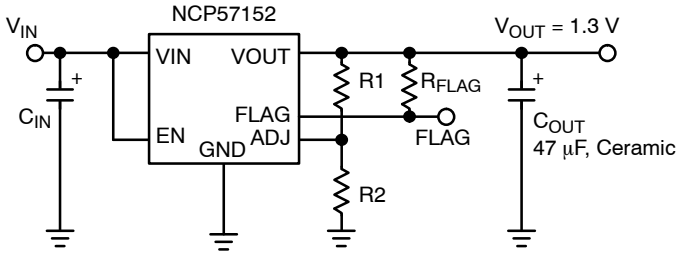



**Figure 2. Adjustable Regulator in DFN Package**

### PIN FUNCTION DESCRIPTION

| Pin Number D2PAK−5 | Pin Number DFN8 | Pin Name | Pin Function |
|---|---|---|---|
| 1 | 2 | EN | Enable Input: CMOS and TTL logic compatible. Logic high = enable; Logic low = shutdown. |
| 2 | 3 | VIN | Input voltage which supplies both the internal circuitry and the current to the output load. |
| 3 | 1 | GND | Ground |
| 4 | 6 | VOUT | Linear Regulator Output. |
| 5 | 7 | ADJ | Adjustable Regulator Feedback Input.<br>Connect to output voltage resistor divider central node. |
| TAB | – | TAB | TAB is connected to ground. |
| – | 8 | FLG | Error Flag Open collector output.<br>Active−low indicates an output fault condition. |
| – | EP | EXPOSED PAD | PAD for removing heat from the device. Must be connected to GND. |
| – | 4, 5 | NC | Not internally connected. |

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Rating | Value | Unit |
|---|---|---|---|
| $V_{IN}$ | Supply Voltage | 0 to 18 | V |
| $V_{EN}$ | Enable Input Voltage | 0 to 18 | V |
| $V_{FLG}$ | Error Flag Open Collector Output Maximum Voltage | 0 to 18 | V |
| $V_{OUT} - V_{IN}$ | Reverse $V_{OUT} - V_{IN}$ Voltage (EN = Shutdown or Vin = 0 V) (Note 1) | 0 to 6.5 | V |
| $P_D$ | Power Dissipation (Notes 2 and 5) | Internally Limited | |
| $T_J$ | Junction Temperature | $-40 \le T_J \le +125$ | °C |
| $T_S$ | Storage Temperature | $-65 \le T_J \le +150$ | °C |
| | ESD Rating (Notes 3 and 4) Human Body Model<br>Machine Model | 2000<br>200 | V |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

NOTE: All voltages are referenced to GND pin unless otherwise noted.

1. The ENABLE pin input voltage must be ≤ 0.8 V or Vin must be connected to ground potential.
2. $P_{D(max)} = (T_{J(max)} - T_A) / R_{\theta JA}$, where $R_{\theta JA}$ depends upon the printed circuit board layout.
3. Devices are ESD sensitive. Handling precautions recommended..
4. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model (HBM) tested per AEC−Q100−002 (EIA/JESD22−A114C)
   ESD Machine Model (MM) tested per AEC−Q100−003 (EIA/JESD22−A115C)
   This device contains latch−up protection and exceeds 100 mA per JEDEC Standard JESD78.
5. This protection is not guaranteed outside the Recommended Operating Conditions.

## RECOMMENDED OPERATING CONDITIONS (Note 6)

| Symbol | Rating | Value | Unit |
|---|---|---|---|
| $V_{IN}$ | Supply Voltage | 1.8 to 13.5 | V |
| $V_{EN}$ | Enable Input Voltage | 0 to 13.5 | V |
| $V_{FLG}$ | Error Flag Open Collector Voltage | 0 to 13.5 | V |
| $T_J$ | Junction Temperature | $-40 \le T_J \le +125$ | °C |

6. The device is not guaranteed to function outside it's Recommended operating conditions.

## ELECTRICAL CHARACTERISTICS

$T_J$ = 25°C with $V_{IN}$ = $V_{OUT\ nominal}$ + 0.6 V; $V_{EN}$ = $V_{IN}$; $I_L$ = 10 mA; bold values indicate –40°C < $T_J$ < +125°C, unless noted. (Note 7)

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Output Voltage Accuracy DFN package | $I_L$ = 10 mA | –1 | | 1 | % |
| | 10 mA < $I_{OUT}$ < 1.5 A , $V_{OUT\ nominal}$ + 0.6 ≤ $V_{IN}$ ≤ 13.5 V | **–2** | | **2** | % |
| Output Voltage Accuracy D2PAK package | IL = 10 mA | –1.5 | | 1.5 | % |
| | 10 mA < $I_{OUT}$ < 1.5 A , $V_{OUT\ nominal}$ + 0.6 ≤ $V_{IN}$ ≤ 13.5 V | **–2.5** | | **2.5** | % |
| Output Voltage Line Regulation | $V_{IN}$ = $V_{OUT\ nominal}$ + 0.6 V to 13.5 V; $I_L$ = 10 mA | | 0.02 | 0.5 | % |
| Output Voltage Load Regulation | $I_L$ = 10 mA to 1.5 A | | 0.2 | 1.0 | % |
| $V_{IN}$ – $V_{OUT}$ Dropout Voltage (Note 8) | $I_L$ = 500 mA (Note 9) | | 180 | **295** | mV |
| | $I_L$ = 750 mA | | 220 | **350** | mV |
| | $I_L$ = 1.0 A (Note 9) | | 260 | **410** | mV |
| | $I_L$ = 1.5 A | | 330 | **520** | mV |
| Ground Pin Current (Note 10) | $I_L$ = 1.5 A | | 40 | 60<br>**80** | mA |
| Ground Pin Current in Shutdown | $V_{EN}$ ≤ 0.5 V | | 1.0 | 5.0 | μA |
| Overload Protection Current Limit | $V_{OUT}$ = 0 V | | 2.0 | **3.0** | A |
| Start–up Time | $V_{EN}$ = $V_{IN}$, $V_{OUT}$ nominal = 2.5 V, $I_{OUT}$ = 10 mA, $C_{OUT}$ = 47 μF | | 100 | 500 | μs |
| Output Voltage Start–up Slope | $V_{EN}$ = $V_{IN}$, $I_{OUT}$ = 10 mA, $C_{OUT}$ = 47 μF (Note 11) | | 40 | 200 | μs/V |
| Reference Voltage DFN Package<br>$D^2PAK$ Package | | 1.228<br>**1.215**<br>1.221<br>**1.209** | 1.240<br><br>1.240 | 1.252<br>**1.265**<br>1.259<br>**1.271** | V |
| Adjust Pin Bias Current | | | 100 | 200<br>**350** | nA |

### ENABLE INPUT

| | | | | | |
|---|---|---|---|---|---|
| Enable Input Signal Levels | Regulator Enable | **1.4** | | | V |
| | Regulator Shutdown | | | **0.8** | V |
| Enable Pin Input Current | $V_{EN}$ ≤ 0.8 V (Regulator Shutdown) | | | 2.0<br>**4.0** | μA |
| | 6.5 V > $V_{EN}$ ≥ 1.4 V (Regulator enable) | | 15 | 30<br>**40** | μA |

### FLAG OUTPUT

| | | | | | |
|---|---|---|---|---|---|
| $I_{FLG(leak)}$ | $V_{oh}$ = 13.5 V, Flag OFF | | | 1.0<br>**2.0** | μA |
| $V_{FLG(LO)}$ | $V_{IN}$ = 1.8 V, $I_{FLG}$ = 1 mA, Flag ON | | 210 | 400<br>**500** | mV |
| $V_{FLG}$ | Low Threshold, % of particular $V_{OUT}$ | 93 | 95 | | % |
| | Hysteresis, % of particular $V_{OUT}$ | | 2 | | % |
| | High Threshold, % of particular $V_{OUT}$ | | 97 | 99.2 | % |

7. $V_{OUTnominal}$ can be set by external resistor divider in the application. Tested for $V_{OUTnominal}$ = 1.24 V unless noted.
8. $V_{DO}$ = $V_{IN}$ – $V_{OUT}$ when $V_{OUT}$ decreases to 98% of its nominal output voltage with $V_{IN}$ = $V_{OUT}$ + 1 V. Tested for $V_{OUTnominal}$ = 2.5 V.
9. Guaranteed by design.
10. $I_{IN}$ = $I_{GND}$ + $I_{OUT}$.
11. Device Start–up Time = Output Voltage Start–up Slope * $V_{OUT}$ nominal.

| Package | Conditions / PCB Footprint | Thermal Resistance |
|---|---|---|
| D2PAK–5, Junction–to–Case | | $R_{\theta JC}$ = 2.1°C/W |
| D2PAK–5, Junction–to–Air | PCB with 100 $mm^2$ 2.0 oz Copper Heat Spreading Area | $R_{\theta JA}$ = 52°C/W |
| DFN8, Junction–to–Air | PCB with 500 $mm^2$ 2.0 oz Copper Heat Spreading Area | $R_{\theta JA}$ = 75°C/W |

## TYPICAL CHARACTERISTICS

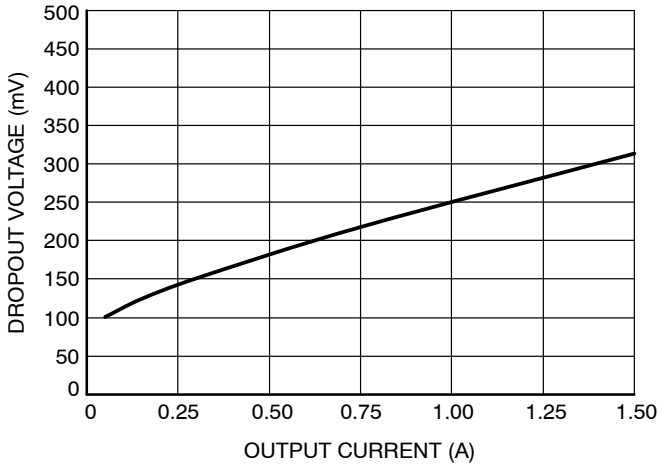



**Figure 3. Dropout Voltage vs. Output Current ($V_{OUTnom}$ = 2.5 V)**

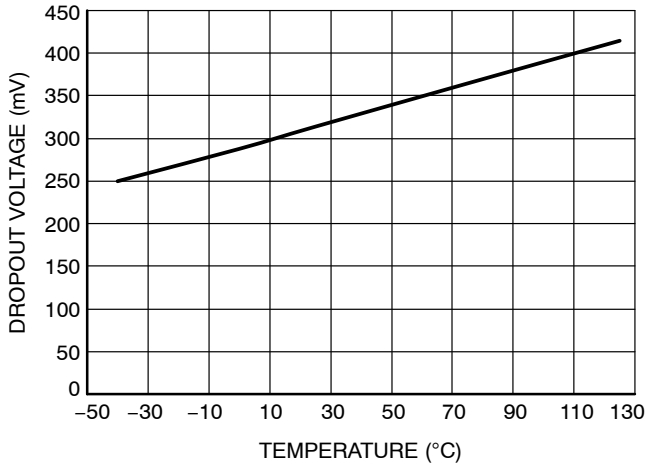



**Figure 4. Dropout Voltage vs. Temperature ($V_{OUTnom}$ = 2.5 V, $I_{OUT}$ = 1.5 A)**

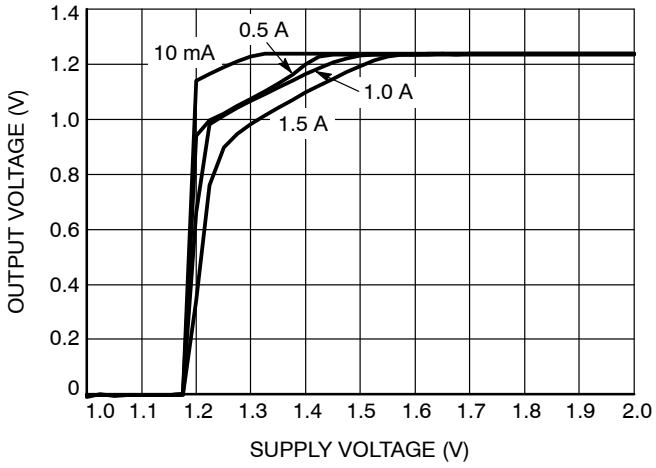



**Figure 5. Dropout Characteristics ($V_{OUTnom}$ = 1.24 V)**

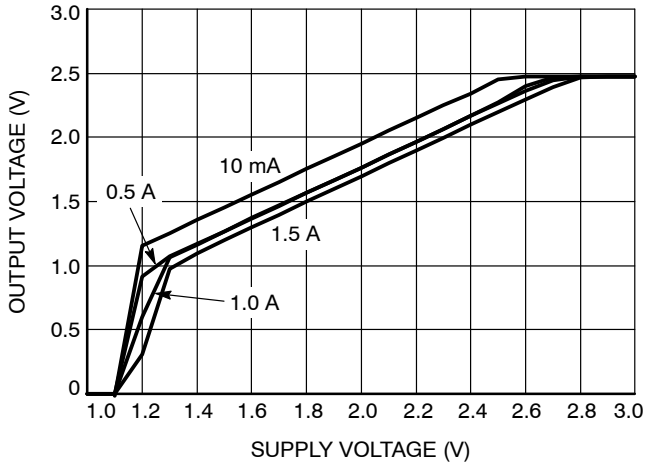



**Figure 6. Dropout Characteristics ($V_{OUTnom}$ = 2.5 V)**

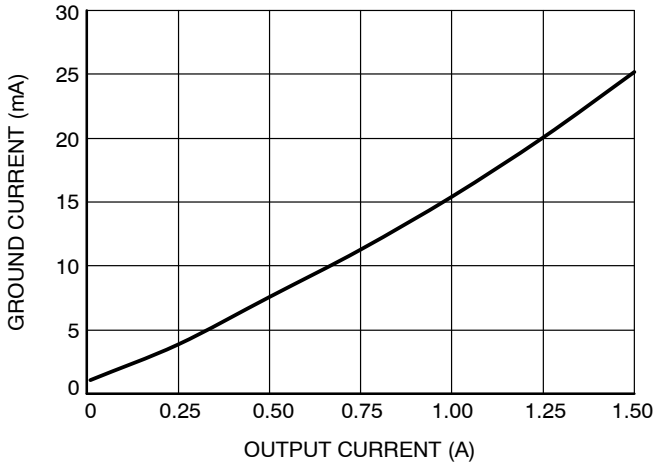



**Figure 7. Ground Current vs. Output Current ($V_{OUTnom}$ = 1.24 V)**

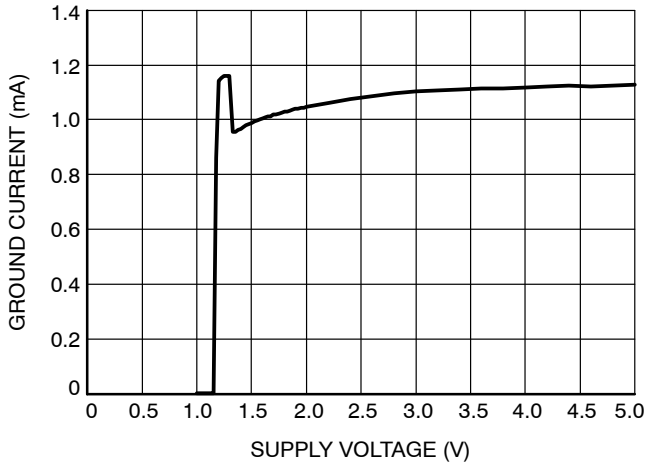



**Figure 8. Ground Current vs. Supply Voltage ($V_{OUTnom}$ = 1.24 V, $I_{OUT}$ = 10 mA)**

## TYPICAL CHARACTERISTICS

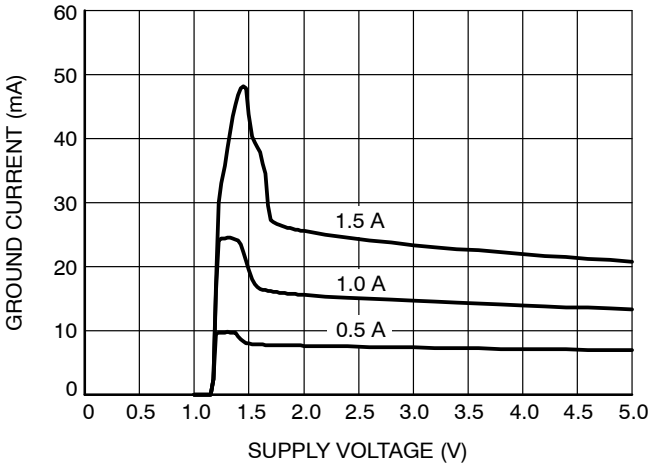



**Figure 9. Ground Current vs. Supply Voltage ($V_{OUTnom}$ = 1.24 V)**

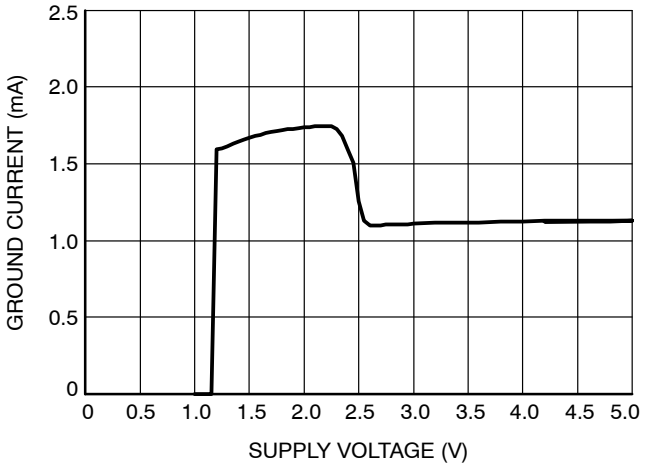



**Figure 10. Ground Current vs. Supply Voltage ($V_{OUTnom}$ = 2.5 V, $I_{OUT}$ = 10 mA)**

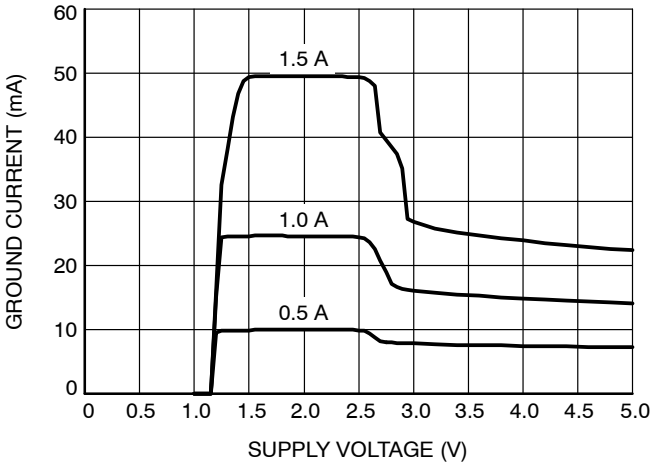



**Figure 11. Ground Current vs. Supply Voltage ($V_{OUTnom}$ = 2.5 V)**

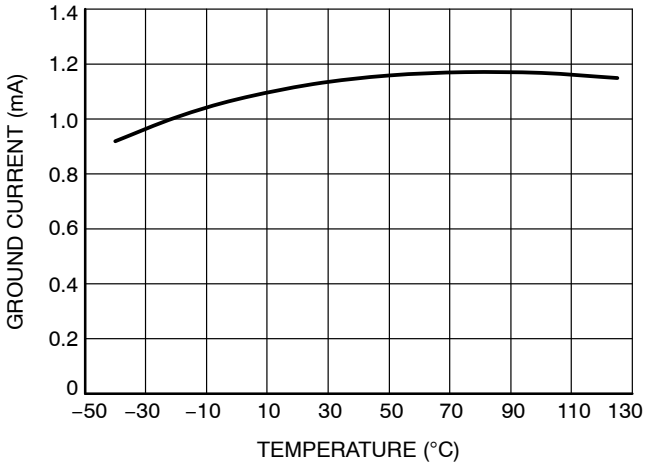



**Figure 12. Ground Current vs. Temperature ($V_{OUTnom}$ = 2.5 V, $I_{OUT}$ = 10 mA, $V_{IN}$ = 3.5 V)**

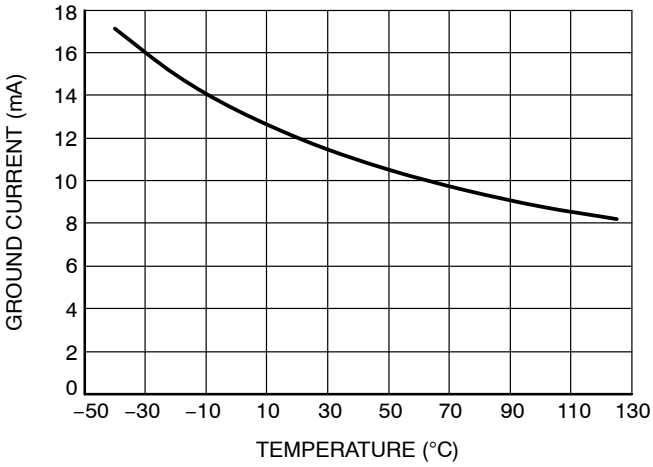



**Figure 13. Ground Current vs. Temperature ($V_{OUTnom}$ = 2.5 V, $I_{OUT}$ = 0.75 A, $V_{IN}$ = 3.5 V)**

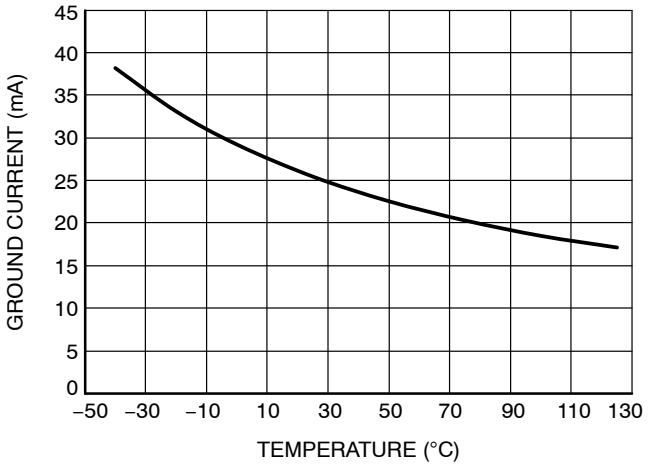



**Figure 14. Ground Current vs. Temperature ($V_{OUTnom}$ = 2.5 V, $I_{OUT}$ = 1.5 A, $V_{IN}$ = 3.5 V)**

## TYPICAL CHARACTERISTICS

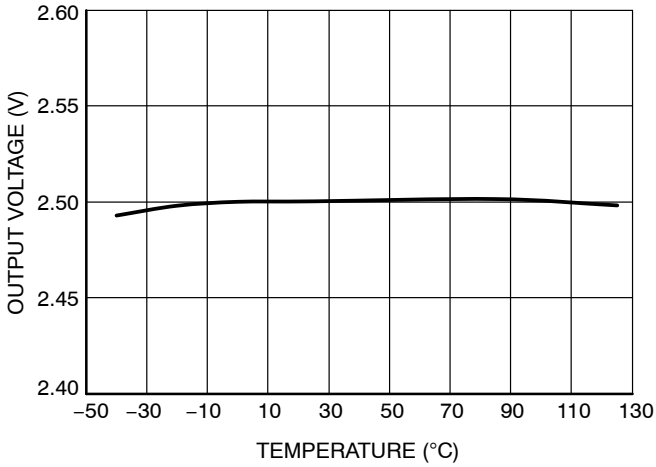



**Figure 15. Output Voltage vs. Temperature ($V_{OUTnom}$ = 2.5 V, $I_{OUT}$ = 10 mA)**

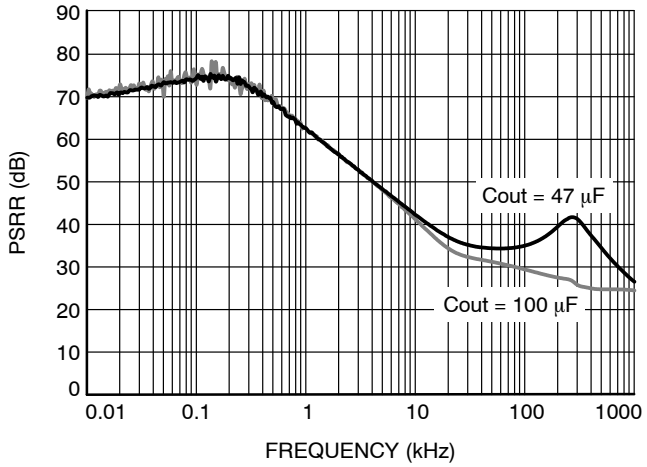



**Figure 16. PSRR vs. Frequency, Vin = 3.5 V + 200 mVpp Modulation, Vout = 2.5 V, Iout = 0.5 A**

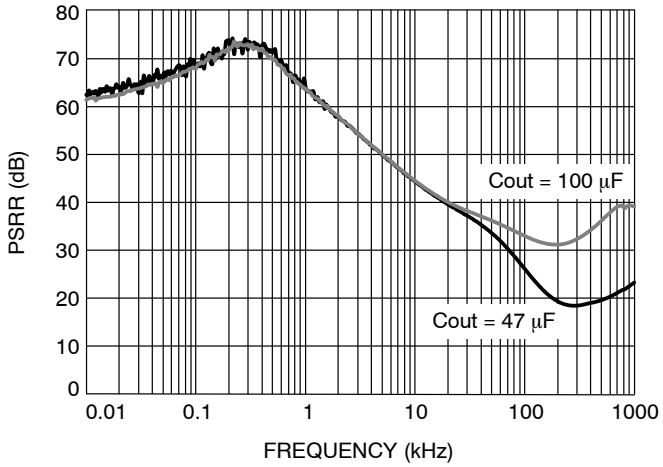



**Figure 17. PSRR vs. Frequency, Vin = 3.5 V + 200 mVpp Modulation, Vout = 2.5 V, Iout = 1.5 A**

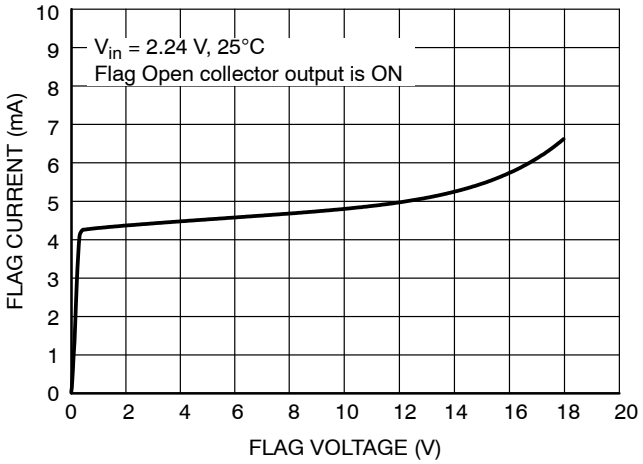



**Figure 18. Flag Current vs. Flag Voltage**

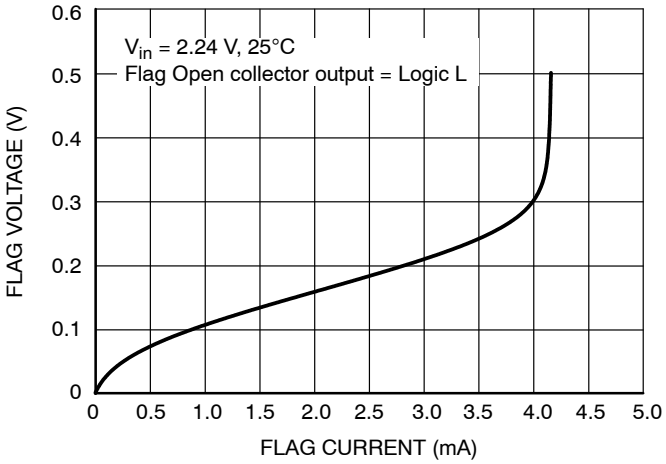



**Figure 19. Flag Voltage vs. Flag Current**

## TYPICAL CHARACTERISTICS

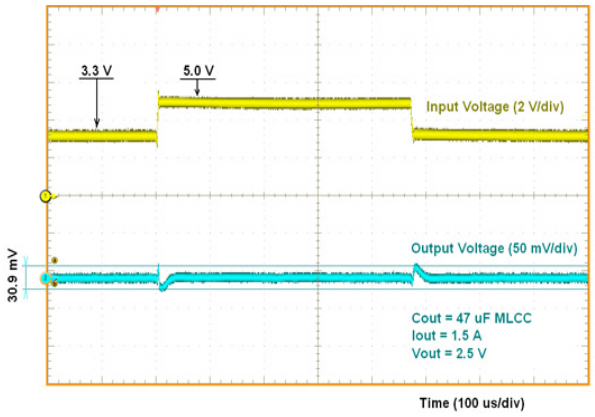



Figure 20. Line Transient Response

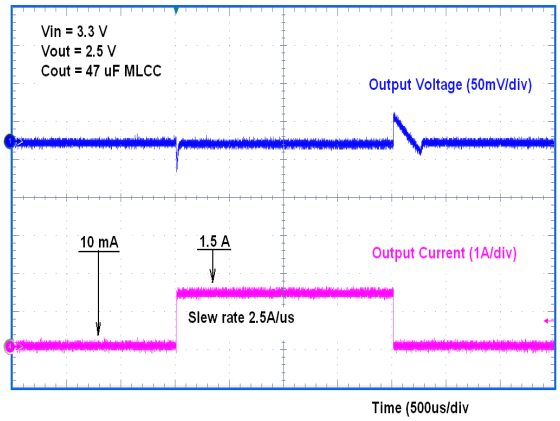



Figure 21. Load Transient Response

## APPLICATIONS INFORMATION

### Output Capacitor and Stability

The NCP57152 device requires an output capacitor for stable operation. The NCP57152 is designed to operate with ceramic output capacitors. The recommended output capacitance value is 47 μF or greater. Such capacitors help to improve transient response and noise reduction at high frequency.

### Input Capacitor

An input capacitor of 1.0 μF or greater is recommended when the device is more than 4 inches away from the bulk supply capacitance, or when the supply is a battery. Small, surface−mount chip capacitors can be used for the bypassing. The capacitor should be place within 1 inch of the device for optimal performance. Larger values will help to improve ripple rejection by bypassing the input of the regulator, further improving the integrity of the output voltage.

### Minimum Load Current

The NCP57152 regulator is specified between finite loads. A 5 mA minimum load current is necessary for proper operation.

### Enable Input

NCP57152 regulators also feature an enable input for on/off control of the device. It's shutdown state draws "zero" current from input voltage supply (only microamperes of leakage). The enable input is TTL/CMOS compatible for simple logic interface, but can be connected up to $V_{IN}$.

### Error Flag

NCP57152 devices in DFN package feature an error flag circuit that monitors the output voltage and signals an error condition when the voltage is 5% below the nominal output voltage. The error flag is an open−collector output that can sink up to 5 mA typically during a $V_{OUT}$ fault condition.

The FLG output is overload protected when a short circuit of the pullup load resistor occurs in the application. This is guaranteed in the full range of FLG output voltage Max ratings (see Max Ratings table). Please be aware operation in this mode is not recommended, power dissipated in the device can impact on output voltage precision and other device characteristics.

### Overcurrent and Reverse Output Current Protection

The NCP57152 regulator is fully protected from damage due to output current overload and output short conditions. When NCP57152 output is overloaded, Output Current limiting is provided. This limiting is linear; output current during overload or output short conditions is constant. These features are advantageous for powering FPGAs and other ICs having current consumption higher than nominal during their startup.

Thermal shutdown disables the NCP57152 device when the die temperature exceeds the maximum safe operating temperature.

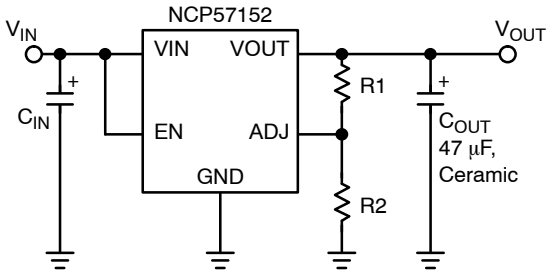
When NCP57152 is disabled and ($V_{OUT}$ – $V_{IN}$) voltage difference is less than 6.5 V in the application, the output structure of these regulators is able to withstand output voltage (backup battery as example) to be applied without reverse current flow. Of course the additional current flowing through the feedback resistor divider needs to be included in the backup battery discharging calculations.

### Adjustable Voltage Design

The NCP/NCV57152 Adjustable voltage Device Output voltage is set by the ratio of two external resistors as shown in Figure 22.

The device maintains the voltage at the ADJ pin at 1.24 V referenced to ground. The current in R2 is then equal to 1.24 V / R2, and the current in R1 is the current in R2 plus

the ADJ pin bias current. The ADJ pin bias current flows from $V_{OUT}$ through R1 into the ADJ pin.




$$V_{OUT} = 1.24\ V \cdot \left(1 + \frac{R1}{R2}\right) + I_{ADJ} \cdot R1$$

**Figure 22. Adjustable Voltage Operation**

For the R2 resistor value up to 15 kOhm the $I_{ADJ}$ current impact can be neglected and the R1 resistor value can be calculated by:

$$R1 = R2 \cdot \left((V_{OUT}/1.24) - 1\right) \qquad \text{(eq. 1)}$$

Where $V_{OUT}$ is the desired nominal output voltage.

### Thermal Considerations

The power handling capability of the device is limited by the maximum rated junction temperature (125°C). The $P_D$ total power dissipated by the device has two components, Input to output voltage differential multiplied by Output current and Input voltage multiplied by GND pin current.

$$P_D = \left(V_{IN} - V_{OUT}\right) \cdot I_{OUT} + V_{IN} \cdot I_{GND} \qquad \text{(eq. 2)}$$

The GND pin current value can be found in Electrical Characteristics table and in Typical Characteristics graphs.

The Junction temperature $T_J$ is

$$T_J = T_A + P_D \cdot R_{\theta JA} \qquad \text{(eq. 3)}$$

where $T_A$ is ambient temperature and $R_{\theta JA}$ is the Junction to Ambient Thermal Resistance of the NCP/NCV57152 device mounted on the specific PCB.

To maximize efficiency of the application and minimize thermal power dissipation of the device it is convenient to use the Input to output voltage differential as low as possible.

The static typical dropout characteristics for various output voltage and output current can be found in the Typical Characteristics graphs.

## ORDERING INFORMATION

| Device | Output Current | Output Voltage | Junction Temp. Range | Package | Shipping† |
|---|---|---|---|---|---|
| NCP57152MNADJTYG | 1.5 A | ADJ | −40°C to +125°C | DFN8−4x4 (Pb−Free) | 4000 / Tape & Reel |
| NCV57152MNADJTYG* | 1.5 A | ADJ | −40°C to +125°C | DFN8−4x4 (Pb−Free) | 4000 / Tape & Reel |
| NCP57152DSADJR4G | 1.5 A | ADJ | −40°C to +125°C | D2PAK−5 (Pb−Free) | 800 / Tape & Reel |
| NCV57152DSADJR4G* | 1.5 A | ADJ | −40°C to +125°C | D2PAK−5 (Pb−Free) | 800 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

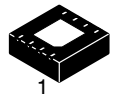
*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

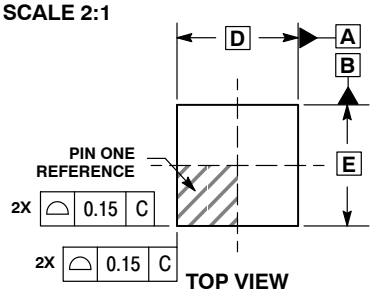
ON Semiconductor®

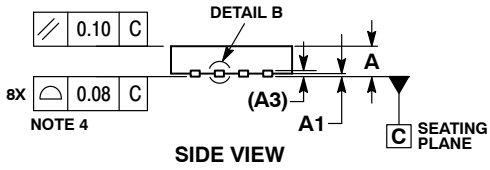
**DFN8, 4x4**
CASE 488AF−01
ISSUE C

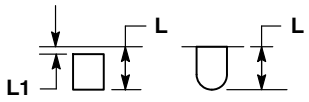
DATE 15 JAN 2009

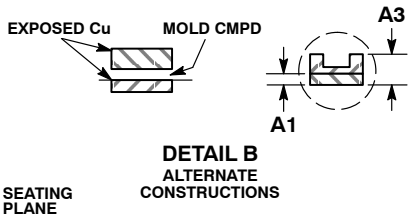


SCALE 2:1



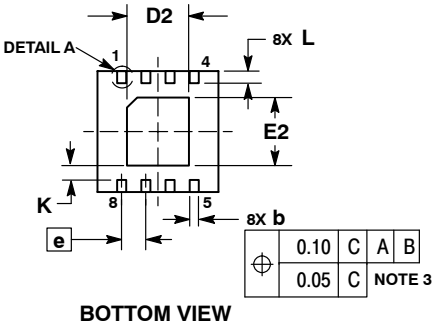



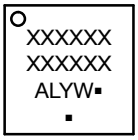




NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. DETAILS A AND B SHOW OPTIONAL CONSTRUCTIONS FOR TERMINALS.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | 0.00 | 0.05 |
| A3 | 0.20 REF | |
| b | 0.25 | 0.35 |
| D | 4.00 BSC | |
| D2 | 1.91 | 2.21 |
| E | 4.00 BSC | |
| E2 | 2.09 | 2.39 |
| e | 0.80 BSC | |
| K | 0.20 | --- |
| L | 0.30 | 0.50 |
| L1 | --- | 0.15 |




### GENERIC MARKING DIAGRAM*

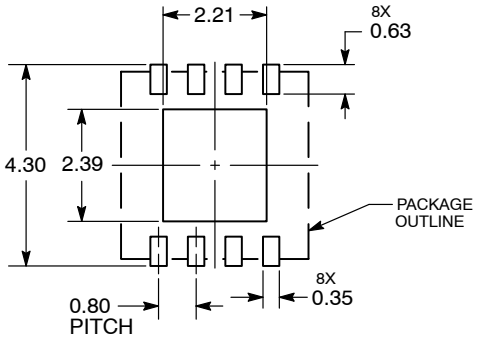



XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

### SOLDERING FOOTPRINT*




DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

| | | |
|---|---|---|
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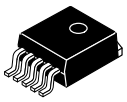
| DESCRIPTION: | DFN8, 4X4, 0.8P | PAGE 1 OF 1 |

# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

ON Semiconductor®

**D²PAK 5–LEAD**
CASE 936A–02
ISSUE E

DATE 28 JUL 2021



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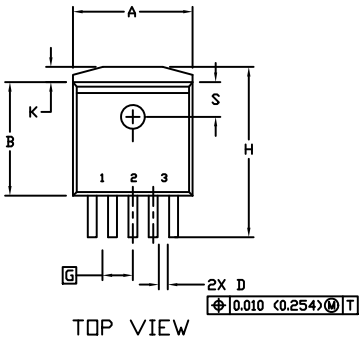
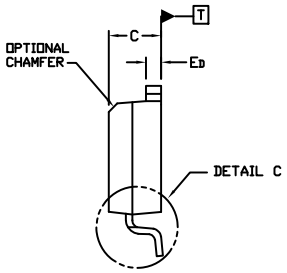
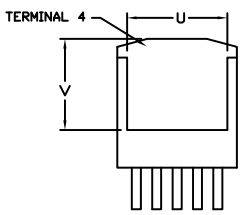


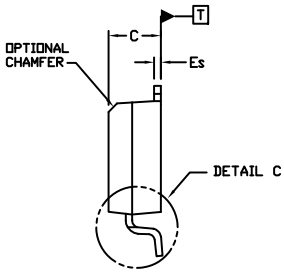

TOP VIEW



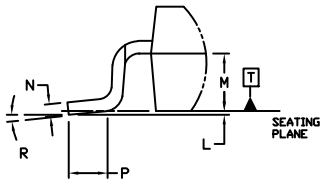

SIDE VIEW
DUAL GUAGE CONSTRUCTION



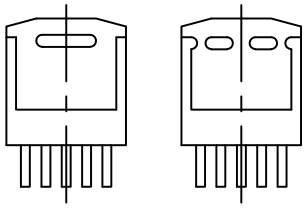

BOTTOM VIEW




SIDE VIEW
SINGLE GUAGE CONSTRUCTION




DETAIL C
TIP LEADFORM
ROTATED 90° CW

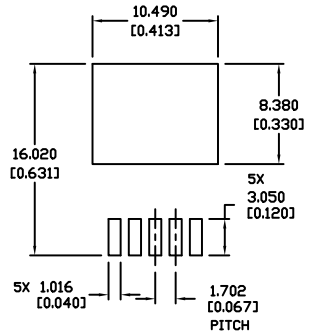


BOTTOM VIEW
OPTIONAL CONSTRUCTIONS

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCHES
3. TAB CONTOUR OPTIONAL WITHIN DIMENSIONS A AND K.
4. DIMENSIONS U AND V ESTABLISH A MINIMUM MOUNTING SURFACE FOR TERMINAL 4.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.025 (0.635) MAXIMUM.

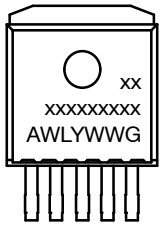
| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN. | MAX. | MIN. | MAX. |
| A | 0.396 | 0.403 | 9.804 | 10.236 |
| B | 0.356 | 0.368 | 9.042 | 9.347 |
| C | 0.170 | 0.180 | 4.318 | 4.572 |
| D | 0.026 | 0.036 | 0.660 | 0.914 |
| ED | 0.045 | 0.055 | 1.143 | 1.397 |
| ES | 0.018 | 0.026 | 0.457 | 0.660 |
| G | 0.067 BSC | | 1.702 BSC | |
| H | 0.539 | 0.579 | 13.691 | 14.707 |
| K | 0.050 REF | | 1.270 REF | |
| L | 0.000 | 0.010 | 0.000 | 0.254 |
| M | 0.088 | 0.102 | 2.235 | 2.591 |
| N | 0.018 | 0.026 | 0.457 | 0.660 |
| P | 0.058 | 0.078 | 1.473 | 1.981 |
| R | 0° | 8° | 0° | 8° |
| S | 0.116 REF | | 2.946 REF | |
| U | 0.200 MIN | | 5.080 MIN | |
| V | 0.250 MIN | | 6.350 MIN | |




RECOMMENDED
MOUNTING FOOTPRINT *

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### GENERIC MARKING DIAGRAM*




| | |
|---|---|
| XXXXXX | = Device Code |
| A | = Assembly Location |
| WL | = Wafer Lot |
| Y | = Year |
| WW | = Work Week |
| G | = Pb–Free Package |

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

| | | |
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