

SANYO Semiconductors

DATA SHEET

LA5692D, 5692S LA5692M

Monolithic Linear IC With Watchdog Timer Voltage Regulator Driver

Overview

The LA5692 is a single-chip voltage regulator for microcomputer system monitor use that performs the functions of 5V output voltage control, watchdog timer, and voltage detector. Since the LA5692 can hold the reset output, it is especially suited for use in peripheral control and monitor output applications (example : valves used in refrigeration equipment, hot water supply system).

Applications

• Microcomputer system for car equipment, refrigeration/heating equipment, office automation equipment.

Features

- An external PNP transistor can be used to provide a low saturation voltage regulator.
- CK input with edge detector.
- Variable detection voltage.
- The watchdog time can be made longer.

Functions

- Output voltage 5V control.
- Watchdog timer.
- Reset generation at power-ON mode.
- Reset hold output [RES (2)] (Cleared with CK re-input).
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Specifications

Maximum Ratings at $Ta = 25^{\circ}C$

Parameter	Symbol	Conditions	Ratings	Unit
Control pin voltage	VCONT max	1s	60	V
Control pin voltage	VCONT max		41	V
Control pin current	ICONT max	$V_{CC} \ge 6V *$	11	mA
CK input voltage	V _{CK} max		25	V
Reset pin voltage	V _{RES} (1) max, V _{RES} (2) max		41	V
Allowable power dissipation	Pd max	LA 5692D, 5692S	500	mW
		LA5692M	370	mW
Operating temperature	Topr		-40 to +85	°C
Storage temperature	Tstg		-55 to +150	°C

* : A PNP transistor is connected to the LA5692D, 5692S externally to provide a low-saturation voltage regulator.

Therefore, $I_{CONT} \approx 100$ mA will flow, as starting current, in the V_{CC} range where the output cannot be regulated.

Operating Conditions at $Ta = 25^{\circ}C$

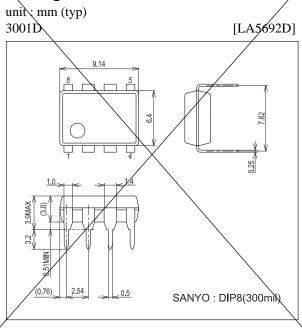
Parameter	Symbol	Conditions	Ratings	Unit
Control pin voltage	VCONT		6 to 40	V
Control pin current	ICONT max		10	mA
Reset output current	I <mark>RES</mark> (1) max, I <u>RES</u> (2) max	External R pull-up	8	mA
Reset detection voltage	V _S min		4	V

Electrical Characteristics at $Ta = 25^{\circ}C$, $V_{CC} = 14V$, $I_{O} = 50mA$, unless otherwise specified.

Parameter	Symbol	Conditions		Ratings		
			min	typ	max	Unit
Output voltage	VO		4.8	5.0	5.2	V
Line regulation1	∆V _{OLN} 1	$9V \le V_{CC} \le 16V$		2	10	mV
Line regulation2	ΔV _{OLN} 2	$6V \le V_{CC} \le 40V$		4	30	mV
Load regulation	ΔV _{OLD}	$1\text{mA} \le I_{O} \le 50\text{mA}$		4	30	mV
Current dissipation	ICC	IO = 0		4.4	6.5	mA
Output noise voltage	V _{NO}	$10Hz \le f \le 100kHz, V_{CK} = 0$		150		μV
Temperature coefficient of output voltage	∆V _O /∆Ta	$I_{O} = 5mA, -40^{\circ}C \le Ta \le +85^{\circ}C$		±0.2		mV/°C
Reference voltage	V _{REF}		1.13	1.18	1.23	V
'H'-level CK input voltage	VIH		2			V
'L'-level CK input voltage	VIL				0.8	V
'H'-level CK input current	Чн	V _{CK} = 5V		0.3	0.7	mA
'L'-level CK input current	Ι _{ΙL}	V _{CK} = 0V	-1.0	-0.1		μΑ
'H'-level reset output voltage	V _{ORH} (1) V _{ORH} (2)	$\overline{\text{RES}}$ (2) : 10K Ω pull-up	4.8	5.0	5.2	V
'L'-level reset output voltage1	V _{ORL} (1) 1 V _{ORL} (2) 1	$\overline{\text{RES}}$ (2) : 10K Ω pull-up		40	200	mV
'L'-level reset output voltage2	V _{ORL} (1) 2 V _{ORL} (2) 2	$I_{\overline{\text{RES}}}(1) = I_{\overline{\text{RES}}}(2) = 8\text{mA}$		0.16	0.8	V
CK input pulse width	^t CKW	V _{CK} = 5V	3			μs
Reset output delay time	td	C _t = 1µF	7.5	10	12.5	ms
Watchdog time	tWD	C _t = 1µF	30	40	50	ms
Watchdog reset time	^t WR	C _t = 1µF	0.1	0.25	0.4	ms
Reset hysteresis voltage	V _{hys}	V _S = 4.5V	100	200	300	mV

Discontinued

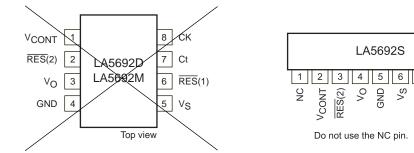
Rackage Dimensions



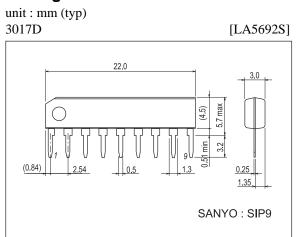
Rackage Dimensions

unit : mm (typ) 3032D [LA5692M] 8 4 63 Ħ H 1 (0.65) 1.27 _0.35 0.1 .7max (1.5) 0.1 SANYO : MFP8(225mil)

Pin Assignment



Package Dimensions



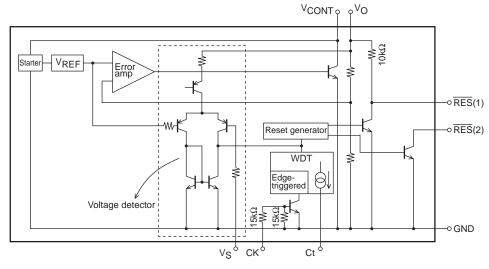
7 8 9 Top view

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<u>RES(1)</u>

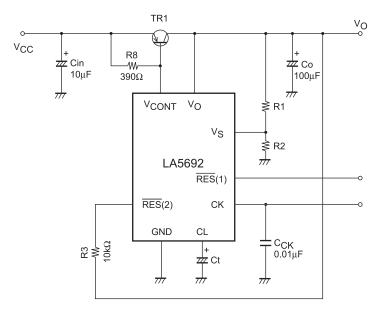
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Block Diagram

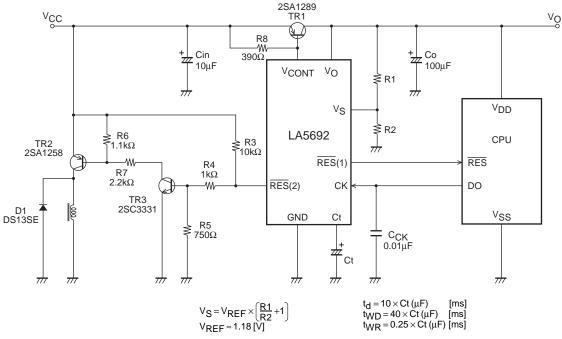


* $\overline{RES}(1)$: Contains a pull-up resistor of 10k Ω . $\overline{RES}(2)$: Open collector

Test Circuit



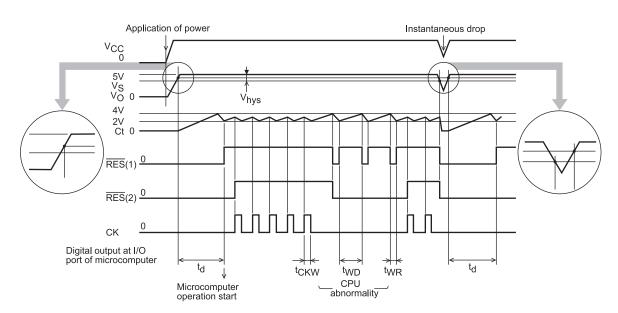
Sample Application Circuit



Note on application

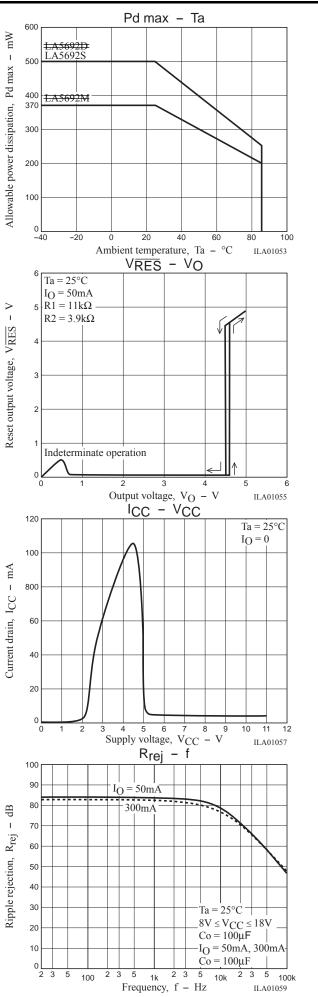
- 1. For stable operation, place Cin, CO, and TR1 as near to the IC as possible.
- 2. When used in 0°C or below it, a capacitor of which impedance at high-frequency operation is low and has a good temperature characteristic (such as SANYO OS-CON capacitor or others) should be used to prevent oscillation.
- 3. Set V_S to the output voltage level where the circuit will be reset using external resistors R1 and R2. V_S should be set to 4V or greater due to internal circuit operation.
- 4. C_{CK} must be inserted to cut the high range element of clock noise to prevent it from becoming a reset output noise.
- 5. For Ct, a capacitor which less varies the capacitance according to the temperature should be used.

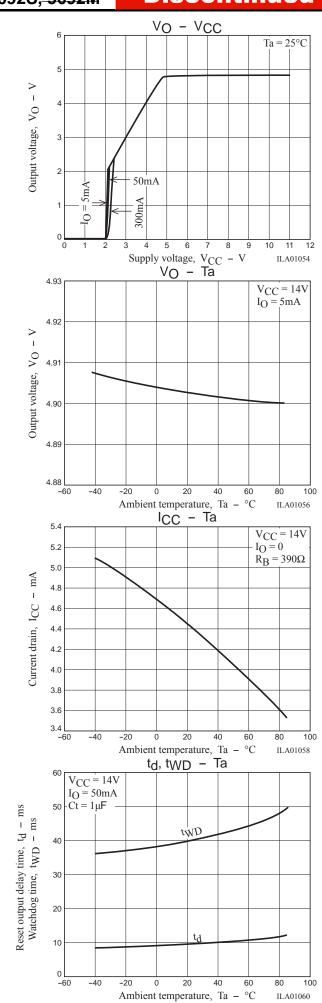
Timing Chart

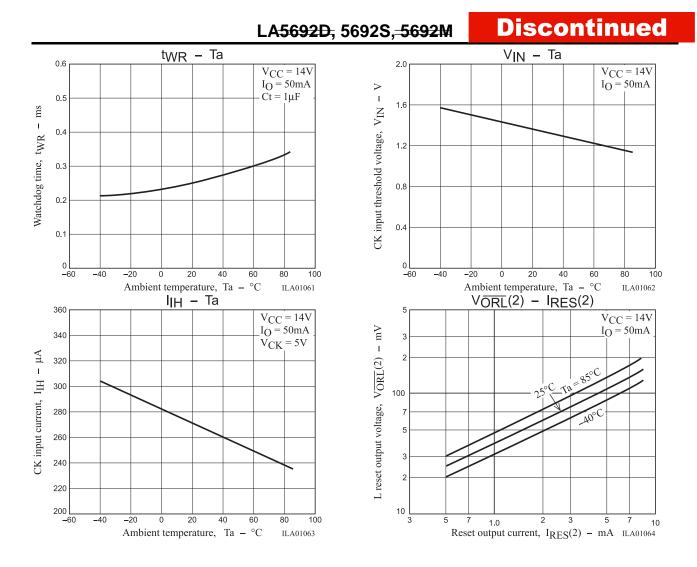


Note : Edge-triggered at the point indicated by the arrow of C_K signal.

LA5692D, 5692S, 5692M







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