NCV8664

[Linear Regulator](#) - Low Dropout, Very Low I_q

The NCV8664 is a precision 3.3 V and 5.0 V fixed output, low dropout integrated voltage regulator with an output current capability of 150 mA. Careful management of light load current consumption, combined with a low leakage process, achieve a typical quiescent current of 22 μA.

NCV8664 is pin and functionally compatible with NCV4264 and NCV4264−2, and it could replace these parts when very low quiescent current is required.

The output voltage is accurate within ±2.0%, and maximum dropout voltage is 600 mV at full rated load current.

It is internally protected against input supply reversal, output overcurrent faults, and excess die temperature. No external components are required to enable these features.

Features

- 3.3 V, 5.0 V Fixed Output
- ±2.0% Output Accuracy, Over Full Temperature Range
- 30 μA Maximum Quiescent Current at I_{OUT} = 100 μA
- 600 mV Maximum Dropout Voltage at 150 mA Load Current
- Wide Input Voltage Operating Range of 4.5 V to 45 V
- Internal Fault Protection
  - −42 V Reverse Voltage
  - Short Circuit/Overcurrent
  - Thermal Overload
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
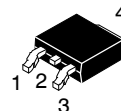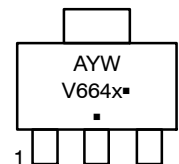- EMC Compliant
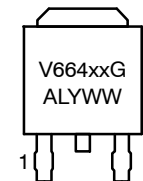- These are Pb−Free Devices

ON Semiconductor®

www.onsemi.com

MARKING DIAGRAMS
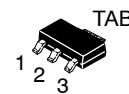
TAB — SOT−223 ST SUFFIX CASE 318E

AYW
V664x▪
▪

DPAK DT SUFFIX CASE 369C

V664xxG
ALYWW

SOIC−8 Fused CASE 751

V664x
ALYWX
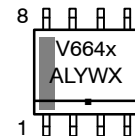
xx	= Voltage Rating DPAK
	(50 = 5.0 V Version)
	(33 = 3.3 V Version)
x	= Voltage Rating SOT223
	(5 = 5.0 V Version)
	(3 = 3.3 V Version)
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W, WW	= Work Week
▪ or G	= Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS

(SOT−223/DPAK)		(SOIC−8 Fused)	
PIN	FUNCTION	PIN	FUNCTION
1	V_{IN}	1	NC
2,TAB	GND	2,	V_{IN}
3	V_{OUT}	3	GND
		4.	V_{OUT}
		5−8.	NC

ORDERING INFORMATION

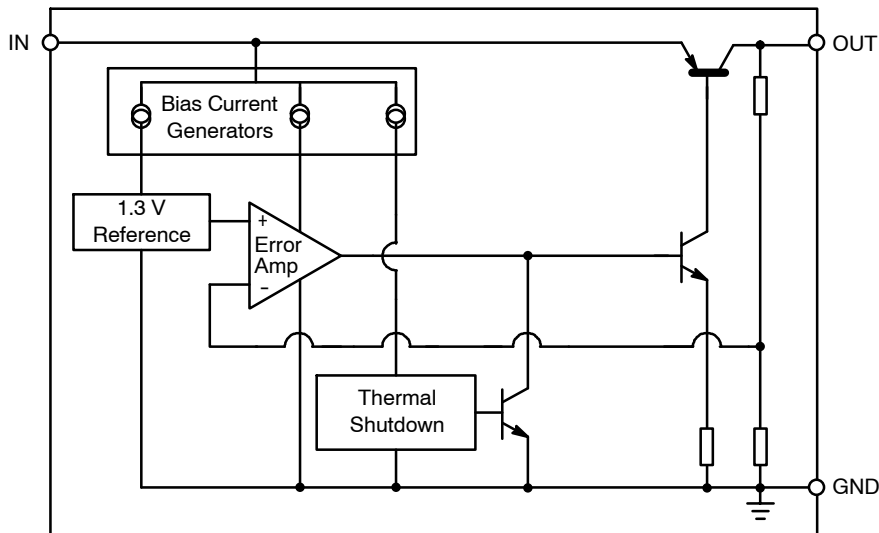See detailed ordering and shipping information in the package dimensions section on page 11 of this data sheet.

Publication Order Number:
NCV8664/D

NCV8664

Figure 1. Block Diagram

PIN FUNCTION DESCRIPTION

Pin No.			
DPAK/SOT−223	**SOIC−8**	**Symbol**	**Function**
1	2	V_{IN}	Unregulated input voltage; 4.5 V to 45 V.
2	3	GND	Ground; substrate.
3	4	V_{OUT}	Regulated output voltage; collector of the internal PNP pass transistor.
TAB	−	GND	Ground; substrate and best thermal connection to the die.
−	1, 5−8	NC	No Connection.

OPERATING RANGE

Pin Symbol, Parameter	Symbol	Min	Max	Unit
V_{IN}, DC Input Operating Voltage	V_{IN}	4.5	+45	V
Junction Temperature Operating Range	T_J	−40	+150	°C

MAXIMUM RATINGS

Rating	Symbol	Min	Max	Unit
V_{IN}, DC Voltage	V_{IN}	−42	+45	V
V_{OUT}, DC Voltage	V_{OUT}	−0.3	+18	V
Storage Temperature	T_{stg}	−55	+150	°C
ESD Capability, Human Body Model (Note 1)	V_{ESDHB}	4000	−	V
ESD Capability, Machine Model (Note 1)	V_{ESDMIM}	200	−	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. This device series incorporates ESD protection and is tested by the following methods:
    ESD HBM tested per AEC−Q100−002 (EIA/JESD22−A 114C)
    ESD MM tested per AEC−Q100−003 (EIA/JESD22−A 115C)

THERMAL RESISTANCE

Parameter		Symbol	Condition	Min	Max	Unit
Junction−to−Ambient	DPAK SOT−223 SOIC−8 Fused	$R_{\theta JA}$		− − −	101 (Note 2) 99 (Note 2) 145	°C/W
Junction−to−Case	DPAK SOT−223 SOIC−8 Fused	$R_{\theta JC}$		− − −	9.0 17 −	°C/W

2. 1 oz., 100 mm^2 copper area.

NCV8664

LEAD SOLDERING TEMPERATURE AND MSL

Rating	Symbol	Min	Max	Unit
Lead Temperature Soldering Reflow (SMD Styles Only), Lead Free (Note 3)	T_{sld}	–	265 pk	°C
Moisture Sensitivity Level SOT223 DPAK SOIC−8 Fused	MSL	3 2 1	– – –	–

3. Lead Free, 60 sec − 150 sec above 217°C, 40 sec max at peak.

ELECTRICAL CHARACTERISTICS (V_{IN} = 13.5 V, Tj = −40°C to +150°C, unless otherwise noted.)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage 5.0 V Version	V_{OUT}	0.1 mA ≤ I_{OUT} ≤ 150 mA (Note 4) 6.0 V ≤ V_{IN} ≤ 28 V	4.900	5.000	5.100	V
Output Voltage 5.0 V Version	V_{OUT}	0 mA ≤ I_{OUT} ≤ 150 mA 5.5 V ≤ V_{IN} ≤ 28 V −40°C ≤ T_J ≤ 125°C	4.900	5.000	5.100	V
Output Voltage 3.3 V Version	V_{OUT}	0.1 mA ≤ I_{OUT} ≤ 150 mA (Note 4) 4.5 V ≤ V_{IN} ≤ 28 V	3.234	3.300	3.366	V
Line Regulation 5.0 V Version	ΔV_{OUT} vs. V_{IN}	I_{OUT} = 5.0 mA 6.0 V ≤ V_{IN} ≤ 28 V	−25	5.0	+25	mV
Line Regulation 3.3 V Version	ΔV_{OUT} vs. V_{IN}	I_{OUT} = 5.0 mA 4.5 V ≤ V_{IN} ≤ 28 V	−25	5.0	+25	mV
Load Regulation	ΔV_{OUT} vs. I_{OUT}	1.0 mA ≤ I_{OUT} ≤ 150 mA (Note 4)	−35	5.0	+35	mV
Dropout Voltage 5.0 V Version	V_{IN}–V_{OUT}	I_Q = 100 mA (Notes 4 & 5) I_Q = 150 mA (Notes 4 & 5)	– –	265 315	500 600	mV
Dropout Voltage 3.3 V Version	V_{IN}–V_{OUT}	I_Q = 100 mA (Notes 4 & 7) I_Q = 150 mA (Notes 4 & 7)	– –	– –	1.266 1.266	V
Quiescent Current	I_q	I_{OUT} = 100 μA T_J = 25°C T_J = −40°C to +85°C	– –	21 22	29 30	μA
Active Ground Current	$I_{G(ON)}$	I_{OUT} = 50 mA (Note 4) I_{OUT} = 150 mA (Note 4)	– –	1.3 8.0	3 15	mA
Power Supply Rejection	PSRR	V_{RIPPLE} = 0.5 $V_{P–P}$, F = 100 Hz	–	67	–	dB
Output Capacitor for Stability 5.0 V Version	C_{OUT} ESR	I_{OUT} = 0.1 mA to 150 mA (Note 4)	10 –	– –	– 9.0	μF Ω
Output Capacitor for Stability 3.3 V Version	C_{OUT} ESR	I_{OUT} = 0.1 mA to 150 mA (Note 4)	22 –	– –	– 18	μF Ω

PROTECTION

	Symbol	Test Conditions	Min	Typ	Max	Unit
Current Limit	$I_{OUT(LIM)}$	V_{OUT} = 4.5 V (5.0 V Version) (Note 4) V_{OUT} = 3.0 V (3.3 V Version) (Note 4)	150 150	– –	500 500	mA
Short Circuit Current Limit	$I_{OUT(SC)}$	V_{OUT} = 0 V (Note 4)	100	–	500	mA
Thermal Shutdown Threshold	T_{TSD}	(Note 6)	150	–	200	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
4. Use pulse loading to limit power dissipation.
5. Dropout voltage = (V_{IN} − V_{OUT}), measured when the output voltage has dropped 100 mV relative to the nominal value obtained with V_{IN} = 13.5 V.
6. Not tested in production. Limits are guaranteed by design.
7. V_{DO} = V_{IN} − V_{OUT}. For output voltage set to < 4.5 V, V_{DO} will be constrained by the minimum input voltage.
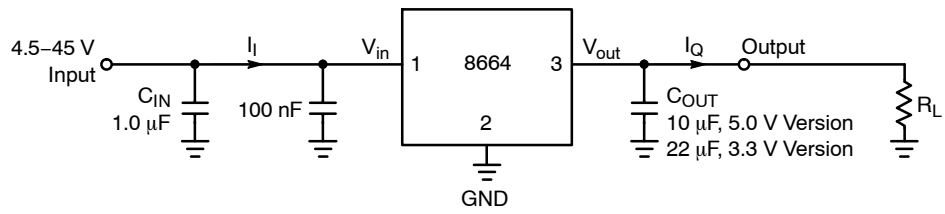
NCV8664

Figure 2. Measurement Circuit

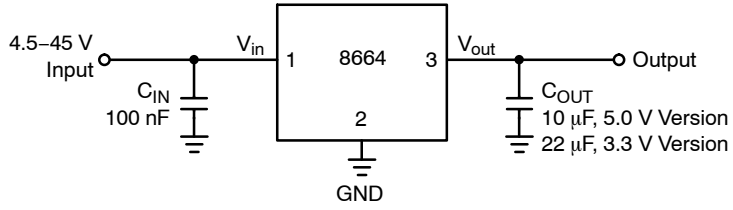

Figure 3. Applications Circuit

NCV8664

Typical Curves

Figure 4. ESR Characterization, 5.0 V Version

Figure 5. Output Voltage vs. Input Voltage,
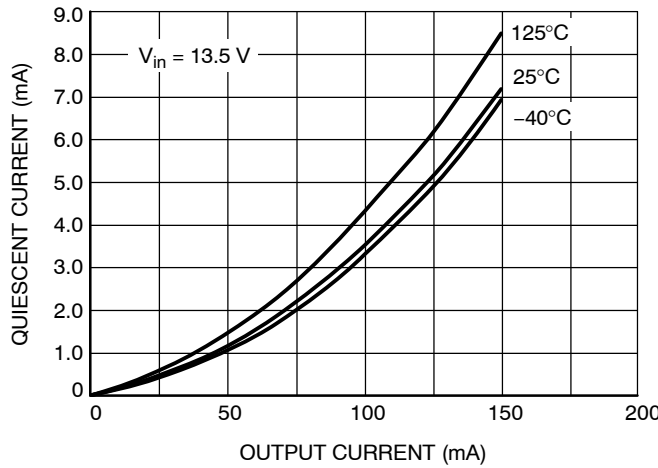5.0 V Version

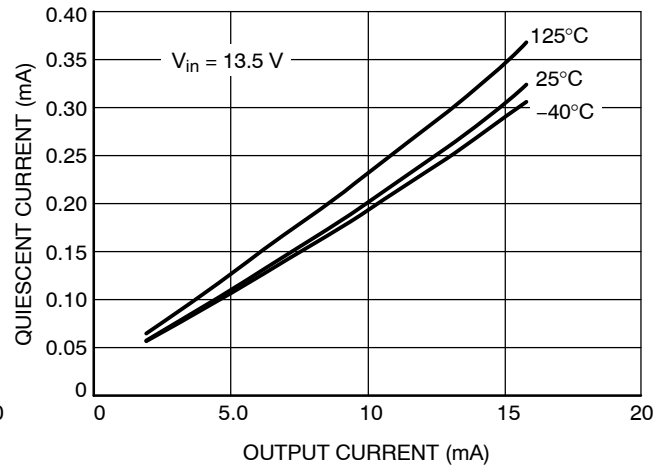Figure 6. Current Consumption vs. Output
Load, 5.0 V Version

Figure 7. Current Consumption vs. Output
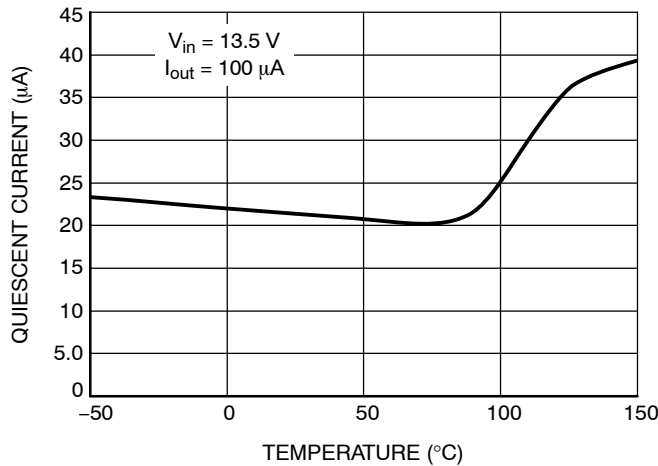Load (Low Load), 5.0 V Version

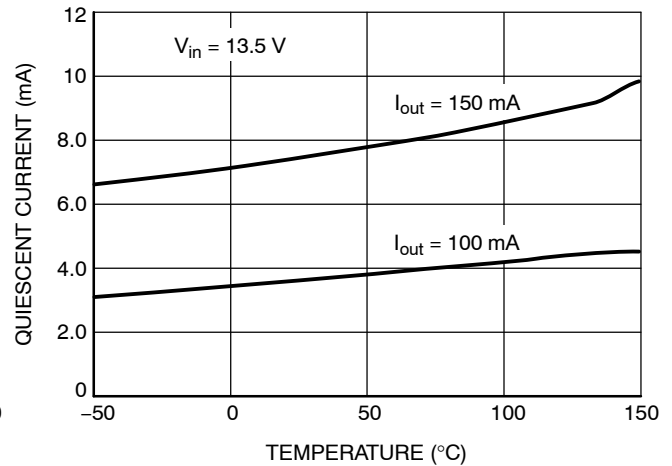Figure 8. Quiescent Current vs. Temperature,
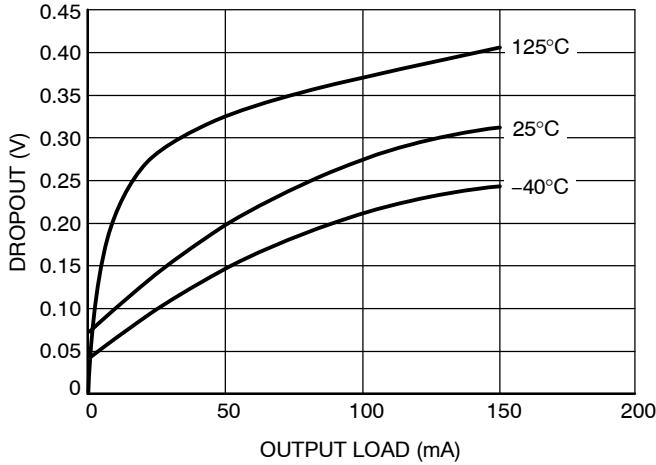5.0 V Version

Figure 9. Quiescent Current vs. Temperature,
5.0 V Version

Typical Curves
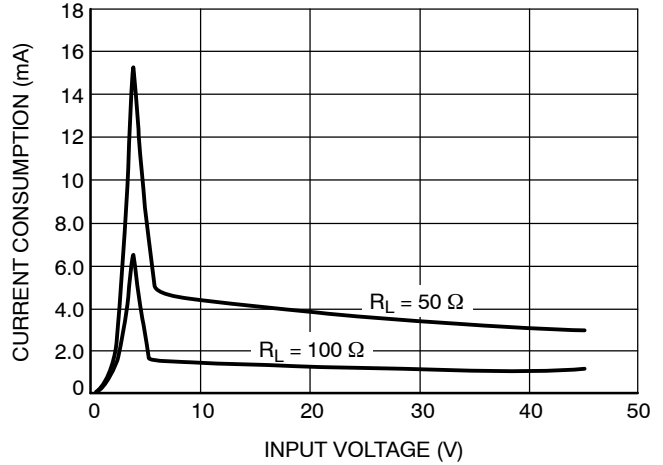
Figure 10. Dropout Voltage vs. Output Load, 5.0 V Version

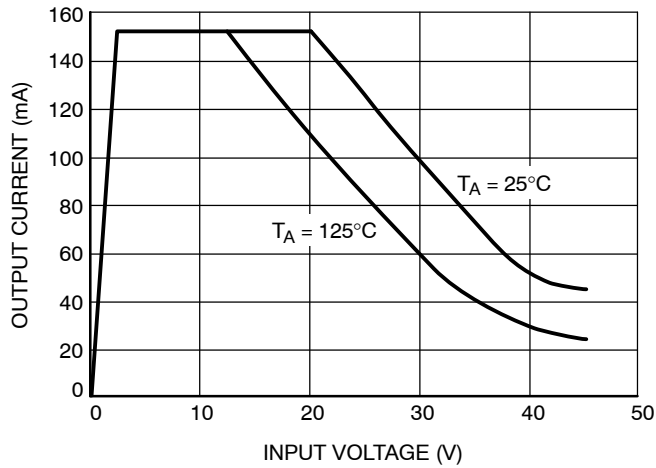**Figure 11. Current Consumption vs. Input Voltage, 5.0 V Version**

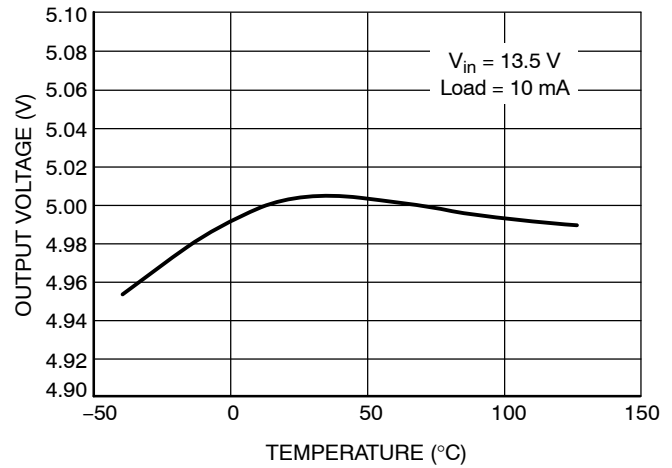**Figure 12. Output Current vs. Input Voltage, 5.0 V Version**

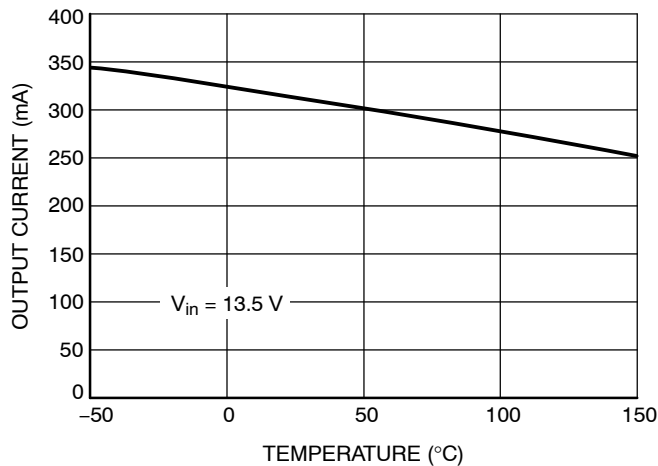**Figure 13. Output Voltage vs. Temperature, 5.0 V Version**

Figure 14. Current Limit vs. Temperature, 5.0 V Version

Typical Curves

Figure 15. ESR Stability, 3.3 V Version

Figure 16. Output Voltage vs. Input Voltage, 3.3 V Version
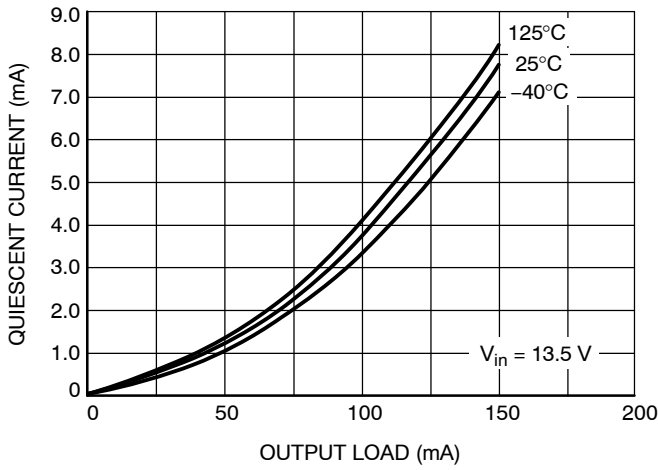

Figure 17. Current Consumption vs. Output Load, 3.3 V Version
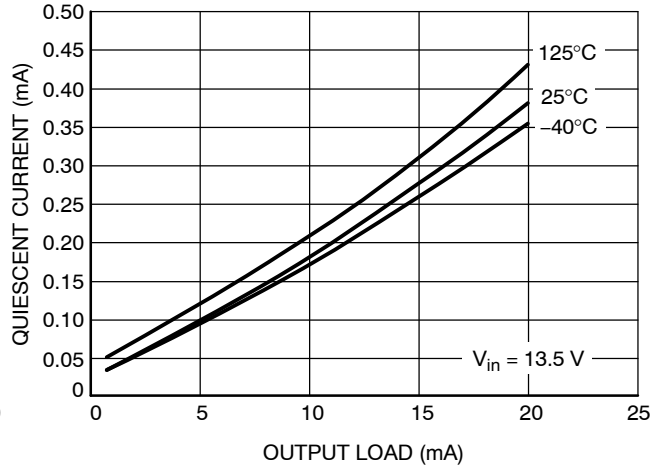

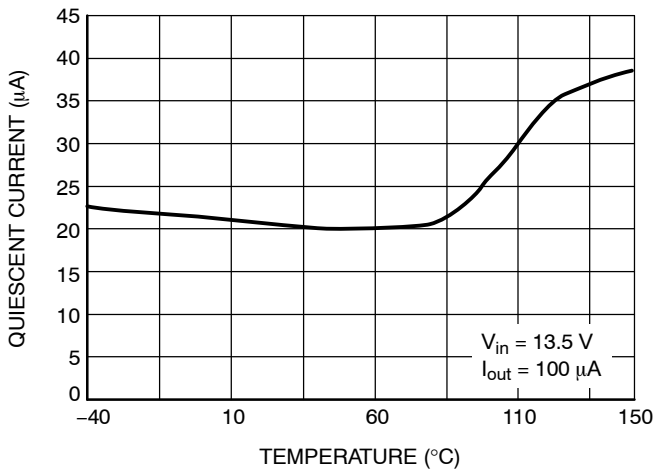**Figure 18. Current Consumption vs. Output Load (Low Load), 3.3 V Version**

Figure 19. Quiescent Current vs. Temperature, 3.3 V Version
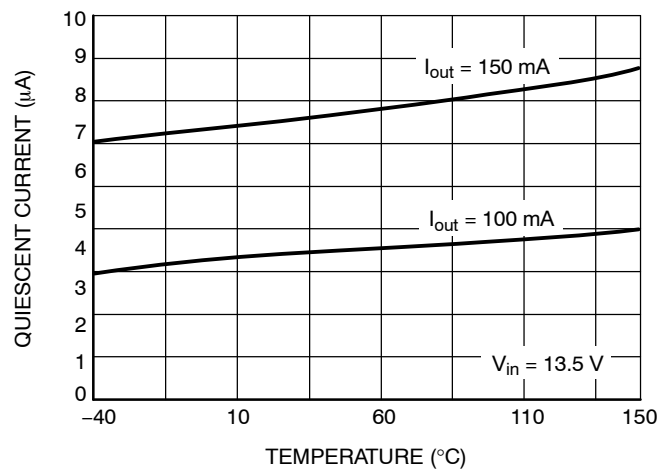

Figure 20. Quiescent Current vs. Temperature, 3.3 V Version
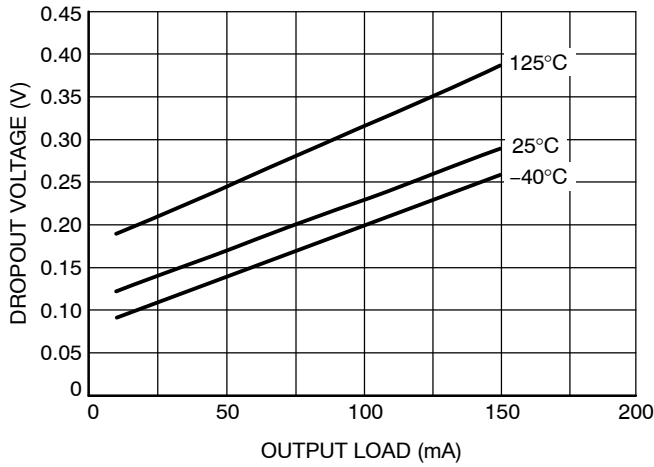
Typical Curves
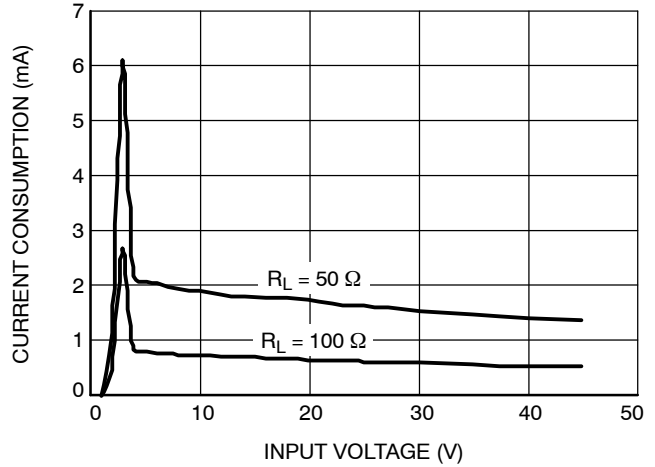

Figure 21. Dropout Voltage, 3.3 V Version

Figure 22. Current Consumption vs. Input Voltage, 3.3 V Version
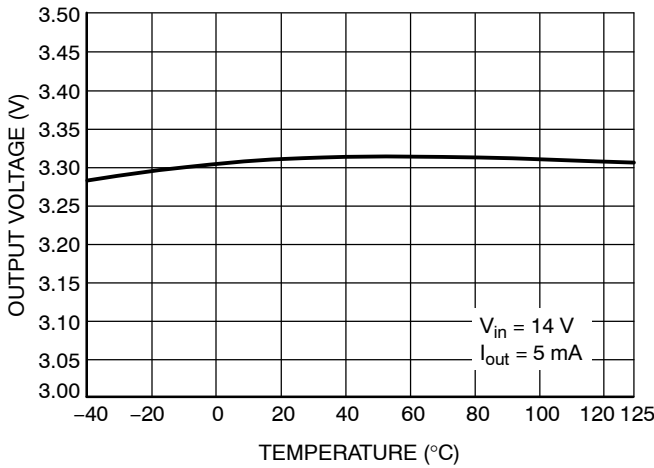

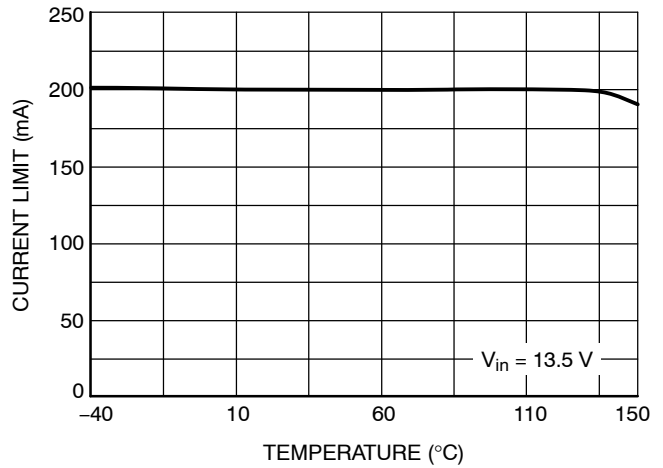Figure 23. Output Voltage vs. Temperature, 3.3 V Version

Figure 24. Short Circuit Current Limit vs. Temperature, 3.3 V Version

Circuit Description

The NCV8664 is a precision trimmed 3.3 V and 5.0 V fixed output regulator. Careful management of light load consumption combined with a low leakage process results in a typical quiescent current of 22 μA. The device has current capability of 150 mA, with 600 mV of dropout voltage at full rated load current. The regulation is provided by a PNP pass transistor controlled by an error amplifier with a bandgap reference. The regulator is protected by both current limit and short circuit protection. Thermal shutdown occurs above 150°C to protect the IC during overloads and extreme ambient temperatures.

Regulator

The error amplifier compares the reference voltage to a sample of the output voltage (V_{out}) and drives the base of a PNP series pass transistor by a buffer. The reference is a bandgap design to give it a temperature−stable output. Saturation control of the PNP is a function of the load current and input voltage. Over saturation of the output power device is prevented, and quiescent current in the ground pin is minimized. The NCV8664 is equipped with foldback current protection. This protection is designed to reduce the current limit during an overcurrent situation.

Regulator Stability Considerations

The input capacitor C_{IN} in Figure 2 is necessary for compensating input line reactance. Possible oscillations caused by input inductance and input capacitance can be damped by using a resistor of approximately 1 Ω in series with C_{IN}. The output or compensation capacitor, C_{OUT} helps determine three main characteristics of a linear regulator: startup delay, load transient response and loop stability. The capacitor value and type should be based on cost, availability, size and temperature constraints. Tantalum, aluminum electrolytic, film, or ceramic capacitors are all acceptable solutions, however, attention must be paid to ESR constraints. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures (−25°C to −40°C), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturer's data sheet usually provides this information. The value for the output capacitor C_{OUT} shown in Figure 2 should work for most applications; however, it is not necessarily the optimized solution. Stability is guaranteed at values $C_{OUT} \geq 10\,\mu F$ and ESR $\leq 9\,\Omega$ for 5.0 V version, and $C_{OUT} \geq 22\,\mu F$ and ESR $\leq 18\,\Omega$ for 3.3 V version, within the operating temperature range. Actual limits are shown in a graph in the Typical Performance Characteristics section.

Calculating Power Dissipation in a Single Output Linear Regulator

The maximum power dissipation for a single output regulator (Figure 3) is:

$$P_{D(max)} = [V_{IN(max)} - V_{OUT(min)}] \cdot I_{Q(max)} + V_{I(max)} \cdot I_q \quad \text{(eq. 1)}$$

Where:
$V_{IN(max)}$ is the maximum input voltage,
$V_{OUT(min)}$ is the minimum output voltage,
$I_{Q(max)}$ is the maximum output current for the application, and I_q is the quiescent current the regulator consumes at $I_{Q(max)}$.

Once the value of $P_{D(Max)}$ is known, the maximum permissible value of $R_{\theta JA}$ can be calculated:

$$P_{\theta JA} = \frac{150°C - T_A}{P_D} \quad \text{(eq. 2)}$$

The value of $R_{\theta JA}$ can then be compared with those in the package section of the data sheet. Those packages with $R_{\theta JA}$'s less than the calculated value in Equation 2 will keep the die temperature below 150°C. In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heat sink will be required. The current flow and voltages are shown in the Measurement Circuit Diagram.

Heat Sinks

For proper heat sinking of the SOIC−8 Lead device, connect pins 5 − 8 to the heat sink.

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air. Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\theta JA}$:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA} \quad \text{(eq. 3)}$$

Where:
$R_{\theta JC}$ = the junction−to−case thermal resistance,
$R_{\theta CS}$ = the case−to−heat sink thermal resistance, and
$R_{\theta SA}$ = the heat sink−to−ambient thermal resistance.
$R_{\theta JA}$ appears in the package section of the data sheet.

Like $R_{\theta JA}$, it too is a function of package type. $R_{\theta CS}$ and $R_{\theta SA}$ are functions of the package type, heat sink and the interface between them. These values appear in data sheets of heat sink manufacturers. Thermal, mounting, and heat sinking are discussed in the ON Semiconductor application note AN1040/D, available on the ON Semiconductor Website.

Downloaded from Arrow.com.

EMC−Characteristics: Conducted Susceptibility

All EMC−Characteristics are based on limited samples and not part of production testing, according to 47A/658/CD IEC62132−4 (Direct Power Injection)

Direct Power Injection: 33 dBm forward power CW
Acceptance Criteria: Amplitude Dev. max 2% of Output Voltage

Test Conditions

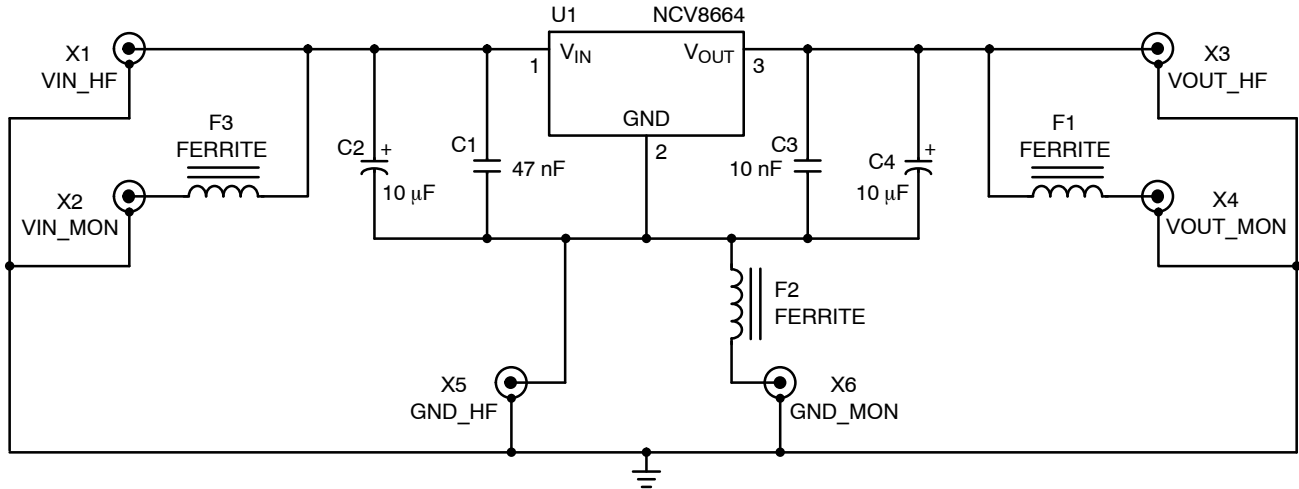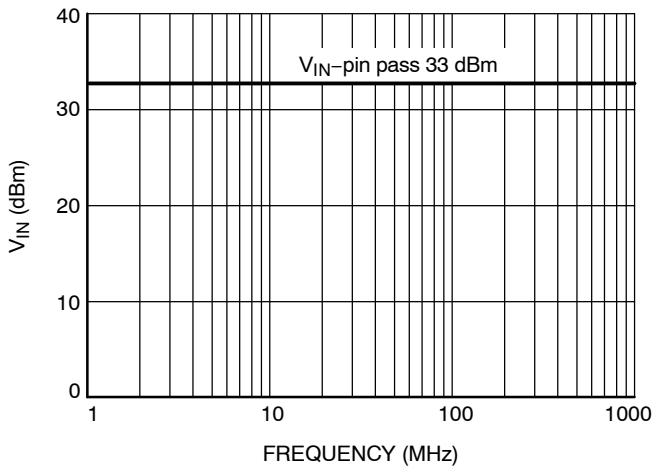|	
Supply Voltage	V_{IN} = 12 V
Temperature	T_A = 23°C ±5°C
Load	R_L = 35 Ω

Figure 25. Test Circuit
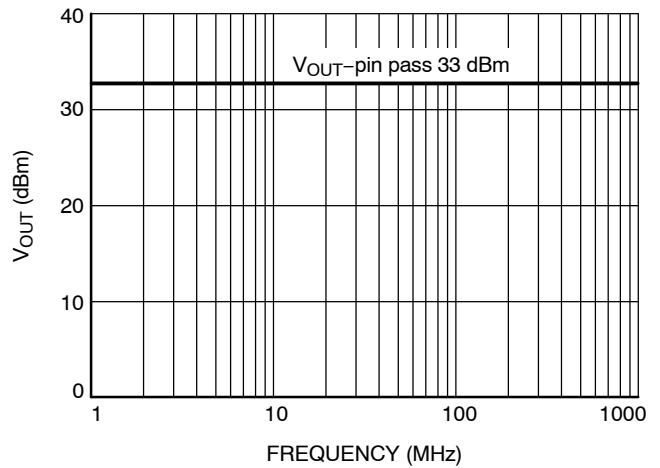
Figure 26. Typical V_{IN}−pin Susceptibility

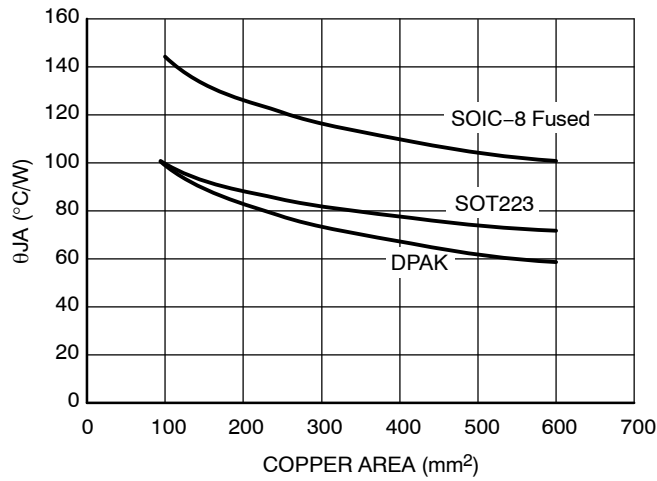**Figure 27. Typical V_{OUT}−pin Susceptibility**

NCV8664

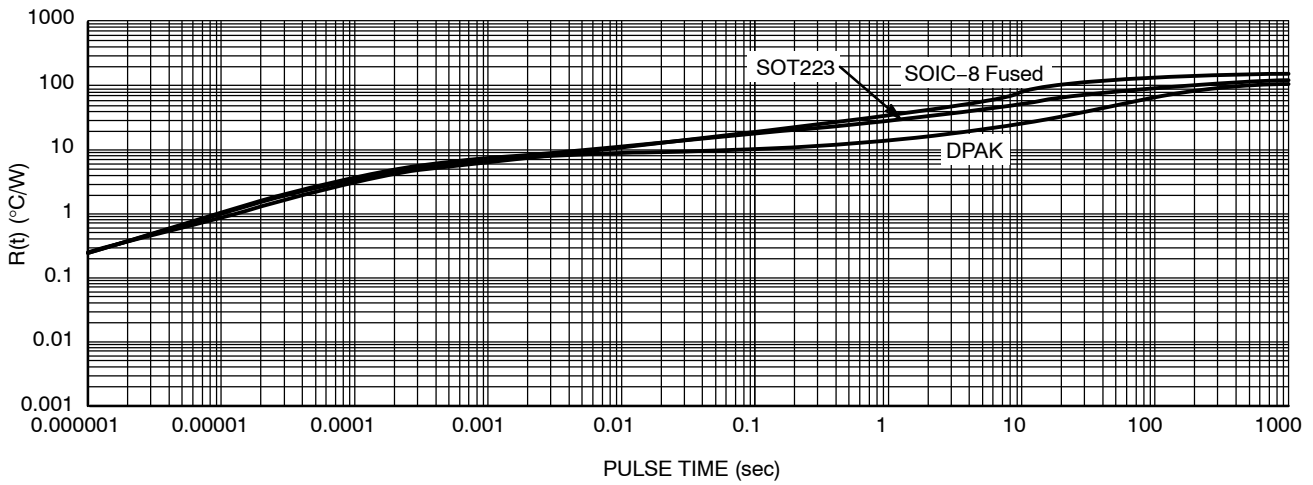**Figure 28. θJA vs. Copper Spreader Area**

Figure 29. Single−Pulse Heating Curves

ORDERING INFORMATION

Device*	Marking	Package	Shipping†
NCV8664D50R2G	V6645	SOIC−8 Fused (Pb−Free)	2500 / Tape & Reel
NCV8664D50G	V6645	SOIC−8 Fused (Pb−Free)	98 Units / Rail
NCV8664DT50RKG	V66450G	DPAK (Pb−Free)	2500 / Tape & Reel
NCV8664DT33RKG	V66433G	DPAK (Pb−Free)	2500 / Tape & Reel
NCV8664ST50T3G	V6645	SOT−223 (Pb−Free)	4000 / Tape & Reel
NCV8664ST33T3G	V6643	SOT−223 (Pb−Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.