



SANYO Semiconductors

DATA SHEET

LA6261 — Monolithic Linear IC For Optical Disk Drive 6-Channel Driver (BTL: 4 channels, H bridge: 2 channels)

Overview

The LA6261 is a 6-channel driver IC that incorporates 4 channels of BTL output and 2 channels of H-bridge output. It is optimal for the actuator driver for CDs, MDs, and other optical disk drives.

Features

- Six power amplifier channels on a single chip (BTL: 4 channels, H-bridge: 2 channels)
- I_O max: 700mA (Each channel)
- Built-in level shifter circuits (BTL amplifier)
- Built-in thermal protection (thermal shutdown) circuit
- Separate power supply for H-bridge (2 channels)
- Onchip 3.3V regulator controller (uses an external output transistor)
- Adjustment pin for the H-bridge output

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V _{CC} max		14	V
Maximum output current	I _O max	for each of the channel 1 to 6	0.7	A
Maximum input voltage	V _{INB}		13	V
MUTE pin voltage	V _{MUTE}		13	V
Allowable power dissipation	Pd max	Independent IC	0.8	W
		Mounted on the specified board *	2	W
Operating ambient temperature	T _{opr}		-30 to +85	°C
Storage ambient temperature	T _{stg}		-55 to +150	°C

* Mounted on a specified board: 76.1mm×114.1mm×1.6mm, glass epoxy.

Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V _{CC}		5.6 to 13	V

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LA6261

Electrical Characteristics at $T_a = 25^\circ\text{C}$, $V_{CC1} = V_{CC2} = 8\text{V}$, $V_{REF} = 1.65\text{V}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
All Blocks						
No-load current drain ON	I_{CC-ON}	All outputs on *1, FWD=REV=0V		30	50	mA
V_{REF} input voltage range	V_{REF-IN}		0.5		$V_{CC}-1.5$	V
BTL AMP						
Output offset voltage	V_{OFF}	BTL amplifier, the voltage difference between each channel outputs	-50		+50	mV
Input voltage range	V_{IN}	Applied to pins V_{IN1} to V_{IN4}	0		V_{CC}	V
Output voltage	V_O	Voltage between V_{O+} and V_{O-} for each channel when $R_L=8\Omega$ *2	4	5		V
Closed-circuit voltage gain	V_G	The gain from the input to the output		4		deg
MUTE ON voltage	V_{MTON}	*3	2		SV_{CC}	V
MUTE OFF voltage	V_{MTOFF}	*3	0		0.5	V
Slew rate	SR	For the independent amplifier. Times 2 when between outputs *4		0.5		V/ μs
H-bridge Block						
Output voltage	V_{O-LOAD}	Voltage between V_{O+} and V_{O-} for each channel when $R_L=10\Omega$	6.2	6.7		V
Input low level	V_{IN-L}		0		1	V
Input high level	V_{IN-H}		2		SV_{CC}	V
Output setting voltage	V_{CONT}	Voltage between V_{O+} and V_{O-} for each channel when $V_{CONT}=3\text{V}$ and $R_L=10\Omega$		2.8		V
Regulator Block						
Output voltage	V_{reg}	$I_L=100\text{mA}$	3.05	3.3	3.55	V
Output load variation	ΔV_{RL}	$I_L=0$ to 200mA	-50	0	10	mV
Supply voltage variation	ΔV_{VCC}	$V_{CC}=6$ to 12V , $I_L=100\text{mA}$	-15	21	60	mV

*1: The total current dissipation for SV_{CC} , PV_{CC1} , and PV_{CC2} with no load

*2: Output in the saturated state

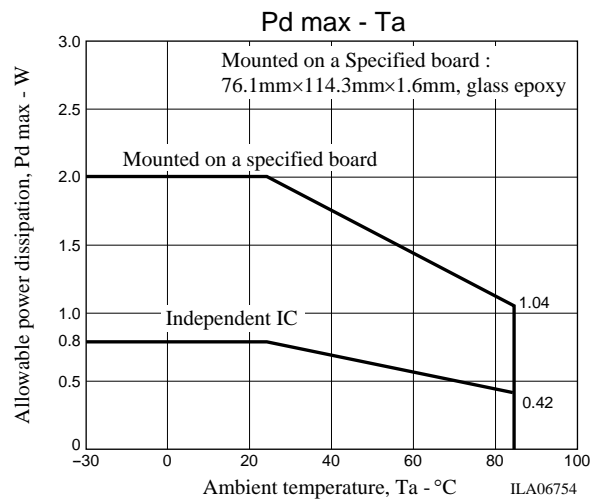
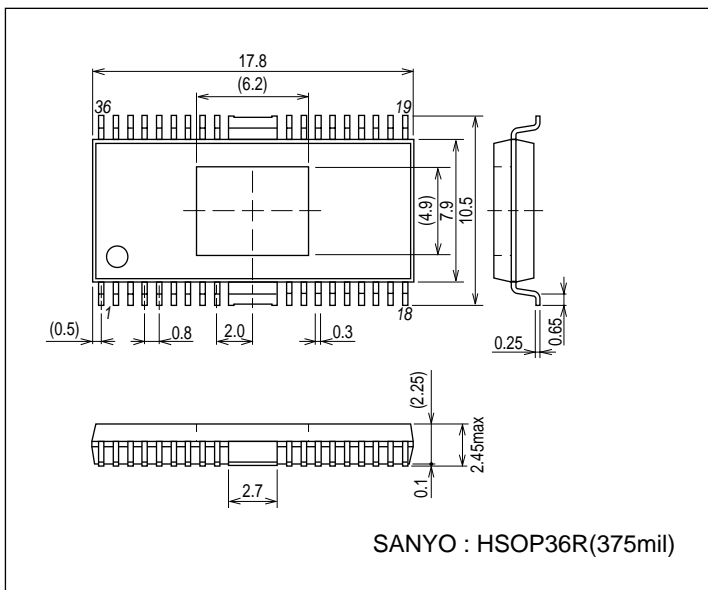
*3: When the MUTE pin is high, the BTL output will be on, and when low, the BTL output will be OFF (HI impedance).

*4: Design guarantee value

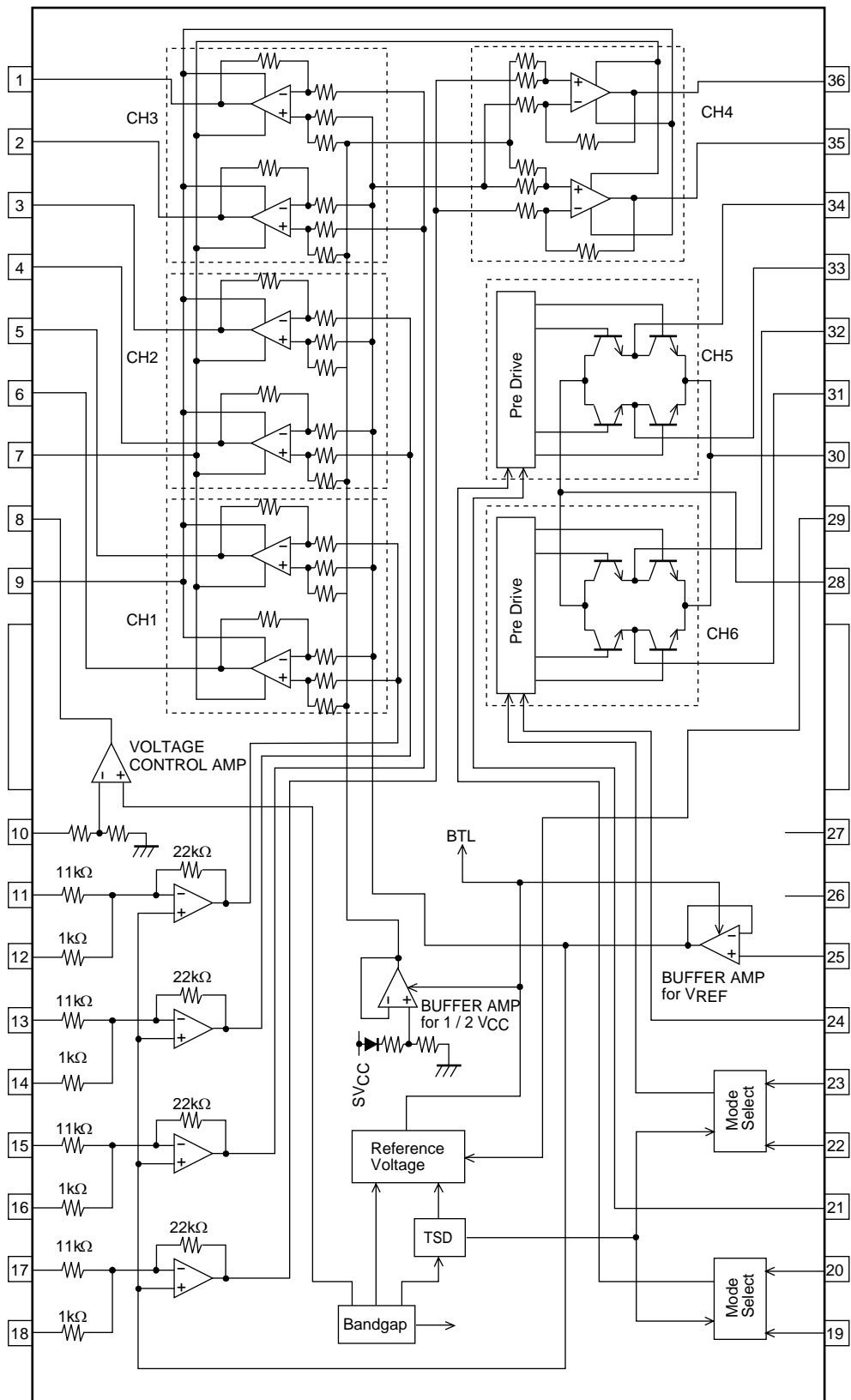
Package Dimensions

unit : mm (typ)

3251



Block Diagram



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Pin Description

Pin No.	Pin Name	Description	Equivalent Circuit Diagram	
1	V _{O3+}	Channel 3 (BTL) output (+)		
2	V _{O3-}	Channel 3 (BTL) output (-)		
3	V _{O2+}	Channel 2 (BTL) output (+)		
4	V _{O2-}	Channel 2 (BTL) output (-)		
5	V _{O1+}	Channel 1 (BTL) output (+)		
6	V _{O1-}	Channel 1 (BTL) output (-)		
7	PGND	Power system ground for channels 1 to 4 (BTL)		
9	PV _{CC1}	Power system power supply for channels 1 to 4 (BTL) (shorted to SV _{CC})		
35	V _{O4+}	Channel 4 (BTL) output (+)		
8	REGIN	Regulator (to the base of the external PNP transistor)		
10	REGOUT	Regulator (to the collector of the external PNP transistor)		
11	V _{IN1}	Channel 1 input		
12	V _{IN1G}	Channel 1 input (gain adjustment)		
13	V _{IN2}	Channel 2 input		
14	V _{IN2G}	Channel 2 input (gain adjustment)		
15	V _{IN3}	Channel 3 input		
16	V _{IN3G}	Channel 3 input (gain adjustment)		
17	V _{IN4}	Channel 4 input		
18	V _{IN4G}	Channel 4 input (gain adjustment)		
19	FWD5	Channel 5 output direction switching (FWD), H-bridge logic input		
20	REV5	Channel 5 output direction switching (REV), H-bridge logic input		
22	FWD6	Channel 6 output direction switching (FWD), H-bridge logic input		
23	REV6	Channel 6 output direction switching (REV), H-bridge logic input		

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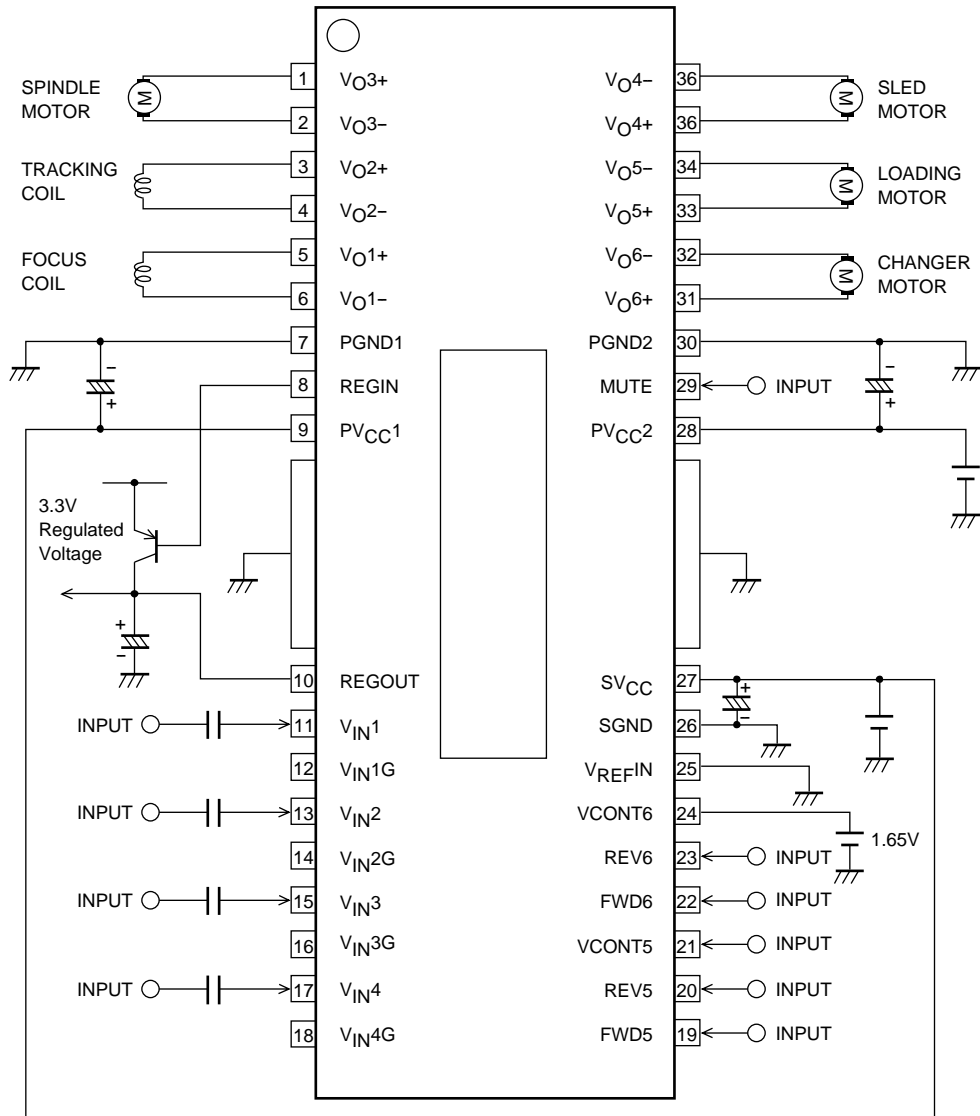
Pin No.	Pin Name	Description	Equivalent Circuit Diagram
21 24	VCONT5 VCONT6	Channel 5 output voltage setting Channel 6 output voltage setting	
25	VREFIN	Reference voltage input	
28 30 31 32 33 34	PVCC2 PGND2 VO6+ VO6- VO5+ VO5-	Power system power supply for for channels 5 and 6 (H-bridge) Power system ground for channels 5 and 6 (H-bridge) Channel 6 (H-bridge) output (+) Channel 6 (H-bridge) output (-) Channel 5 (H-bridge) output (+) Channel 5 (H-bridge) output (-)	
29	MUTE	BTL mute signal input	
26	SGND	Signal system ground	
27	SVCC	Signal system power supply (shorted to PVCC1)	

Truth Table

INPUT		OUTPUT	
FWD5(6)	REV5(6)	VO5(6)+	VO5(6)-
L	L	Z	Z
L	H	H	L
H	L	L	H
H	H	L	L

*Z: HI-Impedance

Sample Application Circuit



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