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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

FAIRCHILD SEMICONDUCTOR®

FAN6862H / FAN6862HR
Highly Integrated Green-Mode PWM Controller

Features

- Low Startup Current: 8μA
- Low Operating Current in Green Mode: 2mA
- Peak-Current Mode Operation with Cycle-by-Cycle Current Limiting
- PWM Frequency Continuously Decreasing with Burst Mode at Light Loads
- V_{DD} Over-Voltage Protection (OVP)
- Constant Output Power Limit (Full AC Input Range)
- Internal Latch Circuit (FAN6862H) for OVP, OTP
- Fixed PWM Frequency (100KHz) with Frequency Hopping
- Feedback Open-Loop Protection with 56ms Delay
- Soft Startup Time: 5ms

Applications

General-purpose switched-mode power supplies and flyback power converters, including:

- Power Adapters
- Open-Frame SMPS
- SMPS with Surge-Current Output, such as for Printers, Scanners, Motor Drivers

Description

A highly integrated PWM controller, FAN6862H(HR) provides several features to enhance the performance of flyback converters. To minimize standby power consumption, a proprietary Green-Mode function provides off-time modulation to continuously decrease the switching frequency under light-load conditions. Under zero-load conditions, the power supply enters Burst Mode, which completely shuts off PWM output. Output restarts just before the supply voltage drops below the UVLO lower limit. This Green-Mode function enables power supplies to meet international power conservation requirements.

The FAN6862H(HR) is designed for SMPS and integrates frequency-hopping function internally, which helps reduce EMI emission of a power supply with minimum line filters. The built-in synchronized slope compensation is proprietary saw-tooth compensation for constant output power limit over universal AC input range. The gate output is clamped at 18V to protect the external MOSFET from over-voltage damage.

Other protection functions include V_{DD} Over-Voltage Protection (OVP) and Over-Temperature Protection (OTP). For over-temperature protection, an external NTC thermistor can be applied to sense the ambient temperature. When V_{DD} OVP or OTP is activated, an internal latch circuit latches off the controller.

Ordering Information

Part Number	Operating Temperature Range	OVP	OLP	OTP/OTP2	Package	Packing Method
FAN6862HTY	-40 to +105°C	Latch	A/R	Latch	6-Pin, Super Small Outline Package, SuperSOT™-6	Tape & Reel
FAN6862HRTY	-40 to +105°C	Auto-Restart (A/R)			6-Pin, Super Small Outline Package, SuperSOT™-6	Tape & Reel

Typical Application

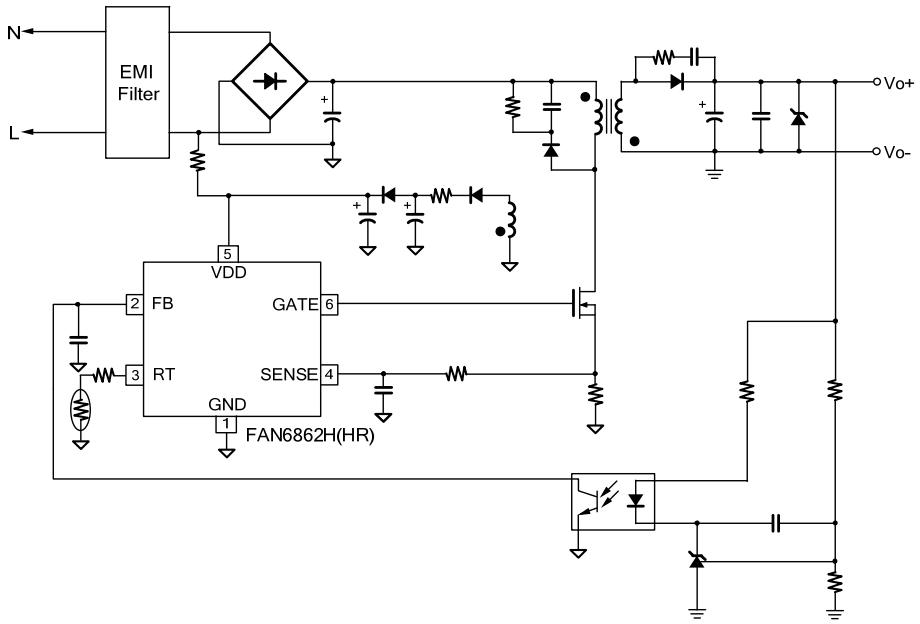


Figure 1. Typical Application

Block Diagram

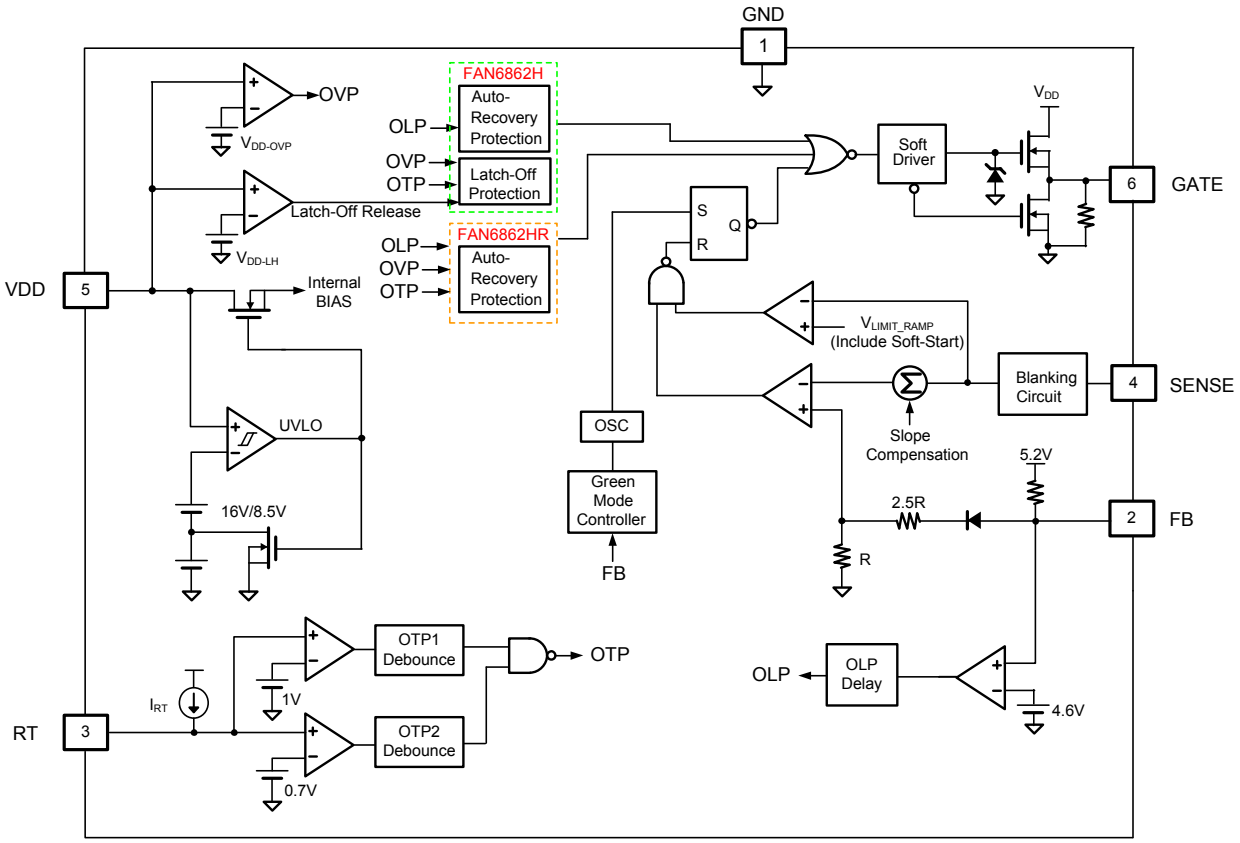
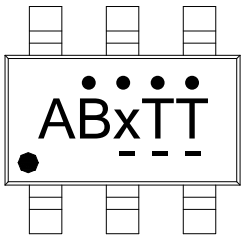


Figure 2. Block Diagram

Marking Information



ABx:	ABO: FAN6862HTY ABP: FAN6862HRTY
TT:	Wafer Lot Code
●●●●:	Year Code
_ _ _:	Week Code

Figure 3. Top Mark

Pin Configuration

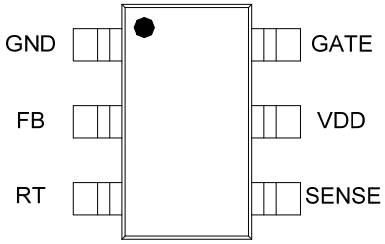


Figure 4. Pin Assignments

Pin Definitions

Pin #	Name	Function	Description
1	GND	Ground	Ground
2	FB	Feedback	Feedback. The FB pin provides the output voltage regulation signal. It provides feedback to the internal PWM comparator, so the PWM comparator can control the duty cycle. This pin also provides OCP: once V_{FB} is larger than the trigger level and lasts for a long time, the controller stops and restarts.
3	RT	Temperature Detection	For over-temperature protection, an external NTC thermistor is connected from this pin to the GND pin. The impedance of the NTC thermistor decreases at high temperatures. Once the voltage of the RT pin drops below a threshold, PWM output is disabled.
4	SENSE	Current Sense	This pin senses the voltage across a resistor. When the voltage reaches the internal threshold, PWM output is disabled. This activates over-current protection. This pin also provides current amplitude information for current-mode control.
5	VDD	Power Supply	Power supply
6	GATE	Driver Output	The totem-pole output driver for driving the power MOSFET.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. All voltage values, except differential voltages, are given with respect to GND pin.

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Supply Voltage		30	V
V_L	Input Voltage to FB, SENSE, RT Pins	-0.3	7.0	V
P_D	Power Dissipation at T_A<50°C		300	mW
Θ_{JC}	Thermal Resistance (Junction-to-Case)		115	°C/W
T_J	Operating Junction Temperature	-40	+125	°C
T_{STG}	Storage Temperature Range	-55	+150	°C
T_L	Lead Temperature, Wave Soldering, 10 Seconds		+260	°C
ESD	Human Body Model, JESD22-A114		4	kV
	Charge Device Model, JESD22-C101		2	

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
T_A	Operating Ambient Temperature	-40	+105	°C

Electrical Characteristics

V_{DD} = 15V and T_A = 25°C unless otherwise noted.

Symbol	Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{DD} Section							
V_{DD-OP}	Continuously Operating Voltage					24	V
V_{DD-ON}	Turn-On Threshold Voltage			15	16	17	V
V_{DD-OFF}	Turn-Off Voltage			7.5	8.5	9.5	V
V_{DD-LH}	Threshold voltage for Latch-Off release			3	4	5	V
I_{DD-ST}	Startup Current		V_{TH-ON} – 0.16V		8	30	µA
I_{DD-OP}	Normal Operating Supply Current		With 1nF Load on Gate, $V_{FB} \geq V_{FB-N}$		3	4	mA
I_{DD-BM}	Green Mode Operating Supply Current		GATE Open, $V_{FB} = V_{FB-G}$			2.5	mA
V_{DD-OVP}	V_{DD} Over Voltage Protection		FAN6862H Latch, FAN6862HR Auto-Restart	24	25	26	V
$t_{D-VDDOVP}$	V_{DD} OVP Debounce Time				30	50	µs
I_{DD-LH}	Latch-Off Holding Current		V_{DD} = 5V		40	65	µA
Feedback Input Section							
A_V	Input-Voltage to Current-Sense Attenuation			1/4.0	1/3.5	1/3.0	V/V
Z_{FB}	Input Impedance				6		kΩ
V_{FBO}	FB Pin Open Voltage			5.0	5.2	5.4	V
V_{FB-OLP}	Threshold Voltage for Open-Loop Protection			4.3	4.6	4.9	V
t_{D-OLP}	Open-Loop Protection Delay				56		ms
Current Sense Section							
t_{PD}	Delay to Output				100	250	ns
t_{LEB}	Leading-Edge Blanking Time			270	360		ns
V_{STHFL}	Flat Threshold Voltage for Current Limit		Duty>51%	0.52	0.55	0.58	V
V_{STHVA}	Valley Threshold Voltage for Current Limit		Duty = 0%	0.37	0.40	0.43	V
$t_{SOFT-START}$	Period During Startup		Startup Time	4	5	6	ms
Oscillator Section							
f_{OSC}	Normal PWM Frequency	Center Frequency	$V_{FB} > V_{FB-N}$	95.5	100.0	104.5	kHz
		Hopping Range	$V_{FB} \geq V_{FB-N}$	±5.9	±6.5	±7.3	
		Hopping Range[1]	$V_{FB} = V_{FB-G}$		±2.9		
t_{hop-1}	Hopping Period 1[1]		$V_{FB} \geq V_{FB-N}$		4.4		ms
t_{hop-3}	Hopping Period 3[1]		$V_{FB} = V_{FB-G}$		11.5		ms
f_{OSC-G}	Green Mode Minimum Frequency			23	25	27	kHz
V_{FB-N}	FB Threshold Voltage For Frequency Reduction			2.4	2.6	2.8	V
V_{FB-G}	FB Voltage at f_{OSC-G}			1.9	2.1	2.3	V
V_{FB-ZDC}	FB Threshold Voltage for Zero Duty				1.7		V
f_{DV}	Frequency Variation vs. V_{DD} Deviation		V_{DD} = 11.5V to 20V		0.02		%
f_{DT}	Frequency Variation vs. Temperature Deviation		T_A = -40 to +105°C			2	%

Continued on following page…

Electrical Characteristics (Continued)

V_{DD} = 15V, T_A = 25°C, unless noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
PWM Output Section						
DCY_{MAX}	Maximum Duty Cycle		60	65	70	%
V_{OL}	Output Voltage Low	V_{DD} = 15V, I_O = 50mA			1.5	V
V_{OH}	Output Voltage High	V_{DD} = 8V, I_O = 50mA	6			V
t_R	Rising Time	GATE = 1nF		150	200	ns
t_F	Falling Time	GATE = 1nF		35	80	ns
V_{CLAMP}	Gate Output Clamping Voltage	V_{DD} = 20V	15.0	16.5	18.0	V
Over-Temperature Protection (OTP) Section						
I_{RT}	Output Current of RT Pin		92	100	108	µA
V_{OTP}	Threshold Voltage for Over-Temperature Protection	FAN6862H Latch, FAN6862HR Auto-Restart	0.97	1.00	1.07	V
t_{DOTP}	Over-Temperature Debounce Time	V_{FB} = V_{FB-N}	15	17	19	ms
		V_{FB} = V_{FB-G} (1)		51		
V_{OTP2}	2nd Threshold Voltage for Over-Temperature Protection	FAN6862H Latch, FAN6862HR Auto-Restart	0.65	0.70	0.75	V
t_{DOTP2}	2nd Over-Temperature Debounce Time		80	200	250	µs

Note:
1. Guarantee by design.

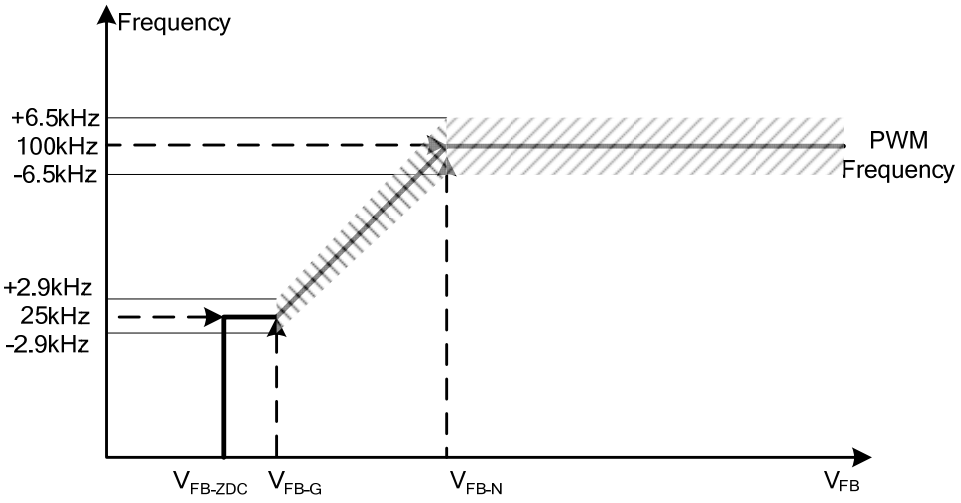


Figure 5. PWM Frequency

Typical Performance Characteristics

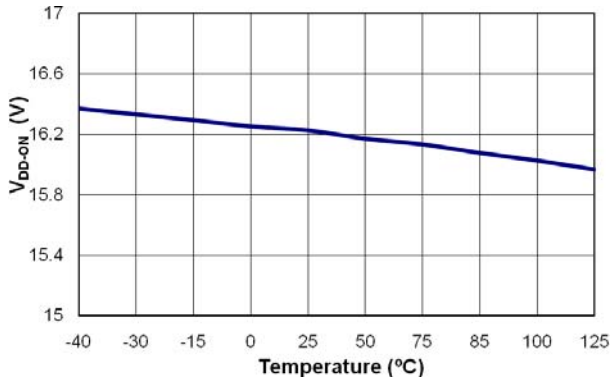


Figure 6. Turn-On Threshold Voltage (V_{DD-ON}) vs. Temperature

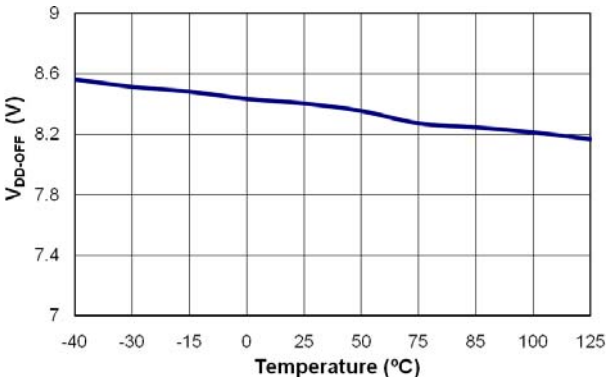


Figure 7. Turn-Off Threshold Voltage (V_{DD-OFF}) vs. Temperature

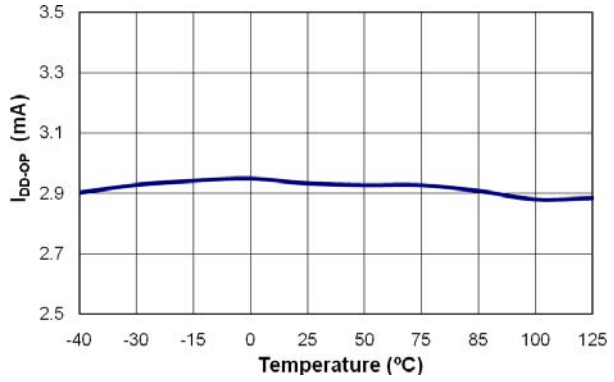


Figure 8. Operating Current (I_{DD-OP}) vs. Temperature

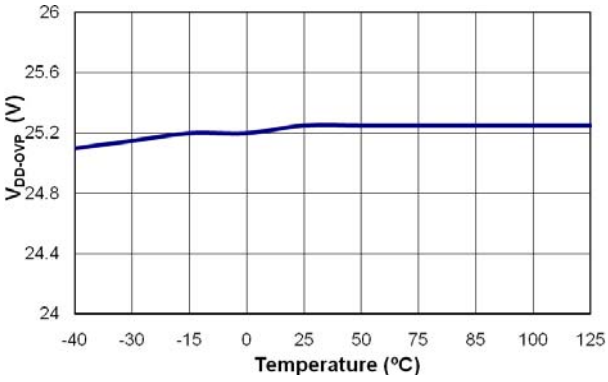


Figure 9. V_{DD} Over-Voltage Protection (V_{DD-OVP}) vs. Temperature

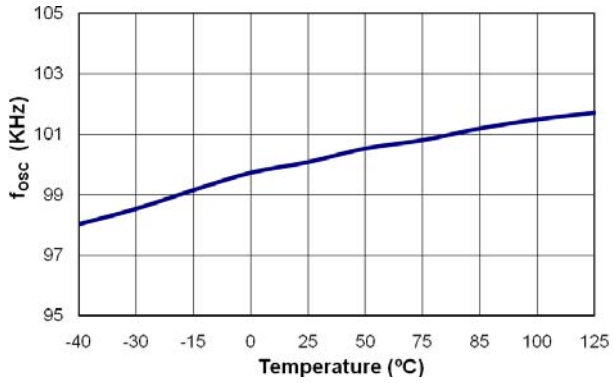


Figure 10. Center Frequency (f_{OSC}) vs. Temperature

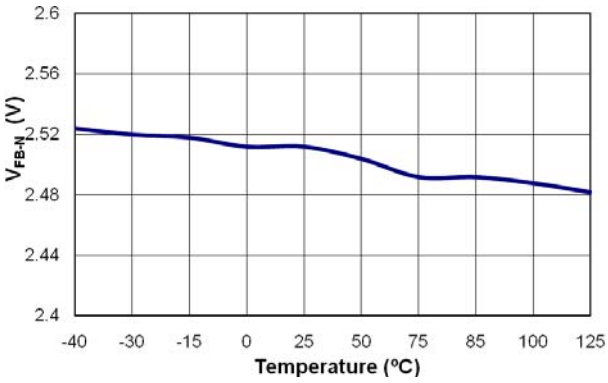


Figure 11. FB Threshold Voltage for Frequency Reduction (V_{FB-N}) vs. Temperature

Typical Performance Characteristics (Continued)

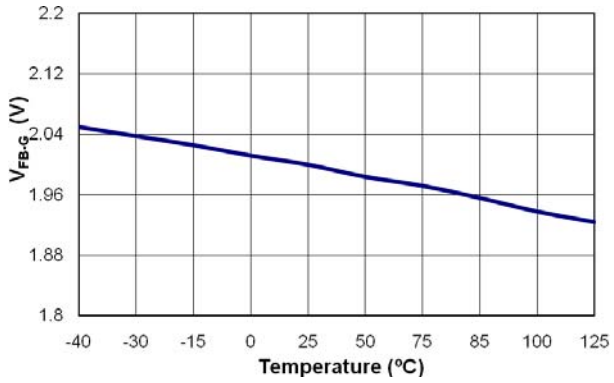


Figure 12. FB Voltage at f_{OSC-G} (V_{FB-G}) vs. Temperature

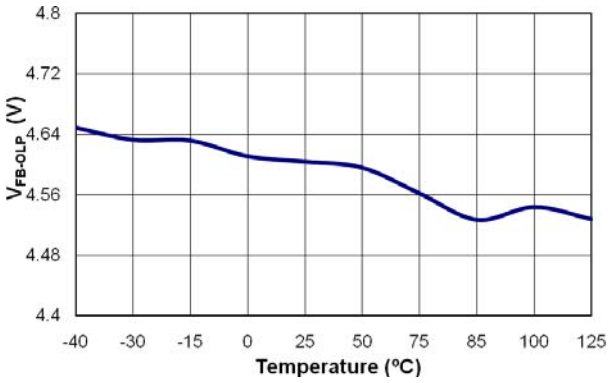


Figure 13. Threshold Voltage for Open-Loop Protection (V_{FB-OLP}) vs. Temperature

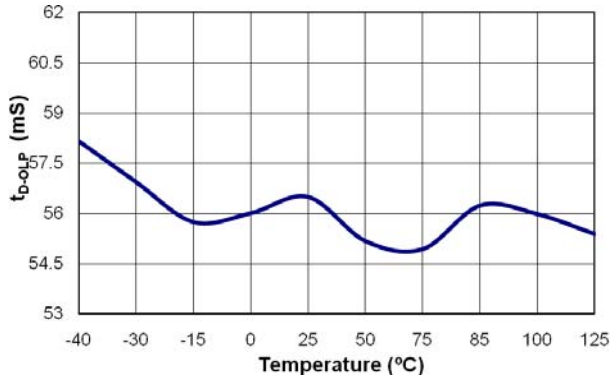


Figure 14. Open-Loop Protection Delay (t_{D-OLP}) vs. Temperature

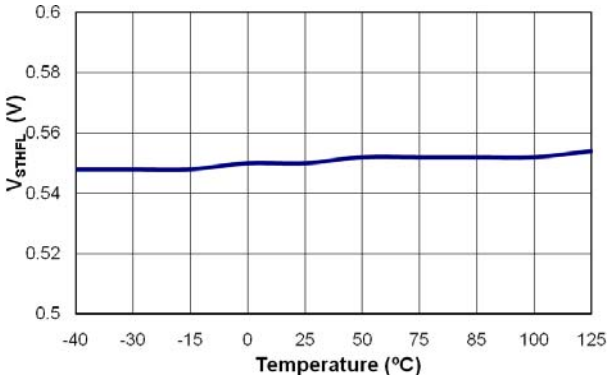


Figure 15. Flat Threshold Voltage for Current Limit (V_{STHFL}) vs. Temperature

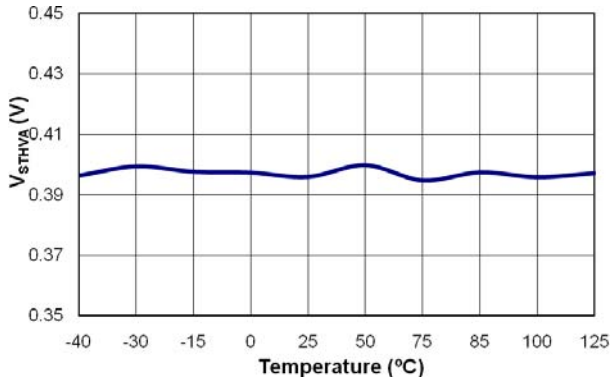


Figure 16. Valley Threshold Voltage for Current Limit (V_{STHVA}) vs. Temperature

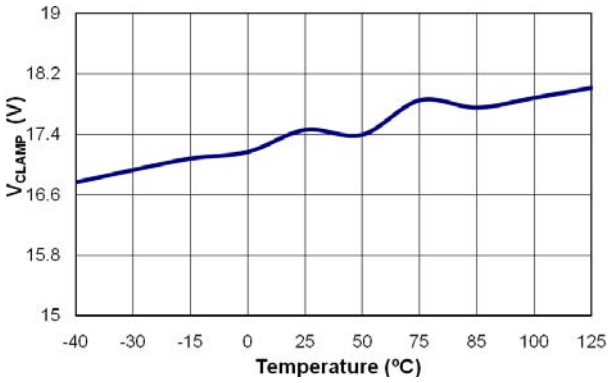


Figure 17. GATE Output Clamping Voltage (V_{CLAMP}) vs. Temperature

Typical Performance Characteristics (Continued)

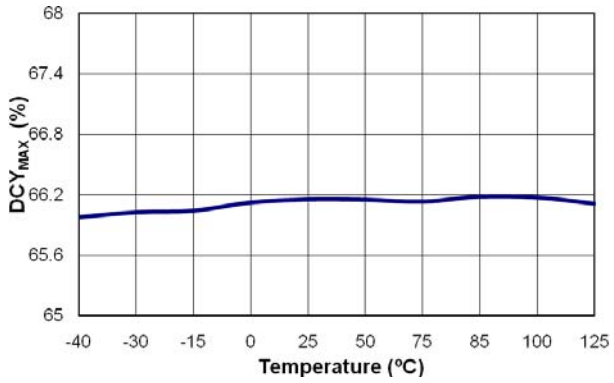


Figure 18. Maximum Duty Cycle (DCY_{MAX}) vs. Temperature

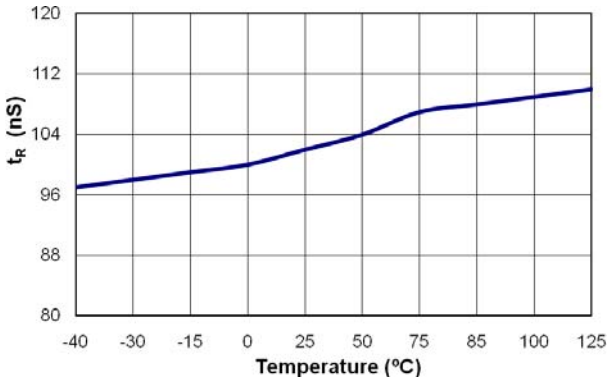


Figure 19. Rising Time (t_R) vs. Temperature

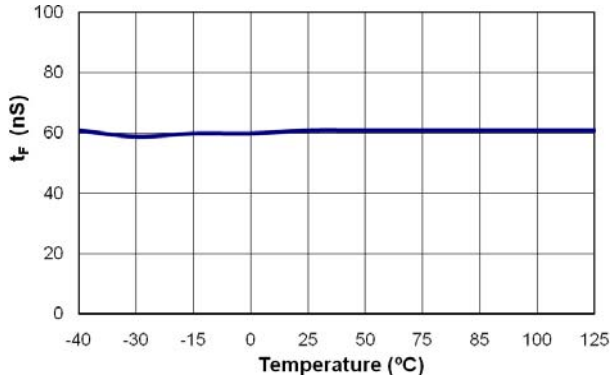


Figure 20. Falling Time (t_F) vs. Temperature

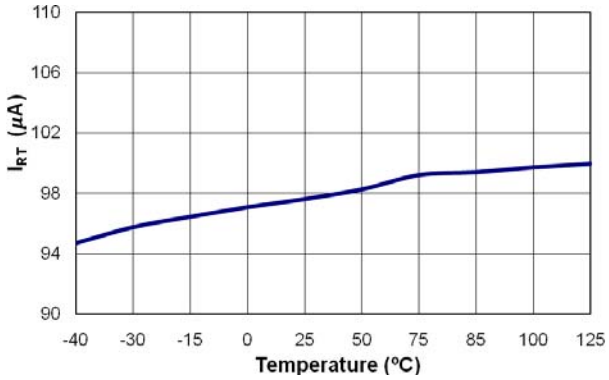


Figure 21. Output Current of RT Pin (I_{RT}) vs. Temperature

Operation Description

Startup Operation

Figure 22 shows a typical startup circuit and transformer auxiliary winding for a FAN6862H(HR) application. Before FAN6862H(HR) begins switching, it consumes only startup current (typically 8μA) and the current supplied through the startup resistor charges the V_{DD} capacitor (C_{DD}). When V_{DD} reaches a turn-on voltage of 16V (V_{DD-ON}), switching begins and the current consumed increases to 2mA. Then, the power required is supplied from the transformer auxiliary winding. The large hysteresis of V_{DD} (8.5V) provides more holdup time, which allows using a small capacitor for V_{DD}. The startup resistor is typically connected to the AC line for a fast reset of latch protection.

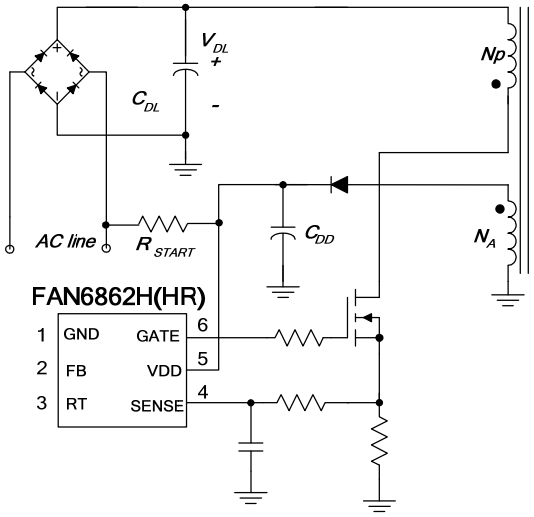


Figure 22. Startup Circuit

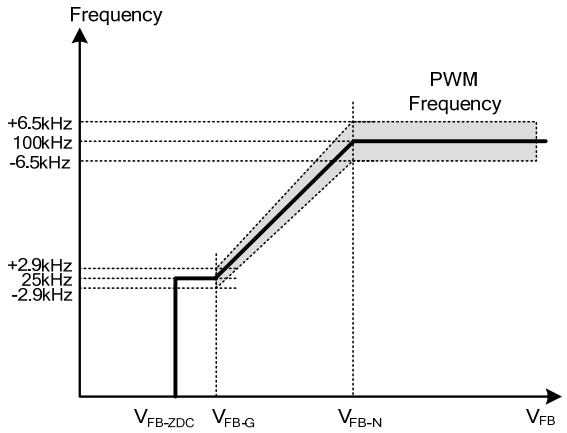


Figure 23. PWM Frequency

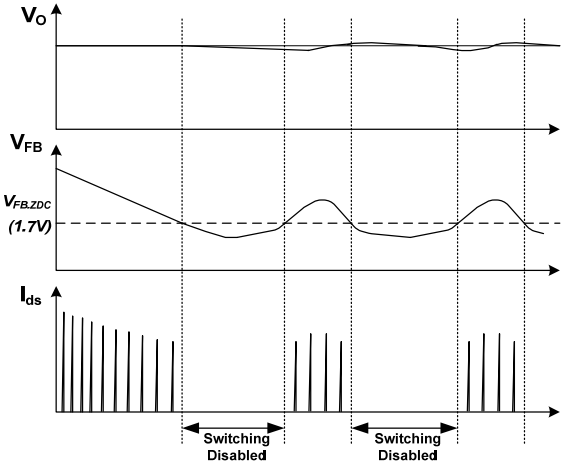


Figure 24. Burst-Mode Operation

Green-Mode Operation

The FAN6862H(HR) uses feedback voltage (V_{FB}) as an indicator of the output load and modulates the PWM frequency, as shown in Figure 23, such that the switching frequency decreases as load decreases. In heavy-load conditions, the switching frequency is 65KHz. Once V_{FB} decreases below V_{FB-N} (2.6V), the PWM frequency starts to linearly decrease from 100KHz to 25kHz to reduce the switching losses. As V_{FB} decreases below V_{FB-G} (2.1V), the switching frequency is fixed at 25kHz and FAN6862H(HR) enters “deep” Green Mode, where the operating current decreases to 2.5mA (maximum), further reducing the standby power consumption. As V_{FB} decreases below V_{FB-ZDC} (1.7V), FAN6862H(HR) enters Burst Mode. When V_{FB} drops below V_{FB-ZDC}, FAN6862H(HR) stops switching and the output voltage starts to drop, which causes the feedback voltage to rise. Once V_{FB} rises above V_{FB-ZDC}, switching resumes. Burst Mode alternately enables and disables switching, reducing switching loss in standby mode, as shown in Figure 24.

Frequency Hopping

EMI reduction is accomplished by frequency hopping, which spreads the energy over a wider frequency range than the bandwidth measured by the EMI test equipment. An internal frequency hopping circuit changes the switching frequency between 93.5kHz and 106.5kHz with a period of 4.4ms, as shown in Figure 25.

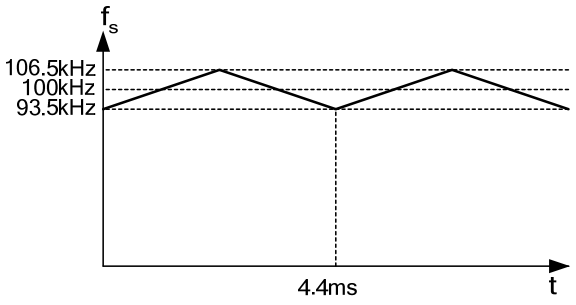


Figure 25. Frequency Hopping

Protections

Self-protective functions include V_{DD} Over-Voltage Protection (OVP), Open-Loop / Overload Protection (OLP), Over-Current Protection (OCP), Short-Circuit Protection (SCP), and Over-Temperature Protection (OTP). OLP, OCP, and SCP are Auto-Restart Mode protections; OVP and OTP are Latch-Mode protections. In FAN6862HR, all of these protections are applied with Auto-Restart Mode.

Auto-Restart Mode Protections

Once a fault condition is detected, switching is terminated and the MOSFET remains off. This causes V_{DD} to fall because no more power is delivered from the auxiliary winding. When V_{DD} falls to V_{DD-OFF} (8.5V), the protection is reset and the operating current reduces to startup current, which causes V_{DD} to rise. FAN6862H(HR) resumes normal operation when V_{DD} reaches V_{DD-ON} (16V). In this manner, the auto-restart can alternately enable and disable MOSFET switching until the fault condition is eliminated (*see Figure 26*).

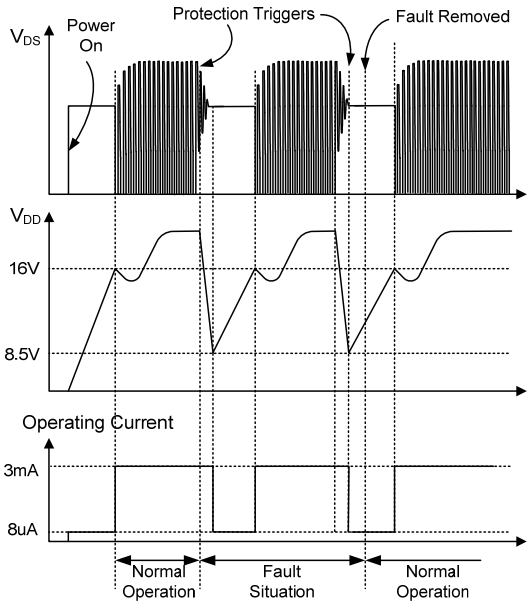


Figure 26. Auto-Restart Operation

Latch-Mode Protections

Once this protection is triggered, switching is terminated and the MOSFET remains off. The latch is reset only when V_{DD} is discharged below 4V by unplugging the AC power line.

Over-Current Protection (OCP)

FAN6862H(HR) has two over-current protection thresholds. One is for pulse-by-pulse current limit, which turns off MOSFET for the remainder of the switching cycle when the sensing voltage of MOSFET drain current reaches the threshold. The other threshold is for the over-current protection, which shuts down the MOSFET gate when the sensing voltage of MOSFET drain current is above the threshold longer than the shutdown delay (56ms).

Open-Loop / Overload Protection (OLP)

When the upper branch of the voltage divider for the shunt regulator (KA431 shown in Figure 27) is broken, no current flows through the opto-coupler transistor, which pulls up the feedback voltage to 5.2V.

When feedback voltage is above 4.6V for longer than 56ms, OLP is triggered. This protection is also triggered when the SMPS output drops below the nominal value for longer than 56ms due to the overload condition.

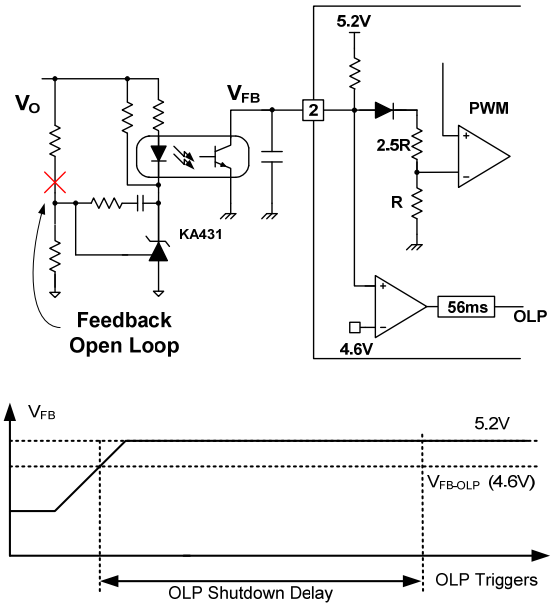


Figure 27. OLP Operation

V_{DD} Over-Voltage Protection (OVP)

V_{DD} over-voltage protection prevents IC damage caused by over voltage on the VDD pin. The OVP is triggered when V_{DD} reaches 25V. A debounce time (typically 30μs) prevents false triggering by switching noise.

Over-Temperature Protection (OTP)

The OTP circuit is composed of current source and voltage comparators. Typically, an NTC thermistor is connected between the RT and GND pins. If the voltage of this pin drops below a threshold of 1.0V, PWM output is disabled after t_{DOTP} debounce time. If this pin drops below 0.7V, it triggers the latch-off protection immediately after t_{DOTP2} debounce time.

Typical Application Circuit (Netbook Adapter by Flyback)

Application	Fairchild Devices	Input Voltage Range	Output
Netbook Adapter	FAN6862H(HR)	90~265V_{AC}	19V / 2.1A (40W)

Features

- High efficiency (>85.3% at full-load condition), meeting EPS regulation with enough margin
- Low standby (pin<0.15W at no-load condition)
- Soft-start time: 5ms

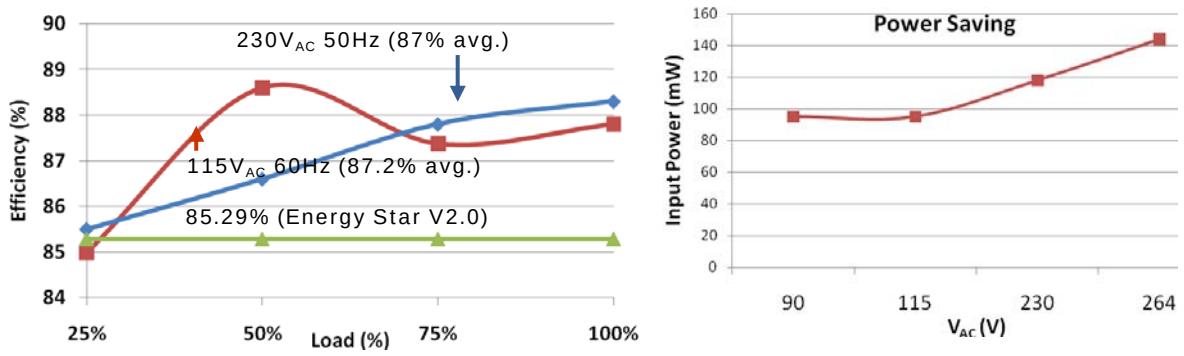


Figure 28. Measured Efficiency and Power Saving

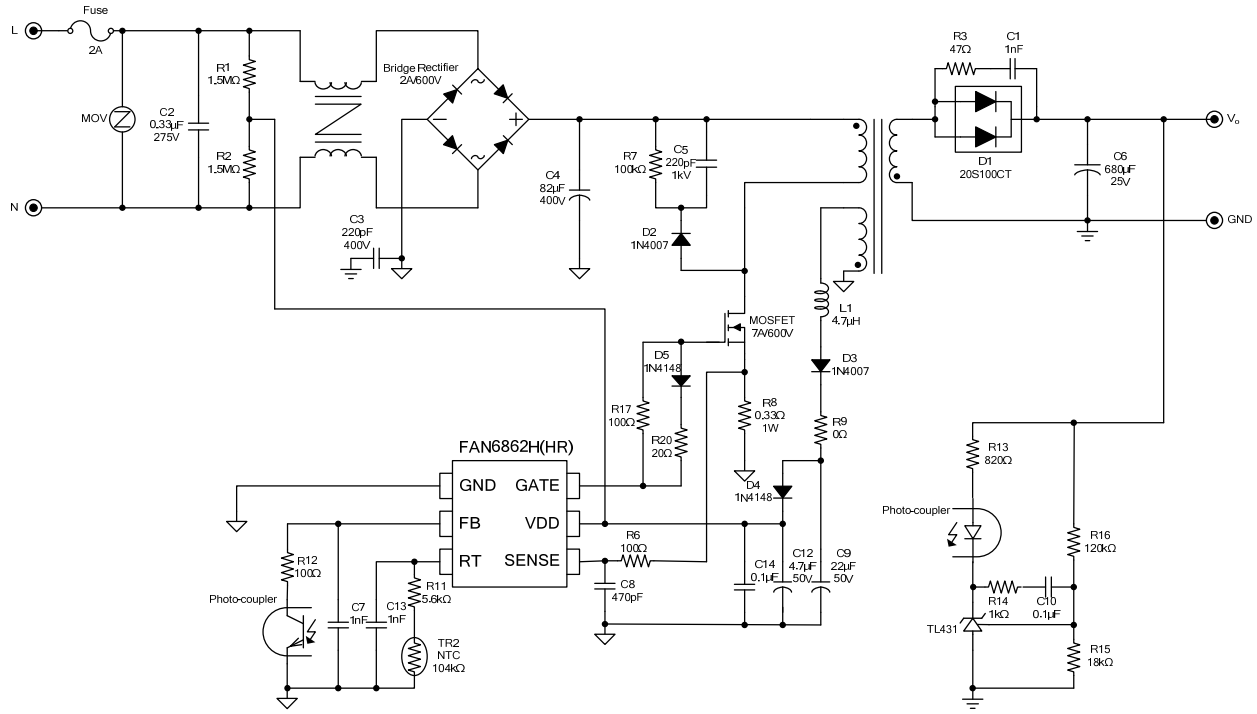


Figure 29. Schematic of Typical Application Circuit

Transformer Specification

- Core: RM 8
- Bobbin: RM 8

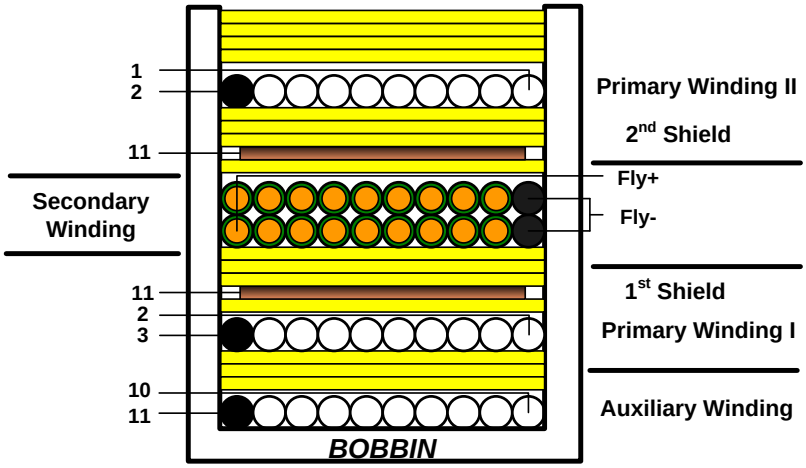


Figure 30. Transformer

NO	Terminal		Wire	Ts	Insulation	Barrier	
	S	F			Ts	Primary	Secondary
N1	11	10	0.37 • 1	7	3		
N2	3	2	0.37 • 1	22	1		
	11		COPPER SHIELD	1.2	3		
N3	Fly-	Fly+	0.75 • 2	8	1		
	11		COPPER SHIELD	1.2	3		
N4	2	1	0.37 • 1	22	4		
			CORE ROUNDING TAPE		3		

	Pin	Specification	Remark
Primary-Side Inductance	3—1	610μH ±5%	100kHz, 1V
Primary-Side Effective Leakage	3—1	15μH Maximum	Short One of the Secondary Windings

Physical Dimensions

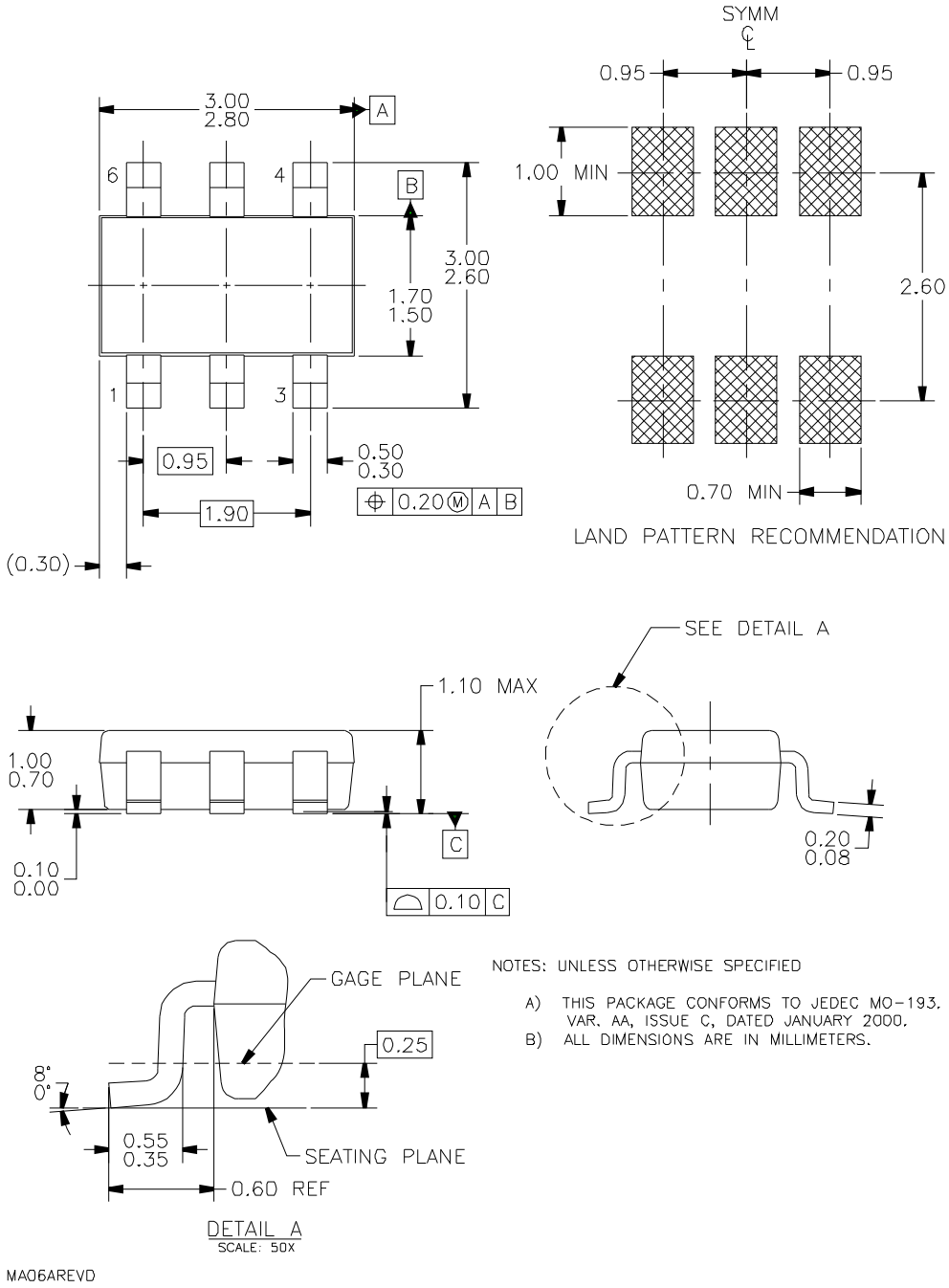


Figure 31. 6-Pin, SuperSOT™6, JEDEC MO-193, 1.6mm Wide

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