LV8415XA

Bi-CMOS IC

Blurring correction driver H bridge x 2-channel driver

Overview

LV8415XA is dual channel H-bridge driver IC for digital still camera.

Function

- Actuator driver (saturation drive H bridge) × 2-channel
- Hall Amplifier × 2-channel
- Constant current hall bias circuit × 2-channel
- General-purpose amplifier × 2-channel
- With built-in for PWM signal generation logic circuit × 2-channel
- 8-bit DAC for hall bias × 2-channel
- 8-bit DAC for hall amplifier offset adjustment × 2-channel
- Three line serial input
- Two systems in power supply (V_M: for actuator, V_{CC})
- With built-in thermal protection circuit
- With built-in low voltage malfunction prevention circuit

Specifications

Absolute Maximum Ratings at $Ta = 25^{\circ}C$

		6		
Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage 1	V _M max		6	V
Supply voltage 2	V _{CC} max		6	V
Output peak current	I _O peak	OUT1 to 2 (t \leq 10msec, duty \leq 20%)	600	mA
Output current	I _O max	OUT1 to 2	350	mA
Hall bias current	I _{HB} max		5	mA
Allowable power dissipation	Pd max	On a specified board *	1	W
Operating temperature	Topr		-20 to +85	°C
Storage temperature	Tstg		-55 to +150	°C

* Specified board: 40.0mm×50.0mm×0.8mm, Four layers fiberglass epoxy circuit board.

* 2 Tjmax=150°C Please design PCB so that internal chip temperature does not exceed 150 °C.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Allowable Operating Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage range 1	VM		2.7 to 5.5	V
Supply voltage range 2	V _{CC}		2.7 to 5.5	V
Logic input voltage	V _{IN}		0 to V _{CC} +0.3	V

ORDERING INFORMATION

See detailed ordering and shipping information on page 13 of this data sheet.

Semiconductor Components Industries, LLC, 2014 January, 2014





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Parameter	Symbol	Conditions		Ratings		Unit
			min	typ	max	
Current consumption when	Icco	ST = "L"			1.0	μA
Standing by	1	$V_{\rm ex} = 5.0V/ST = "H"$ pollogd			10	
		VM = 5.0V, 31 = 11, 10 load		2	2.0	μA
			2.1	2 40	3.2	
VCC low voltage cutting voltage	VIHVCC		2.1	2.40	2.0	V m)/
		Decise succession	100	150	200	v
Thermal shutdown temperature		Design guarantee	100	175	195	ै । ।
	AISD	Design guarantee	15	35	55	Ů
H bridge output (OU11-2)	_					_
Output on resistance	Ronu	I _O = 100mA, Upper-side on resistance		0.7	0.98	Ω
	Rond	I _O = 100mA, Under-side on resistance		0.5	0.7	Ω
Output leakage current	I _O leak				1	μA
Diode forward voltage	VD	ID = -100mA		0.7		V
Operational amplifier (OP-AMP	1-4)					
Input offset voltage	OP_VIO			±1	±5	mV
Input offset current	OP_IIO			±5	±50	nA
Input bias current	OP_IB			30	250	nA
Equal phase input voltage range	VICM		0		V _{CC}	V
Equal phase signal removal	CMR	$R_L = 20k\Omega$, VIN = 1mV(open loop gain)	60	80		dB
ratio						
Large amplitude voltage range	VG	$R_L = 20k\Omega$	1	10		V/mV
Output voltage range	V _O H	$R_L = 20k\Omega$	V _{CC} -0.2			V
	V _O L				0.2	V
Power supply change removal	SVR		65	85		dB
ratio						
Output current (sink/source)	OP_IO		1	2		mA
Hall bias (HB1-2)	1					
Output current	IHB	RHG = $1k\Omega$, VHBIN = $1.0V$	0.95	1.00	1.05	mA
Output saturation voltage	VSATHB	I _{HB} = 1mA	V _{CC} -0.2			V
Reference voltage	1	1				1
Reference voltage	VREF		1.60	1.65	1.70	V
Reference voltage load	VRref	I _{REF} = 100μA	1.60	1.65	1.70	V
characteristic						<u> </u>
Internal CLK frequency for PWM	/ drive					
CLK frequency	Fclk		13.5	15	17.25	MHz
Control pin (ST, SCLK, DATA, S	ТВ)	T				
Built-in pull-down resistance	Rin		50	100	200	kΩ
Input current	IINL	V _{IN} = 0V			1.0	μA
	IINH	V _{IN} = 3.3V	20	33	50	μA
Input "L" level voltage	VINL				1.0	V
Input "H" level voltage	VINH		2.5			V

Electrical Characteristics at Ta = 25°C, V_{CC} = 3.3V, V_M = 5.0V

Block Diagram





SIDE VIEW

Package Dimensions







Pin Assignment



Pin fund	ction		
Pin No.	Pin name	Pin function	Equivalent Circuit
E2 E3 E4 E5	ST SCLK DATA STB	Input pin. High level 2V to (V _{CC} = 3.3V) Low level 0 to 0.5V (V _{CC} = 3.3V)	
F1 F2 F4 F5 E1 F3	OUT1A OUT1B OUT2A OUT2B VM PGND	Output pin. (PWM output) VM : POWER – Power supply pin. PGND : POWER – GND pin.	
D1		Signal system power supply pin	
C1 B1 C6 B6	HB1 HGND1 HB2 HGND2	HB1, 2 pin Hall bias source pin HGND1, 2 pin Hall bias current setting pin	V _{CC} (N) HGND HGND GND
A1 A2 A3 A6 A5 A4	V _{IN} +1 V _{IN} -1A V _{IN} -1B V _{IN} +2 V _{IN} -2A V _{IN} -2B	Hall amplifier input pin V _{IN} + Hall amplifier+ input pin V _{IN} -A Hall amplifier- input pin V _{IN} -B LPF formation pin (The filter is formed for the noise removal.)	V _{CC} 3.6kΩ 3.6kΩ 3kΩ 3.6kΩ 3kΩ 3.6kΩ 3kΩ 3.6kΩ 3kΩ 3.6kΩ 3.6kΩ
B3 B4	VOUT1 VOUT2	Hall amplifier output pin. VOUT1 : Hall amplifier 1ch output pin. VOUT2 : Hall amplifier 2ch output pin.	

Continued on next page.

Continued from	n preceding page.		
Pin No.	Pin name	Pin function	Equivalent Circuit
D2 C2 D5 C5	VIN+3 VIN-3 VIN+4 VIN+4	General purpose amplifier input pin. V_{IN} +3 : 3ch general purpose amplifier+ input pin V_{IN} -3 : 3ch general purpose amplifier- input pin V_{IN} +4 : 4ch general purpose amplifier+ input pin V_{IN} -4 : 4ch general purpose amplifier- input pin	V _{CC}
B2 B5	VOUT3 VOUT4	General purpose amplifier output pin. VOUT3 : 3ch general purpose amplifier output pin VOUT4 : 4ch general purpose amplifier output pin	
E6	VREF	Internal standard voltage pin V _{CC} /2 output	VCC
F6	NC-TEST	N.C. pin TEST pin Please NC_TEST pin connect GND line.	

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3 line serial communication electrical Characteristics at Ta = 25°C, V_{CC} = 3.3V, V_M = 5.0V

				Ratings			
Parameter	Symbol	Conditions	min	typ	max	onit	
Serial data forwarding pin							
Logic pin input current	IINL	V _{IN} =0V(SCLK, DATA, STB)			1.0	μA	
	IINH	V _{IN} =3.3V(SCLK, DATA, STB)		33	50	μA	
Input "H" level voltage	VINH	SCLK, DATA, STB	2.5			V	
Input "L" level voltage	∨ _{IN} L	SCLK, DATA, STB			1.0	V	
Minimum SCLK "H" pulse width	т _{SC} H		0.1			μS	
Minimum SCLK "L" pulse width	T _{SC} L		0.1			μS	
STB regulation time	Tlat		0.1			μS	
Minimum STB pulse width	Tlatw		0.1			μS	
Data set-up time	Tds		0.1			μS	
Data hold time	Tdh		0.1			μS	
maximum CLK frequency	Fclk				4	MHz	



Serial data timing condition

Serial data input timing chart



It inputs it from A0 in order of D11. The data transfer is done by the rising edge, and after all data transfers, the latch does all data to SCLK by the STB signal standing up. The STB signal accepts and the internal logic of IC doesn't accept the SCLK signal during "H".

Serial logic map

PWMh - bridge relation serial map

	-						I	nput	-							Setting mode	Set content	Demarks
A0	A1	A2	A3	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	Setting mode	Ser content	Remarks
0	0	0	0	*	*	0	0	0	0	0	0	0	0	0	0		100%	
				*	*	1	0	0	0	0	0	0	0	0	0		$511/512 \times 100\%$	
				*	*	0	1	0	0	0	0	0	0	0	0		$510/512 \times 100\%$	Reverse
																		Reverse
				*	*	0	1	1	1	1	1	1	1	1	0		$2/512\times100\%$	
				*	*	1	1	1	1	1	1	1	1	1	0		$1/512 \times 100\%$	
				*	*	0	0	0	0	0	0	0	0	0	1	1ch PWM Duty set	0%	Middle point
				*	*	1	0	0	0	0	0	0	0	0	1		1/512 × 100%	Four
				*	*	0	1	0	0	0	0	0	0	0	1		2/512 × 100%	
								-										Normal
				*	*	1	0	1	1	1	1	1	1	1	1		509/512 × 100%	rotation
				*	*	0	1	1	1	1	1	1	1	1	1		510/512 × 100%	
				*	*	1	1	1	1	1	1	1	1	1	1		511/512 × 100%	
1	0	0	0	*	*	0	0	0	0	0	0	0	0	0	0		100%	
				*	*	1	0	0	0	0	0	0	0	0	0		511/512 × 100%	
				*	*	0	1	0	0	0	0	0	0	0	0		510/512 × 100%	
																		Reverse
				*	*	0	1	1	1	1	1	1	1	1	0		2/512 × 100%	
				*	*	1	1	1	1	1	1	1	1	1	0		$1/512 \times 100\%$	
				*	*	0	0	0	0	0	0	0	0	0	1	2ch PWM Duty set	0%	Middle
				*	*	1	0	0	0	0	0	0	0	0	1		1/512 × 1000/	point
				*	*	1	1	0	0	0	0	0	0	0	1		1/312 × 100%	
						0	1	0	0	0	0	0	0	0	1		2/312 × 100%	Normal
				*	*	1	0	1	1	1	1	1	1	1	1			normal
				*	*	1	1	1	1	1	1	1	1	1	1		510/512 × 100%	Totation
				*	*	1	1	1	1	1	1	1	1	1	1		511/512 × 100%	
0	1	0	0	0	0	1	1	1	1	1	1	1 *	1 *	1	1		0V	
0	1	0	0	1	0	0	0	0	0	0	0	*	*	*	*		1/255 × VREE	
				0	1	0	0	0	0	0	0	*	*	*	*		2/255 × VREF	
				0	-	0	0	0	0	0	0	*	*	*	*	1ch hall bias set	2,200	
				1	0	1	1	1	1	1	1	*	*	*	*	(8bit DAC)	253/255 × VREF	
				0	1	1	1	1	1	1	1	*	*	*	*		254/255 × VREF	
				1	1	1	1	1	1	1	1	*	*	*	*		VREF	
1	1	0	0	0	0	0	0	0	0	0	0	*	*	*	*		0V	
				1	0	0	0	0	0	0	0	*	*	*	*		1/255 × VREF	
				0	1	0	0	0	0	0	0	*	*	*	*		2/255 × VREF	
												*	*	*	*	2ch hall bias set		
				1	0	1	1	1	1	1	1	*	*	*	*	(8bit DAC)	253/255 × VREF	
				0	1	1	1	1	1	1	1	*	*	*	*		254/255 × VREF	
				1	1	1	1	1	1	1	1	*	*	*	*		VREF	
0	0	1	0	0	0	0	0	0	0	0	0	*	*	*	*		0V	
				1	0	0	0	0	0	0	0	*	*	*	*		$1/255 \times V_{CC}$	
				0	1	0	0	0	0	0	0	*	*	*	*	1ch hall amplifier	$2/255 \times V_{CC}$	
												*	*	*	*	offset adjustment		
				1	0	1	1	1	1	1	1	*	*	*	*	(8bit DAC)	253/255 × V _{CC}	
				0	1	1	1	1	1	1	1	*	*	*	*		254/255 × V _{CC}	
L				1	1	1	1	1	1	1	1	*	*	*	*		V _{CC}	
1	0	1	0	0	0	0	0	0	0	0	0	*	*	*	*		0V	
				1	0	0	0	0	0	0	0	*	*	*	*		$1/255 \times V_{CC}$	
				0	1	0	0	0	0	0	0	*	*	*	*	2ch hall amplifier	$2/255 \times V_{CC}$	
												*	*	*	*	offset adjustment		
				1	0	1	1	1	1	1	1	*	*	*	*	(8bit DAC)	253/255 × V _{CC}	
				0	1	1	1	1	1	1	1	*	*	*	*		$254/255 \times V_{CC}$	
				1	1	1	1	1	1	1	1	*	*	*	*		V _{CC}	

The PWMh-bridge driver's ON/OFF operation is done with the ST pin.

Hall amplifier gain setting range

Hall amplifier relation serial map

	1	1	Inj	put		1		Setting mode	Hall amplifier magnification
A0	A1	A2	A3	D0	D1	D2	D3	Secting mode	()Inside: Resistance
0	0	0	1	0	0	0	0	1ch hall amplifier gain setting	10 (36k//3.6k)
				1	0	0	0	("3" Resistance ÷ "2"	20 (72k//3.6k)
				0	1	0	0	Resistance)	40 (144k//3.6k)
				1	1	0	0		50 (180k//3.6k)
				0	0	1	0		60 (216k//3.6k)
				1	0	1	0		70 (252k//3.6k)
				0	1	1	0		90 (324k//3.6k)
				1	1	1	0		100 (360k//3.6k)
				0	0	0	1		110 (396k//3.6k)
				1	0	0	1		120 (432k//3.6K)
				0	1	0	1		140 (504k//3.6k)
				1	1	0	1		150 (540k//3.6k)
				0	0	1	1		160 (570k//3.6k)
				1	0	1	1		170 (612k//3.6k)
				0	1	1	1		190 (684k//3.6k)
				1	1	1	1		200 (720k//3.6k)
1	0	0	1	0	0	0	0	2ch hall amplifier gain setting	10 (36k//3.6k)
				1	0	0	0	("3" Resistance ÷ "2"	20 (72k//3.6k)
				0	1	0	0	Resistance)	40 (144k//3.6k)
				1	1	0	0		50 (180k//3.6k)
				0	0	1	0	F	60 (216k//3.6k)
				1	0	1	0	F F	70 (252k//3.6k)
				0	1	1	0		90 (324k//3.6k)
				1	1	1	0		100 (360k//3.6k)
				0	0	0	1		110 (396k//3.6k)
				1	0	0	1	F	120 (432k//3.6K)
				0	1	0	1	F	140 (504k//3.6k)
				1	1	0	1	F	150 (540k//3.6k)
				0	0	1	1	F	160 (570k//3.6k)
				1	0	1	1	F	170 (612k//3.6k)
				0	1	1	1	F	190 (684k//3.6k)
				1	1	1	1	F	200 (720k//3.6k)
0	1	0	1	0	0	0	0	1ch hall amplifier offset	10 (36k//3.6k)
		-		1	0	0	0	resistance / input resistance	20(72k//3.6k)
				0	1	0	0	("1" Resistance ÷ "2"	40 (144k//3.6k)
				1	1	0	0	Resistance)	50 (180k//3.6k)
				0	0	1	0		60 (216k//3.6k)
				1	0	1	0	-	70 (252k//3.6k)
				0	1	1	0	-	90 (324k//3.6k)
				1	1	1	0	-	100 (360k//3.6k)
				0	0	0	1		110 (396k//3 6k)
				1	0	0	1	-	120 (432k//3.6K)
				0	1	0	1	-	140(504k//3.6k)
				1	1	0	1		150(540k//3.6k)
				0	0	1	1		160 (570k//3.6k)
				1	0	1	1		170 (612k//3.6k)
				0	1	1	1		190 (684k//3.6k)
				1	1	1	1		200 (720k//3.6k)
1	1	0	1	0	0	0	0	2ch hall amplifier offset	10 (36k//3.6k)
1		5	1	1	0	0	0	resistance / input resistance	20 (72k//3.6k)
				0	1	0	0	("1" Resistance ÷ "?"	40(144k/3.6k)
				1	1	0	0	Resistance)	50 (180k//3.0K)
				1	0	1	0		50 (100K//3.0K) 60 (216E//2.6E)
				1	0	1	0		70 (250k//3.0K)
				1	1	1	0		10 (232K//3.0K) 00 (2341//2.61-)
				1	1	1	0		90 (324K//3.0K) 100 (2201-//2.cl-)
				1	1	1	1		100 (300K//3.0K)
				1	0	0	1		110 (390K//3.0K)
				1	1	0	1	-	120 (452K//5.0K)
				1	1	0	1	-	140 (504K//3.6K)
				1	1	0	1		150 (540k//3.6k)
				0	0	1	1		160 (570k//3.6k)
				1	0	1	1		1/0 (612k//3.6k)
				0	1	1	1	_	190 (684k//3.6k)
1		1		1	1	1	1		200 (720k//3.6k)

General-purpose amplifier ON/OFF setting

		Inj	put			Catting and to	Satting mode Sat content			
A0	A1	A2	A3	D0	D1	Setting mode	Set content	Remarks		
0	0	1	1	0	*	General-purpose	Stand-by			
				1	*	amplifier 1	Operate			
				*	0	General-purpose	Stand-by			
				*	1	amplifier 2	Operate			

PWM circuit accuracy setting

		Inj	put			Catting made	Cat an utant	Demode
A0	A1	A2	A3	D0	D1	Setting mode	Set content	Remarks
1	0	1	1	0	0		10bit resolution	Initial value
				0	1	DWA	11bit resolution	
				1	0	PWM accuracy setting	12bit resolution	
				*	*		-	

PWM pulse width of moving

1ch (X axis side)

	Input [3:0]							Catting and Is	Moving pulse
A0	A1	A2	A3	D0	D1	D2	D3	Setting mode	number
0	1	1	1	0	0	0	0	1ch (X axis) side width of	0 (Initialization)
				1	0	0	0	moving	1
				0	1	0	0		2
				1	1	0	0		3
				0	0	1	0		4
				1	0	1	0		5
				0	1	1	0		6
				1	1	1	0		7
				0	0	0	1		8
				1	0	0	1		9
				0	1	0	1		10
				1	1	0	1		11
				0	0	1	1		12
				1	0	1	1		13
				0	1	1	1		14
				1	1	1	1		15

Note : 1 pulse = 1CLK

2ch (Y axis side)

	-		Input	[7:4]				Sotting mode	Moving pulse
A0	A1	A2	A3	D4	D5	D6	D7	Setting mode	number
0	1	1	1	0	0	0	0	2ch (Y axis) side width of	0 (Initialization)
				1	0	0	0	moving	1
				0	1	0	0		2
				1	1	0	0		3
				0	0	1	0		4
				1	0	1	0		5
				0	1	1	0		6
				1	1	1	0		7
				0	0	0	1		8
				1	0	0	1		9
				0	1	0	1		10
				1	1	0	1		11
				0	0	1	1		12
				1	0	1	1]	13
				0	1	1	1]	14
				1	1	1	1]	15

Note : 1 pulse = 1CLK

The ON/OFF operation of the hall amplifier and the hall bias is done with the ST pin.

Note : An initial value of A0 to A3 = 1111 is a static test mode. Use it specifying data D0 for one.

TEST mode setting

Input					Catting and to	Contant	Demoder
A0	A1	A2	A3	D0	Setting mode	Content	Remarks
1	1	1	1	0		External CLK	It uses it by the shipment inspection.
				1	NC pin _ TEST mode	Internal CLK	Internal CLK operation

Note : External CLK mode is for the shipment inspection. Use it with internal CLK. Use it after it internal CLK switches because default is external CLK mode.

Hall bias, Offset adjustment circuit configuration



Hall amplifier, Hall bias equivalent circuit

About the gain adjustment

The resistance ratio of "2" and "3" is adjusted in figure and the gain is set. Refer to the setting to the cereal map. The magnification can be set from ten by 200.

About the Offset adjustment

The resistance ratio of "1" and "2" is adjusted in figure and the Offset is set. Refer to the setting to the cereal map. The magnification can be set from ten by 200.

Note in design

• Stand-by function

IC becomes a stand-by state at ST = "L", and IC enters the state of operation at ST = "H". Moreover, the register in IC is reset as for ST = "L" at times.

• Hall bias

The constant current output is built into for the hall element drive. The constant current value is set from detection resistance (RHG) connected from the HBIN pin impression voltage and the HGND pin between GND.

Constant current value (I_{O}) = HBIN voltage ÷ Detection resistance



Constant current value (I_O) becomes about 1mA when assuming HBIN pin impressed voltage =1.0V and detection resistance = $1 k\Omega$ from the above-mentioned calculation type. Moreover, the HGND pin must connect with the HB pin, and connect the detection resistance of a large value as much as possible when you do not use the hall bias circuit.

• Operation amplifier

Impress the bias to the V_{IN+} pin, and compose the buffer by the connection to the VOUT pin in the V_{IN-} pin in the operational amplifier not used.



ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LV8415XA-MH	WLP32L (2.47mm × 2.47mm) (Pb-Free / Halogen Free)	5000 / Tape & Reel

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