JLM158-DIE1

Low power dual operational amplifiers

Wafer form

Features

- Internally frequency compensated
- Large DC voltage gain: 100 dB
- Wide bandwidth (unity gain): 1.1 MHz (temperature compensated)
- Very low supply current per operator essentially independent of supply voltage
- Low input bias current: 20 nA (temperature compensated)
- Low input offset voltage: 2 mV
- Low input offset current: 2 nA
- Input common-mode voltage range includes negative rail
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing 0 V to (V_{CC}^+ - 1.5V)

Description

These circuits consist of two independent, high-gain, internally frequency-compensated op-amps which are designed specifically to operate from a single power supply over a wide range of voltages. The low power supply drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, DC gain blocks and all the conventional op-amp circuits which now can be more easily implemented in single power supply systems. For example, these circuits can be directly supplied with the standard +5 V which is used in logic systems and will easily provide the required interface electronics without requiring any additional power supply.

In linear mode, the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.

1 Schematic diagram

Figure 1. Schematic diagram (1/2 LM158)

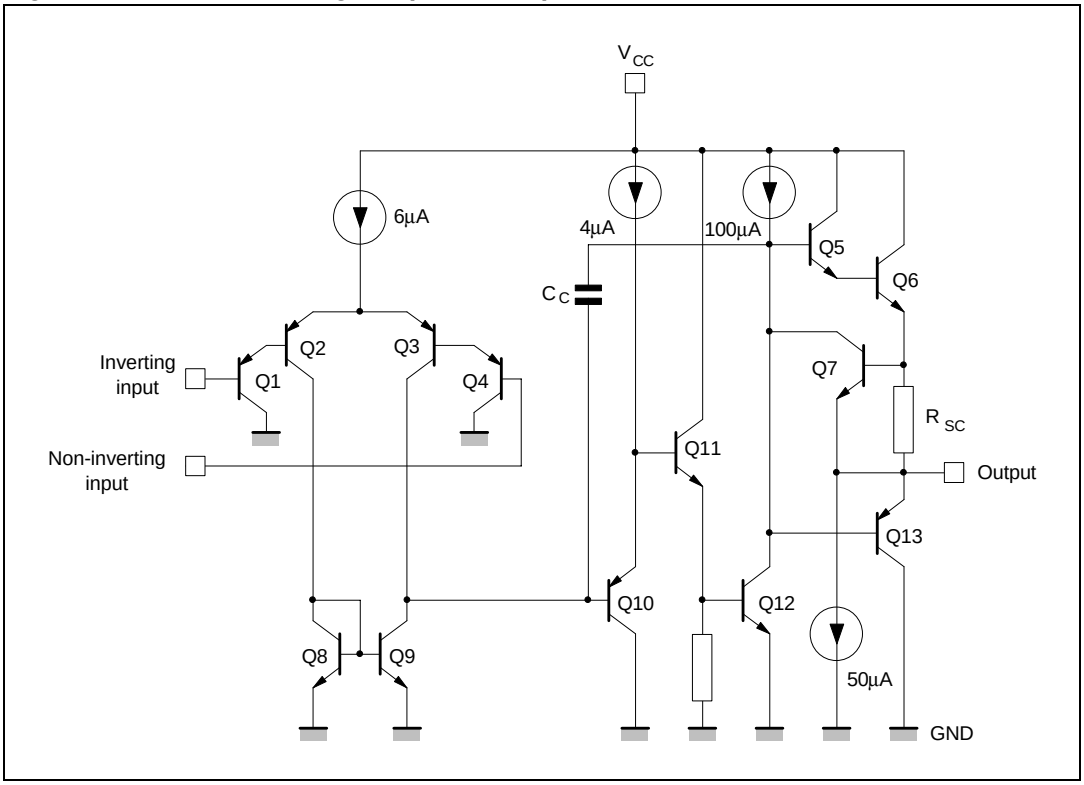
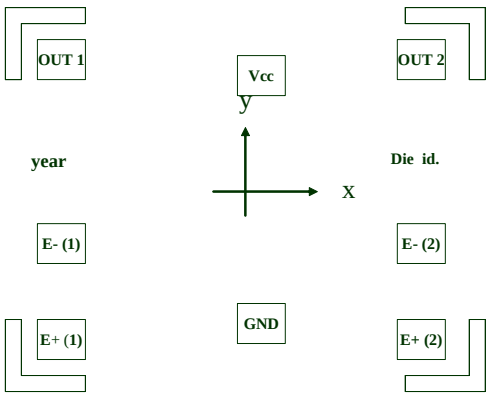


Figure 2. Pad locations



Name	Pad placement		Pad dimensions	
	X	Y	X	Y
GND	0.9	-422.6	81	81
E+1	-445.05	-420.35	76.5	76.5
E-1	-445.05	-170.85	76.5	76.5
OUT1	-445.25	416.75	76.5	76.5
Vcc +	0.9	410.5	81	81
OUT2	445.25	416.75	76.5	76.5
E-2	445.05	-170.85	76.5	76.5
E+2	445.05	-420.35	76.5	76.5

The coordinates origin is at the center of the die.
All dimensions are specified in micrometer (µm).

2 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	+/-16 or 32	V
V_i	Input voltage	32	V
V_{id}	Differential input voltage	32	V
I_{in}	Input current (1)	50	mA
T_{stg}	Storage temperature range	-65 to +150	°C
T_j	Maximum junction temperature	150	°C
ESD	HBM: human body model(2)	300	V
	MM: machine model(3)	200	V
	CDM: charged device model(4)	1.5	kV

1. This input current only exists when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistor becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also NPN parasitic action on the IC chip. This transistor action can cause the output voltages of the Op-amps to go to the V_{CC} voltage level (or to ground for a large overdrive) for the time during which an input is driven negative.
This is not destructive and normal output is restored for input voltages above -0.3 V.
2. Human body model: A 100pF capacitor is charged to the specified voltage, then discharged through a 1.5kΩ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.
3. Machine model: A 200pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5Ω). This is done for all couples of connected pin combinations while the other pins are floating.
4. Charged device model: all pins and the package are charged together to the specified voltage and then discharged directly to the ground through only one pin. This is done for all pins.

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	3 to 30	V
V_{icm}	Common mode input voltage range (1) T_{amb} = +25° C $T_{min} \leq T_{amb} \leq T_{max}$	V_{CC}^- -0.3 to V_{CC}^+ -1.5 V_{CC}^- -0.3 to V_{CC}^+ -2	V
T_{oper}	Operating free-air temperature range	-55 to +125	°C

1. The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is V_{CC}^+ - 1.5 V, but either or both inputs can go to +32 V without damage.

3 Electrical characteristics

Table 3. V_{CC}^+ = +5V, V_{CC}^- = Ground, V_o = 1.4V, T_{amb} = +25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage (1) $T_{min} \le T_{amb} \le T_{max}$		2	5 7	mV
DV_{io}	Input offset voltage drift		7	30	µV/°C
I_{io}	Input offset current $T_{min} \le T_{amb} \le T_{max}$		2	30 40	nA
DI_{io}	Input offset current drift		10	300	pA/°C
I_{ib}	Input bias current (2) $T_{min} \le T_{amb} \le T_{max}$		20	150 200	nA
A_{vd}	Large signal voltage gain V_{CC}^+ = +15V, R_L = 2kΩ, V_o = 1.4V to 11.4V $T_{min} \le T_{amb} \le T_{max}$	50 25	100		V/mV
SVR	Supply voltage rejection ratio ($R_s \le 10$ kΩ) V_{CC}^+ = 5V to 30V $T_{min} \le T_{amb} \le T_{max}$	65 65	100		dB
I_{CC}	Supply current, all amp, no load $T_{min} \le T_{amb} \le T_{max}$ V_{CC}^+ = +5V $T_{min} \le T_{amb} \le T_{max}$ V_{CC}^+ = +30V		0.7	1.2 2	mA
CMR	Common mode rejection ratio ($R_s \le 10$ kΩ) $T_{min} \le T_{amb} \le T_{max}$	70 60	85		dB
I_{source}	Output current source V_{CC}^+ = +15V, V_o = +2V, V_{id} = +1V	20	40	60	mA
I_{sink}	Output sink current (V_{id} = -1V) V_{CC}^+ = +15V, V_o = +2V V_{CC}^+ = +15V, V_o = +0.2V	 10 12	 20		 mA µA
V_{OH}	High level output voltage (V_{CC}^+ = 30V) R_L = 2kΩ $T_{min} \le T_{amb} \le T_{max}$ R_L = 10kΩ $T_{min} \le T_{amb} \le T_{max}$	 26 26 27 27	 27 28		V
V_{OL}	Low level output voltage (R_L = 10 kΩ) $T_{min} \le T_{amb} \le T_{max}$		5	20 20	mV
SR	Slew rate V_{CC}^+ = 15V, V_i = 0.5 to 3V, R_L = 2kΩ, C_L = 100pF, unity gain	 0.3	 0.6		V/µs
GBP	Gain bandwidth product V_{CC}^+ = 30V, f = 100kHz, V_{in} = 10mV, R_L = 2kΩ, C_L = 100pF	0.7	1.1		MHz

Table 3. V_{CC}^+ = +5V, V_{CC}^- = Ground, V_o = 1.4V, T_{amb} = +25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
THD	Total harmonic distortion f = 1kHz, A_v = 20dB, R_L = 2kΩ, V_o = $2V_{pp}$, C_L = 100pF, V_o = $2V_{pp}$		0.02		%
e_n	Equivalent input noise voltage f = 1kHz, R_s = 100Ω, V_{CC}^+ = 30V		55		$\frac{nV}{\sqrt{Hz}}$
V_{o1}/V_{o2}	Channel separation(3) 1kHz ≤ f ≤ 20kHz		120		dB

1. V_o = 1.4 V, R_s = 0 Ω, 5 V < V_{CC}^+ < 30 V, 0 < V_{ic} < V_{CC}^+ - 1.5 V
2. The direction of the input current is out of the IC. This current is essentially constant, independent of the state of the output so there is no change in the load on the input lines.
3. Due to the proximity of external components, ensure that stray capacitance between these external parts does not cause coupling. Typically, this can be detected because this type of capacitance increases at higher frequencies.

Figure 3. Open loop frequency response

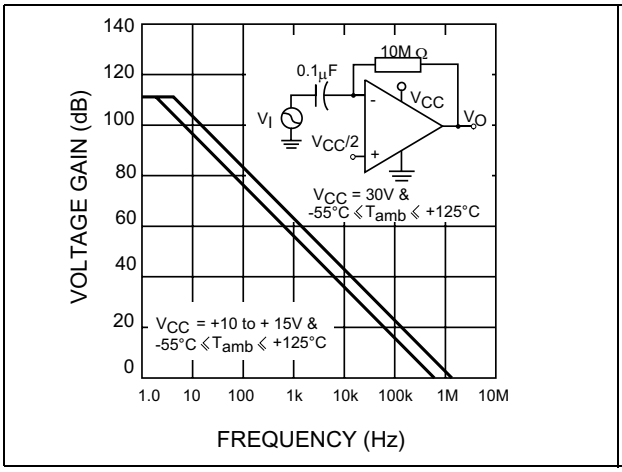


Figure 4. Large signal frequency response

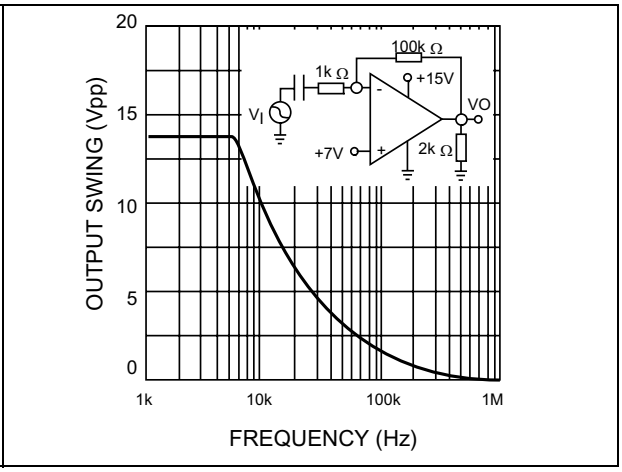


Figure 5. Voltage follower pulse response

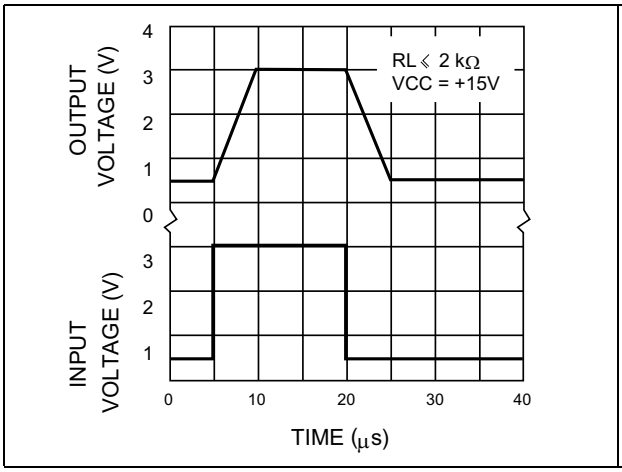


Figure 6. Voltage follower pulse response

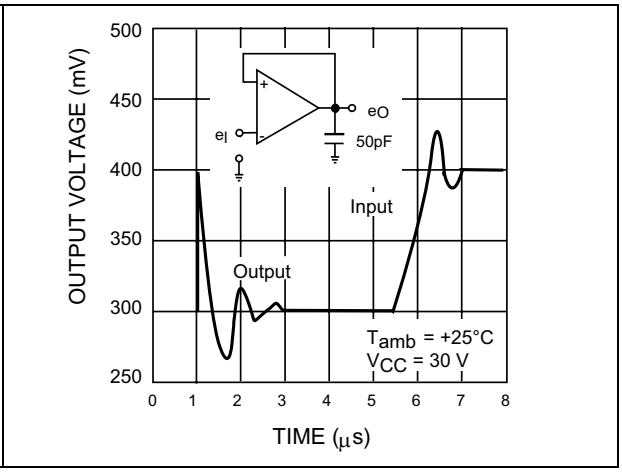


Figure 7. Input current

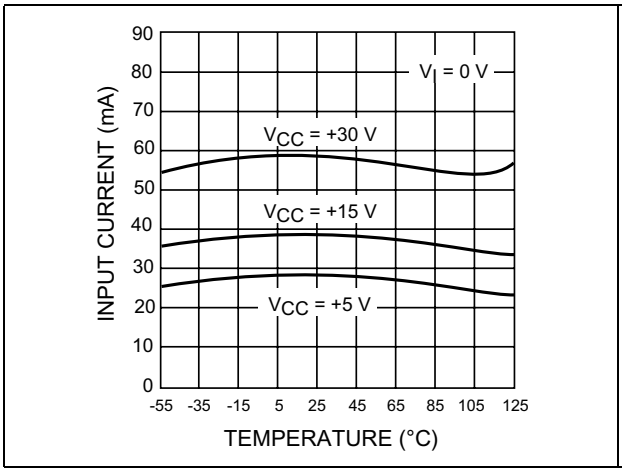


Figure 8. Output characteristics

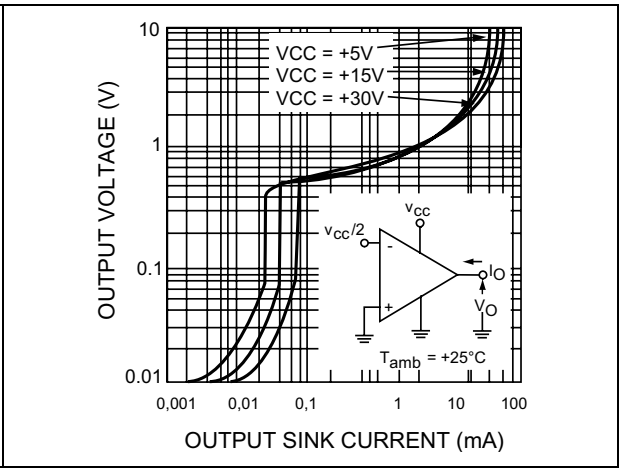


Figure 9. Output characteristics

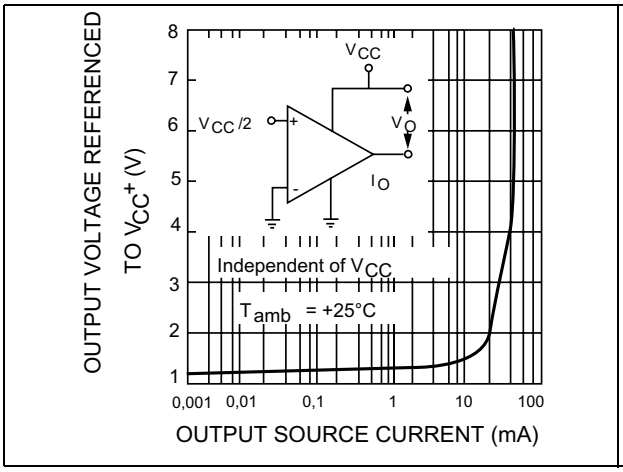


Figure 10. Current limiting

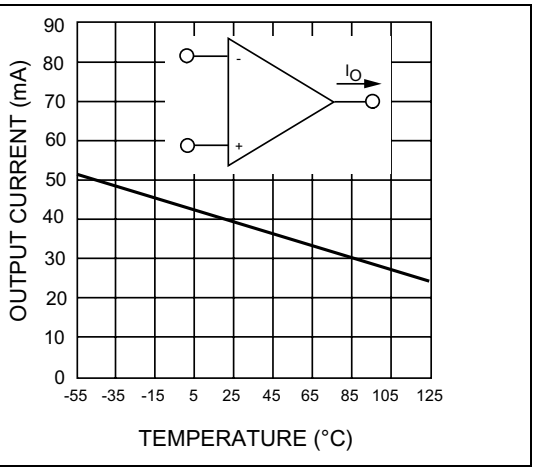


Figure 11. Input voltage range

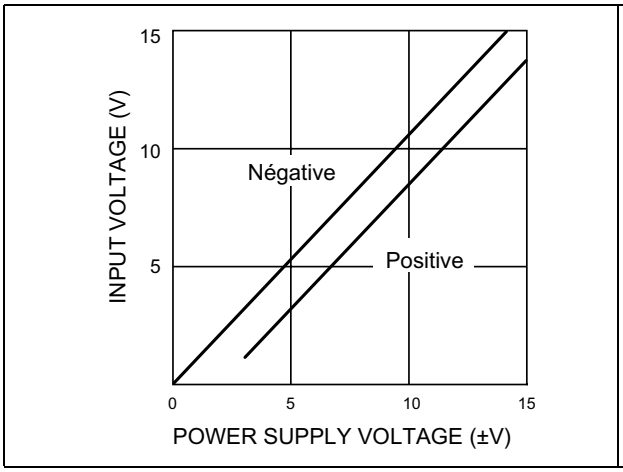


Figure 12. Positive supply voltage

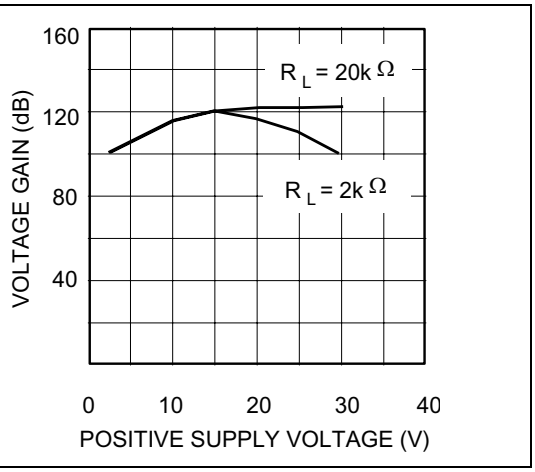


Figure 13. Input voltage range

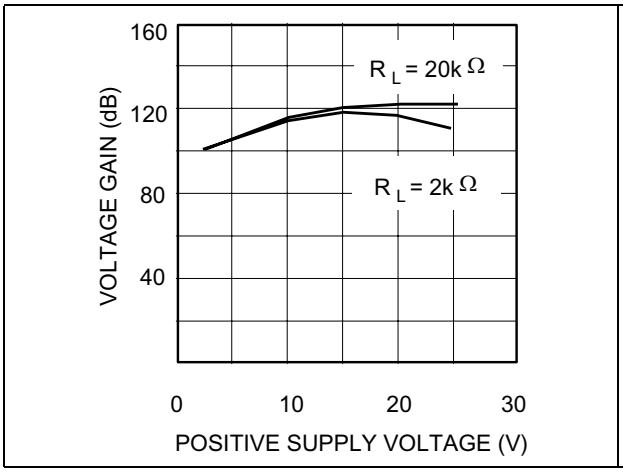


Figure 14. Supply current

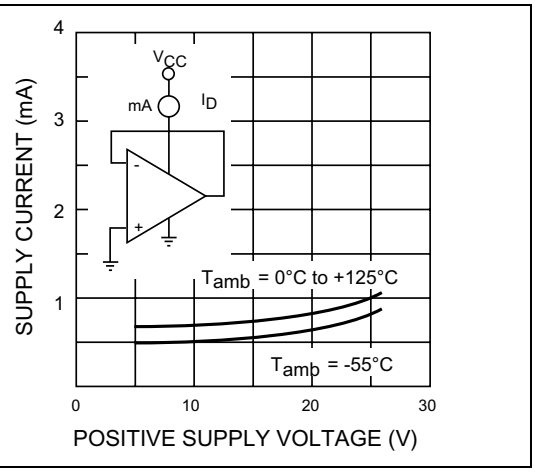


Figure 15. Input current

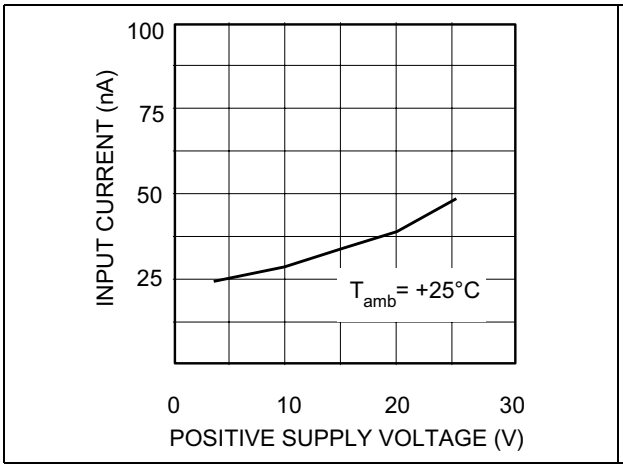


Figure 16. Gain bandwidth product

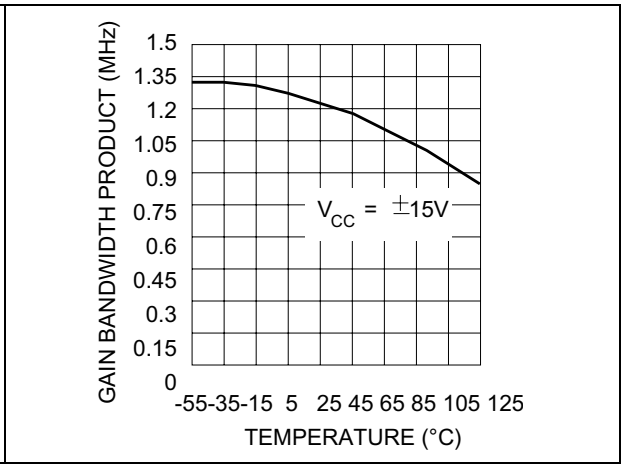


Figure 17. Power supply rejection ratio

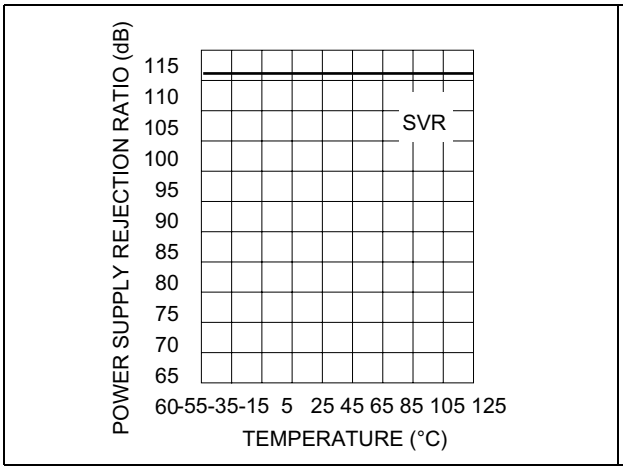


Figure 18. Common mode rejection ratio

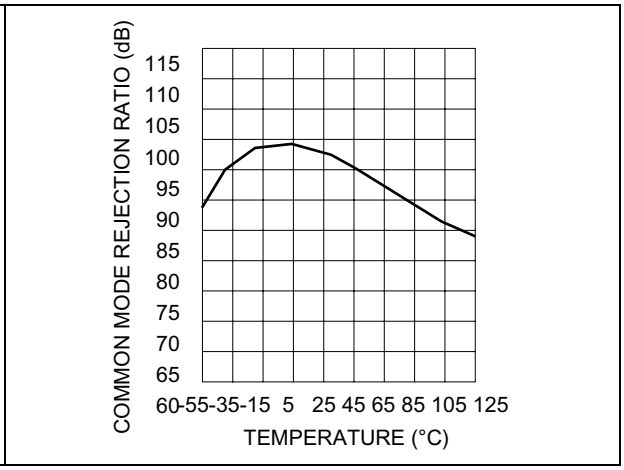
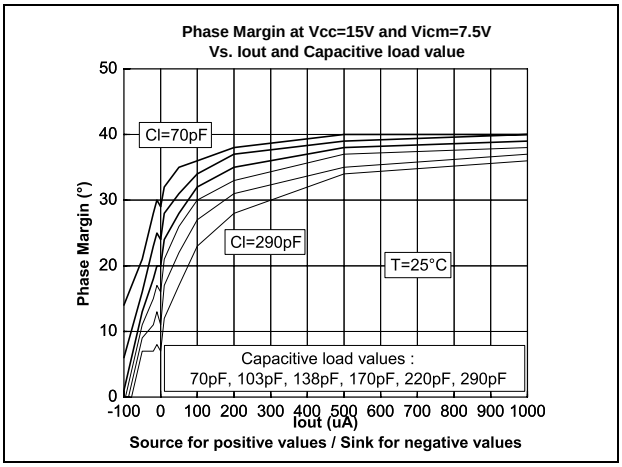


Figure 19. Phase margin vs capacitive load



4 Ordering information

Table 4. Order code

Order code	Temperature range	Package	Packaging
JLM158-die1	-55°C to +125°C	wafer	D4 (1)

1. Wafer tested, inked, cut on sticky foil (cardboard ring).

5 Revision history

Table 5. Document revision history

Date	Revision	Changes
18-Dec-2007	1	Initial release.

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