NCP10670B, NCP10671B, NCP10672B

High-Voltage Switcher for Low Power Offline SMPS

The NCP1067X products integrate a fixed frequency current mode controller with a 700 V MOSFET. Available in a SOIC−7 package, the NCP1067X offer a high level of integration, including soft−start, frequency−jittering, short−circuit protection, skip−cycle, ramp compensation, and a Dynamic Self−Supply (eliminating the need for an auxiliary winding).

During nominal load operation, the NCP1067X switches at one of the available frequencies (60 or 100 kHz). When the output power demand diminishes, the IC automatically enters into a skip mode to reduce the standby consumption down.

Protection features include: a timer to detect an overload or a short−circuit event, Overvoltage Protection with auto−recovery.

For improved standby performance, the connection of an auxiliary winding or supplying the IC from the output, stops the DSS operation and helps to reduce input power consumption below 25 mW at high line.

NCP1067x can be seamlessly used both in non−isolated and in isolated topologies.

Features

- Built−in 700 V MOSFET with $R_{DS(on)}$ of 34 Ω (NCP10670/1) and 12 Ω (NCP10672)
- Large Creepage Distance Between High−Voltage Pins
- Current−Mode Fixed Frequency Operation – 60 or 100 kHz
- Fixed Ramp Compensation
- Direct Feedback Connection for Non−isolated Converter
- Skip−Cycle Operation at Low Peak Currents Only
- Dynamic Self−Supply: No Need for an Auxiliary Winding
- Internal 4 ms Soft−Start
- Auto−Recovery Output Short Circuit Protection with Timer−Based Detection
- Auto−Recovery Overvoltage Protection with Auxiliary Winding Operation
- Frequency Jittering for Better EMI Signature
- No Load Input Consumption < 25 mW
- These Devices are Pb−Free and are RoHS Compliant

Applications

- Auxiliary / Standby Isolated and Non−Isolated Power Supplies
- Power Meter SMPS
- Wide Vin Low Power Industrial SMPS

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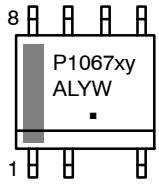
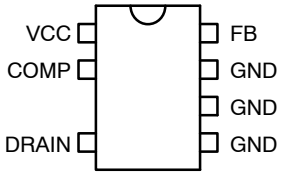
SOIC8
CASE 751EV

MARKING DIAGRAM



P1067	= Specific Device Code
x	= Current Limit (0, 1, 2)
y	= Frequency (060, 100)
A	= Assembly Location
L	= Wafer Lot
Y	= Year
▪	= Pb−Free Package

PIN CONNECTION



SOIC−7

ORDERING INFORMATION

See detailed ordering and shipping information on page 23 of this data sheet.

Table 1. PRODUCTS INFOS & INDICATIVE MAXIMUM OUTPUT POWER

Product	$R_{DS(on)}$	$I_{IPK(0)}$	230 Vac ±15%		85 – 265 Vac	
			Adapter	OpenFrame	Adapter	OpenFrame
NCP10670 60 kHz	34 Ω	100 mA	1.1 W	2.7 W	0.6 W	1.5 W
NCP10671 60 kHz	34 Ω	250 mA	2.7 W	6.7 W	1.5 W	3.7 W
NCP10672 100 kHz	12 Ω	780 mA	6.2 W	15.5 W	3.3 W	7.8 W

1. Informative values only, with T_{amb} = 25°C, T_{case} = 100°C, Self supply via Auxiliary winding and circuit mounted on minimum copper area as recommended.

Table 2. SELECTION TABLE

Device	Frequency	$R_{DS(on)}$	$I_{IPK(0)}$	Package Type
NCP10670	60 kHz	34	100 mA	SOIC−7 (Pb−Free)
NCP10670	100 kHz	34	100 mA	
NCP10671	60 kHz	34	250 mA	
NCP10671	100 kHz	34	250 mA	
NCP10672	60 kHz	12	780 mA	
NCP10672	100 kHz	12	780 mA	

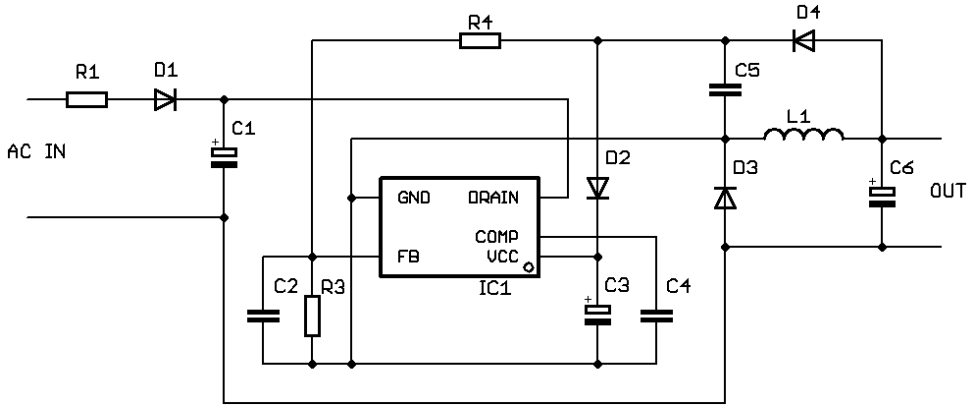


Figure 1. Typical Non−Isolated Application (Buck Converter)

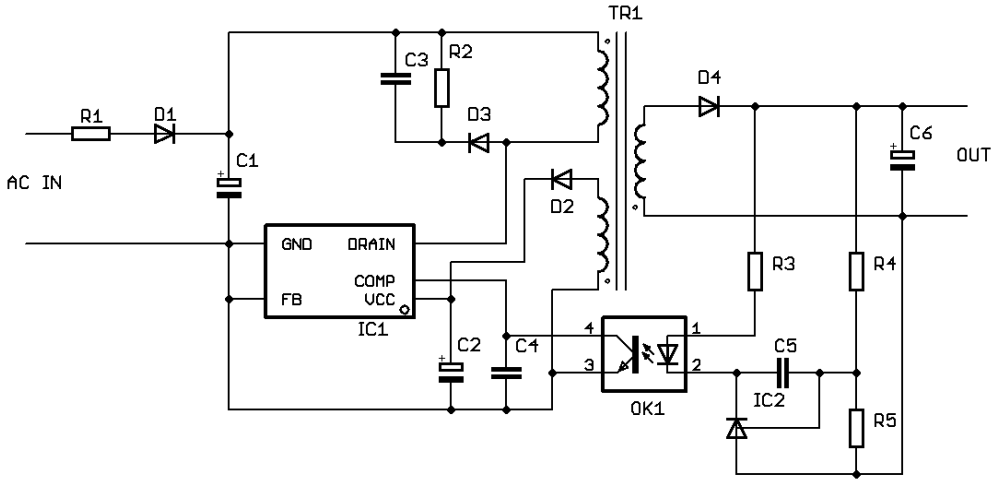


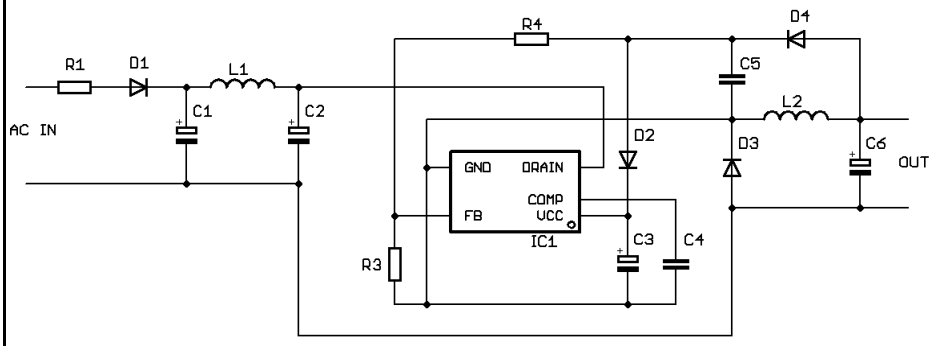
Figure 2. Typical Isolated Application (Flyback Converter)

PIN DESCRIPTION

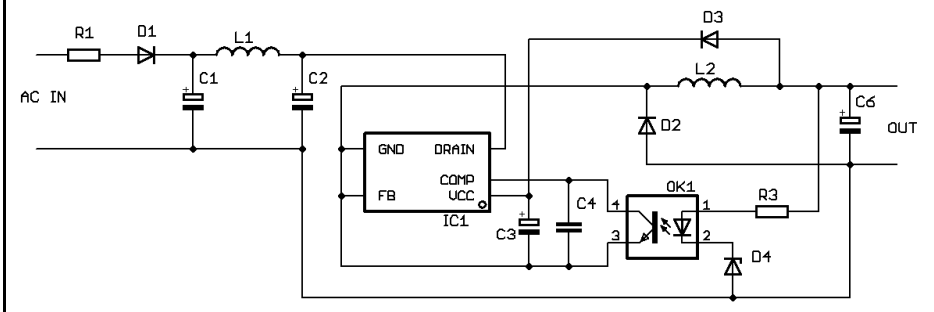
Pin No. SOIC−7	Name	Function	Description
1	V_{CC}	Powers the internal circuitry	This pin is connected to an external capacitor. The V_{CC} includes an auto−recovery over voltage protection.
2	Comp	Compensation	The error amplifier output is available on this pin. The network connected between this pin and ground adjusts the regulation loop bandwidth. Also, by connecting an opto−coupler to this pin, the peak current set point is adjusted accordingly to the output power demand.
3			This missing pin ensures adequate creepage distance
4	Drain	Drain connection	The internal drain MOSFET connection
5−7	GND	The IC Ground	
8	FB	Feedback signal input	This is the inverting input of the trans conductance error amplifier. It is normally connected to the switching power supply output through a resistor divider.

Table 3. TYPICAL APPLICATION

Non Isolated Buck

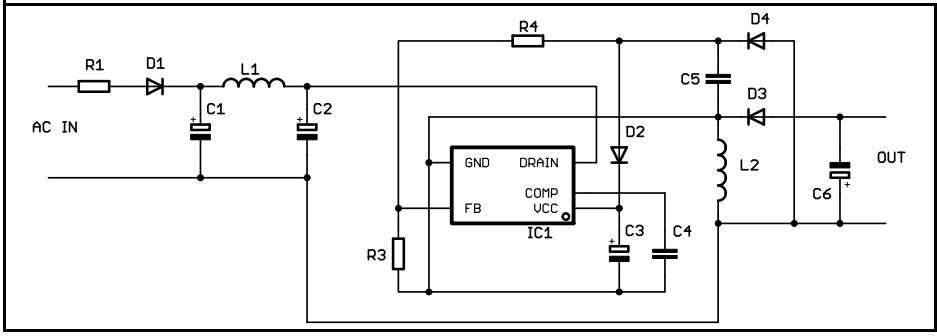


- If the output voltage is above 9.0 V typ. (between $V_{CC(on)}$ level and V_{OVP} level) VCC is supplied from output via D2
- If the output voltage is below 9.0 V, D2 is redundant, the IC is supplied from DSS
- Direct feedback, resistive divider formed by R3, R4 sets output voltage



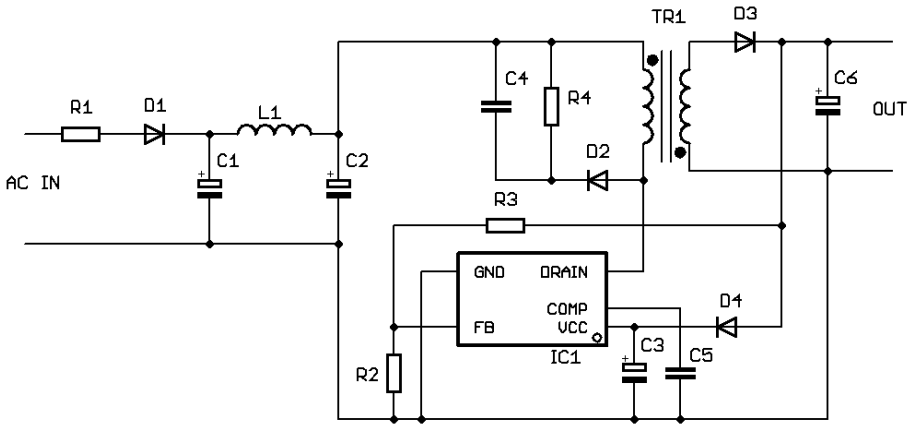
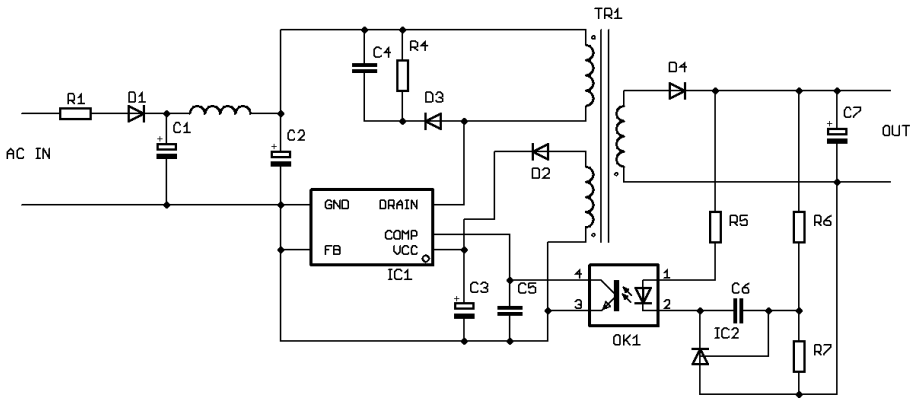
- If the output voltage is above 9.0 V typ. (between $V_{CC(on)}$ level and V_{OVP} level) VCC is supplied from output via D3
- If the output voltage is below 9.0 V, D3 is redundant, the IC is supplied from DSS
- Optocoupler feedback, output voltage is set by D4

Non Isolated Buck−Boost (Invert)



- If the output voltage is above 9.0 V typ. between $V_{CC(on)}$ level and V_{OVP} level, VCC is supplied from output via D2
- If the output voltage is below 9.0 V, D2 is redundant, the IC is supplied from DSS
- Direct feedback, resistive divider formed by R3, R4 sets output voltage

Table 3. TYPICAL APPLICATION

Non Isolated Flyback	
	• If the output voltage is above 9.0 V typ. between $V_{CC(on)}$ level and V_{OVP} level –VCC supplied from output via D4 • If the output voltage is below 9.0 V, D4 is redundant, the IC is supplied from DSS • Resistive divider formed by R2, R3 sets output voltage
Isolated Flyback	
	• VCC supplied from auxiliary winding • Optocoupler feedback, resistive divider formed by R6, R7 sets output voltage

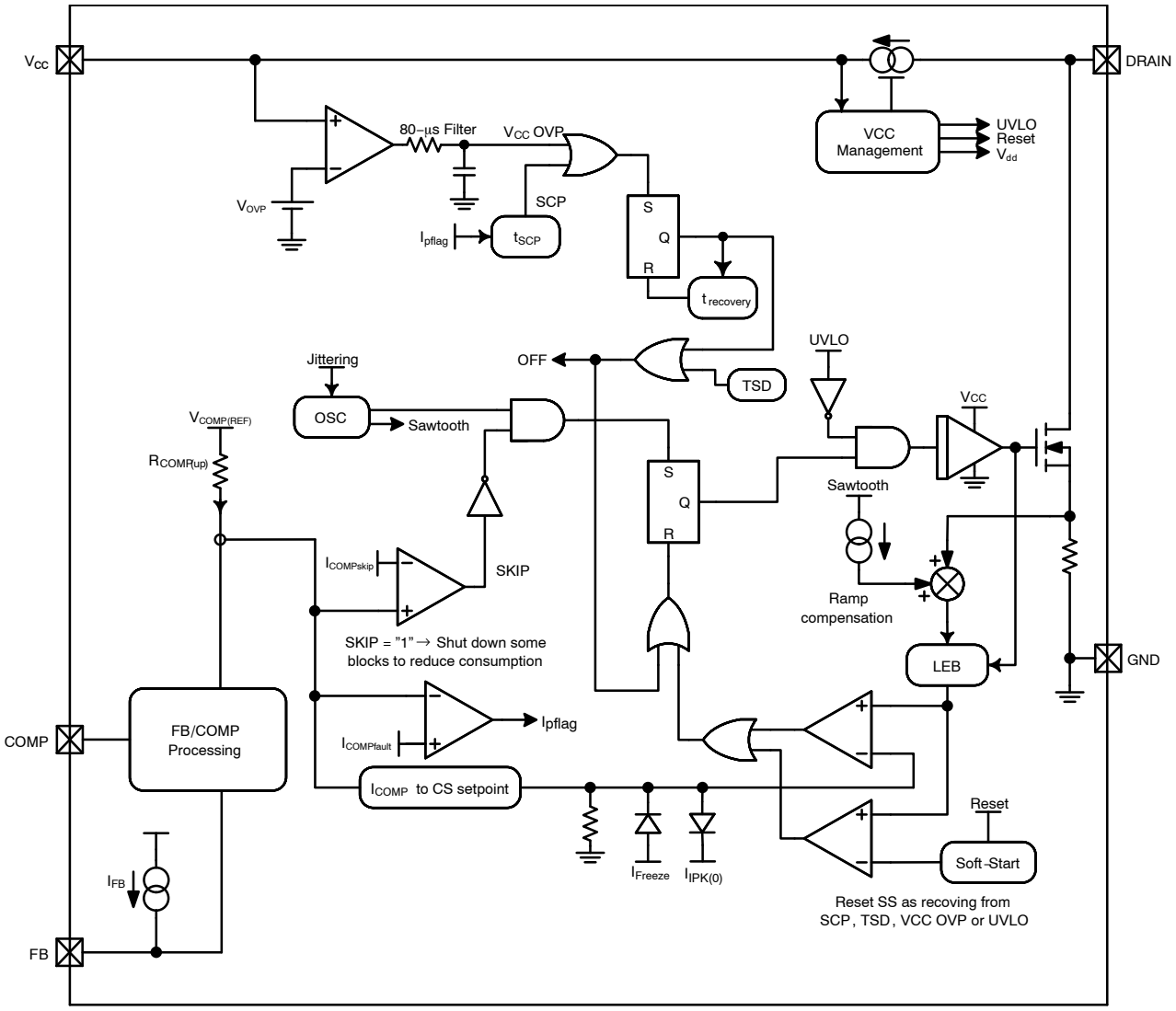


Figure 3. Simplified Internal Circuit Architecture

MAXIMUM RATINGS (All voltages related to GND terminal)

Symbol	Parameter	Rating	Units
V_{CC}	Power supply voltage, V_{CC} pin, continuous voltage	−0.3 to 20	V
Vinmax	Voltage on all pins, except Drain and V_{CC} pin	−0.3 to 10	V
BVdss	Drain voltage	−0.3 to 700	V
I_{CC}	Maximum Current into V_{CC} pin	10	mA
$I_{DS(PK)}$	Drain Current Peak during Transformer Saturation (T_J = 150°C): NCP10670 NCP10671 NCP10672 Drain Current Peak during Transformer Saturation (T_J = 125°C): NCP10670 NCP10671 NCP10672 Drain Current Peak during Transformer Saturation (T_J = 25°C): NCP10670 NCP10671 NCP10672	 300 300 850 335 335 950 520 520 1500	 mA mA mA mA mA mA mA mA mA
$R_{\theta J-A}$	Thermal Resistance Junction−to−Air − NCP10670(1) SOIC7 with 200 mm^2 of 35−μ copper area	116	°C/W
$R_{\theta J-A}$	Thermal Resistance Junction−to−Air − NCP10672 SOIC7 with 200 mm^2 of 35−μ copper area	102	°C/W
T_{JMAX}	Maximum Junction Temperature	150	°C
	Storage Temperature Range	−60 to +150	°C
HBM	Human Body Model ESD Capability per JEDEC JESD22−A114F	2	kV
CDM	Charged−Device Model ESD Capability per JEDEC JESD22−C101E	1	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. This device contains latch−up protection and exceeds 100 mA per JEDEC Standard JESD78.

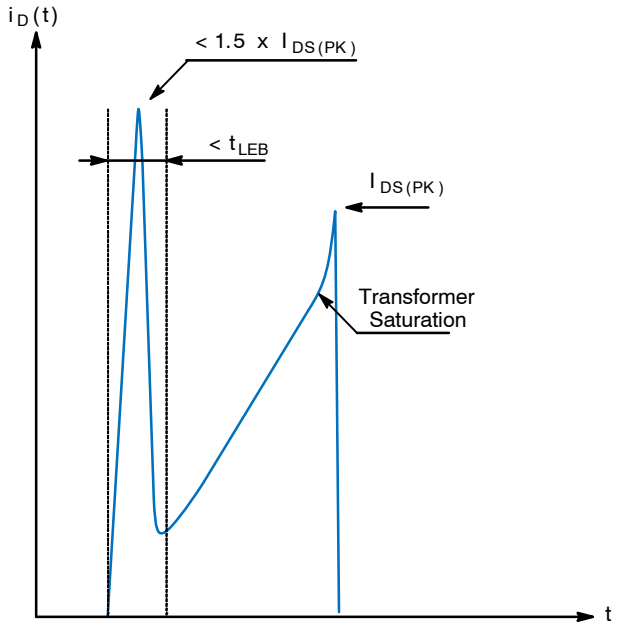


Figure 4. Spike Limits

ELECTRICAL CHARACTERISTICS

(Tj = 25°C, for min/max values Tj = −40°C to +125°C, Vcc = 14 V unless otherwise noted)

Symbol	Rating	Pin	Min	Typ	Max	Unit
SUPPLY SECTION AND V_{CC} MANAGEMENT						
$V_{CC(on)}$	V_{CC} increasing level at which the switcher starts operation	1	8.4	9.0	9.5	V
$V_{CC(min)}$	V_{CC} decreasing level at which the HV current source restarts	1	7.0	7.5	7.8	V
$V_{CC(off)}$	V_{CC} decreasing level at which the switcher stops operation (UVLO)	1	6.7	7.0	7.2	V
I_{CC1}	Internal IC consumption, NCP10670 switching at 60 kHz Internal IC consumption, NCP10670 switching at 100 kHz Internal IC consumption, NCP10671 switching at 60 kHz Internal IC consumption, NCP10671 switching at 100 kHz Internal IC consumption, NCP10672 switching at 60 kHz Internal IC consumption, NCP10672 switching at 100 kHz	1	– – – – – –	0.84 0.88 0.84 0.88 0.91 1.00	1.05 1.10 1.05 1.10 1.15 1.25	mA
I_{CCskip}	Internal IC consumption, COMP is 0 V (No switching on MOSFET)	1	–	340	–	μA
POWER SWITCH CIRCUIT						
$R_{DS(on)}$	Power Switch Circuit on−state resistance NCP10670, NCP10671 (Id = 50 mA) Tj = 25°C Tj = 125°C NCP10672 (Id = 50 mA) Tj = 25°C Tj = 125°C	4	 – – – –	 34 65 12 22	 41 72 14 24	 Ω Ω Ω Ω
BV_{DSS}	Power Switch Circuit & Startup breakdown voltage ($ID_{(off)}$ = 120 μA, Tj = 25°C)	4	700	–	–	V
$I_{DSS(off)}$	Power Switch & Startup breakdown voltage off−state leakage current Tj = 125°C (Vds = 700 V) Tj = 25°C (Vds = 700 V)	4	 – –	 7 1	 – –	 μA μA
t_r t_f	Switching characteristics (R_L = 50 Ω, V_{DS} set for I_{drain} = 0.7 x Ilim) Turn−on time (90% − 10%) Turn−off time (10% − 90%)	4	 – –	 20 10	 – –	 ns ns
$t_{on(min)}$	Minimum on time NCP10670 NCP10671 NCP10672	4	 – – –	 200 200 230	 – – –	 ns ns ns
INTERNAL START−UP CURRENT SOURCE						
I_{start1}	High−voltage current source, V_{CC} = $V_{CC(on)}$ − 200 mV	4	4	8	12	mA
I_{start2}	High−voltage current source, V_{CC} = 0 V	4	–	0.4	–	mA
V_{CCTH}	VCC Transient level for Istart1 to Istart2 toggling point	1	–	1.2	–	V
$V_{start(min)}$	Minimum startup voltage, V_{CC} = 0 V	4	–	–	22	V
CURRENT COMPARATOR						
I_{IPK}	Maximum internal current setpoint at 50% duty cycle FB = 2 V, Tj = 25°C NCP10670 NCP10671 NCP10672	 – – –	 – – –	 83 208 650	 – – –	 mA mA mA
$I_{IPK(0)}$	Maximum internal current setpoint at beginning of switching cycle FB = 2 V, Tj = 25°C NCP10670 NCP10671 NCP10672	 – – –	 85 223 702	 100 250 780	 115 277 858	 mA mA mA
I_{IPKSW}	Final switch current with a primary slope of 200 mA/μs, F_{SW} = 60 kHz (Note 3) NCP10670 NCP10671 NCP10672	 – – –	 – – –	 120 258 740	 – – –	 mA mA mA

ELECTRICAL CHARACTERISTICS

(Tj = 25°C, for min/max values Tj = −40°C to +125°C, Vcc = 14 V unless otherwise noted) (continued)

Symbol	Rating	Pin	Min	Typ	Max	Unit
CURRENT COMPARATOR						
I_{IPKSW}	Final switch current with a primary slope of 200 mA/μs, F_{SW} = 100 kHz (Note 3) NCP10670 NCP10671 NCP10672		 – – –	 120 250 710	 – – –	 mA mA mA
t_{SS}	Soft−start duration (guaranteed by design)	–	–	4	–	ms
t_{prop}	Propagation delay from current detection to drain OFF state	–	–	70	–	ns
t_{LEB}	Leading Edge Blanking Duration NCP10670 NCP10671 NCP10672	 – – –	 – – –	 130 130 160	 – – –	 ns ns ns
INTERNAL OSCILLATOR						
f_{OSC}	Oscillation frequency, 60 kHz version, Tj = 25°C (Note 4)	–	54	60	66	kHz
f_{OSC}	Oscillation frequency, 100 kHz version, Tj = 25°C (Note 4)	–	90	100	110	kHz
f_{jitter}	Frequency jittering in percentage of f_{OSC}	–	–	±6	–	%
f_{swing}	Jittering swing frequency	–	–	300	–	Hz
D_{max}	Maximum duty−cycle	–	62	66	72	%
ERROR AMPLIFIER SECTION						
V_{REF}	Voltage Feedback Input (V_{COMP} = 2.5 V)	8	3.2	3.3	3.4	V
I_{FB}	Input Bias Current (V_{FB} = 3.3 V)	8	–	1	–	μA
G_M	Transconductance	2	–	2	–	mS
I_{OTAlim}	OTA maximum current capability (V_{FB} > V_{OTAen})	2	–	+150/−150	–	μA
V_{OTAen}	FB voltage to disable OTA	8	0.7	1.3	1.7	V
COMPENSATION SECTION						
$I_{COMPfault}$	COMP current for which Fault is detected	2	–	−40	–	μA
$I_{COMP100\%}$	COMP current for which internal current set−point is 100% ($I_{IPK(0)}$)	2	–	−44	–	μA
$I_{COMPfreeze}$	COMP current for which internal current set−point is: $I_{Freeze1,\ 2\ or\ 3}$ (NCP10670/1/2)	2	–	−80	–	μA
$V_{COMP(REF)}$	Equivalent pull−up voltage in linear regulation range (Guaranteed by design)	2	–	2.7	–	V
$R_{COMP(up)}$	Equivalent feedback resistor in linear regulation range (Guaranteed by design)	2	–	17.7	–	kΩ
SKIP CYCLE						
$I_{COMPskip}$	The COMP pin current level to enter skip mode	2	–	−120	–	μA
$I_{Freeze1}$	Internal minimum current setpoint (I_{COMP} = $I_{COMPFreeze}$) in NCP10670	–	–	35	–	mA
$I_{Freeze2}$	Internal minimum current setpoint (I_{COMP} = $I_{COMPFreeze}$) in NCP10671	–	–	92	–	mA
$I_{Freeze3}$	Internal minimum current setpoint (I_{COMP} = $I_{COMPFreeze}$) in NCP10672	–	–	270	–	mA
RAMP COMPENSATION						
$S_{a(60)}$	The internal ramp compensation @ 60 kHz: NCP10670 NCP10671 NCP10672	 – – –	 – – –	 2.8 8.4 15.6	 – – –	 mA/μs mA/μs mA/μs
$S_{a(100)}$	The internal ramp compensation @ 100 kHz: NCP10670 NCP10671 NCP10672	 – – –	 – – –	 4.7 14 26	 – – –	 mA/μs mA/μs mA/μs

ELECTRICAL CHARACTERISTICS

(Tj = 25°C, for min/max values Tj = −40°C to +125°C, Vcc = 14 V unless otherwise noted) (continued)

Symbol	Rating	Pin	Min	Typ	Max	Unit
PROTECTIONS						
t_{SCP}	Fault validation further to error flag assertion	–	35	48	–	ms
$t_{recovery}$	OFF phase in fault mode	–	–	400	–	ms
V_{OVP}	V_{CC} voltage at which the switcher stops pulsing	1	17.0	18.0	18.8	V
t_{OVP}	The filter of V_{CC} OVP comparator	–	–	80	–	μs
TEMPERATURE MANAGEMENT						
TSD	Temperature shutdown (Guaranteed by design)	–	150	163	–	°C
TSD_{HYST}	Hysteresis in shutdown (Guaranteed by design)	–	–	20	–	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. The final switch current is: $I_{IPK(0)}$ / ($V_{in}/L_P + S_a$) x $V_{in}/L_P + V_{in}/L_P$ x t_{prop}, with S_a the built−in slope compensation, Vin the input voltage, L_P the primary inductor in a flyback, and t_{prop} the propagation delay..
4. Oscillator frequency is measured with disabled jittering.

TYPICAL CHARACTERISTICS

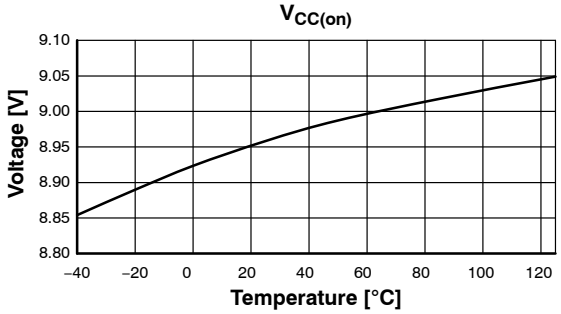


Figure 5. $V_{CC(on)}$ vs. Temperature

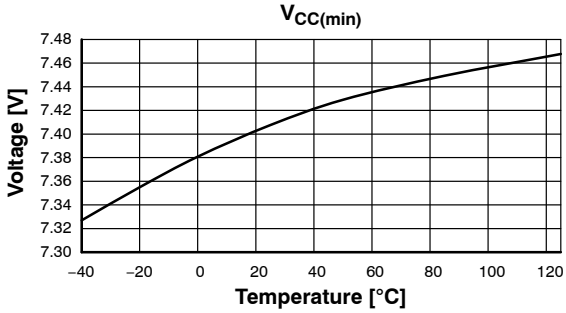


Figure 6. $V_{CC(min)}$ vs. Temperature

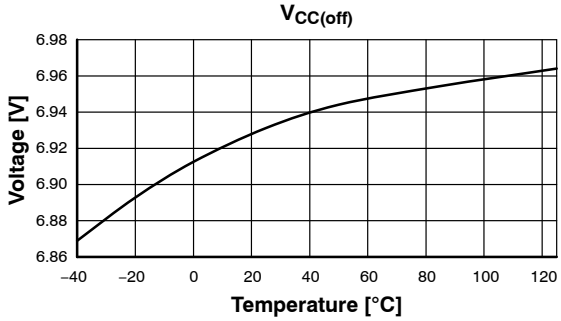


Figure 7. $V_{CC(off)}$ vs. Temperature

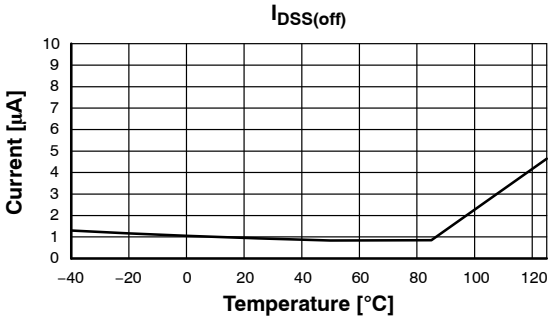


Figure 8. $I_{DSS(off)}$ vs. Temperature

TYPICAL CHARACTERISTICS (continued)

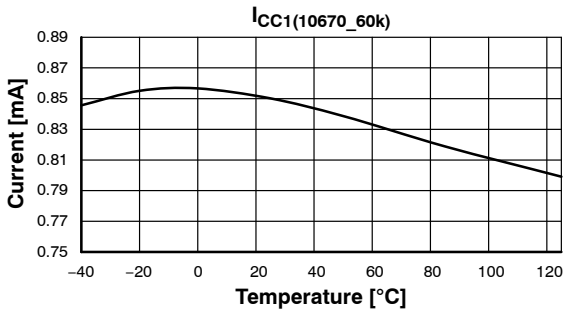


Figure 9. $I_{CC1\ (10670\_60k)}$ vs. Temperature

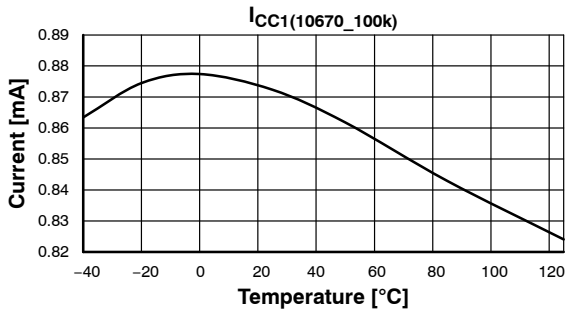


Figure 10. $I_{CC1\ (NCP10670\_100k)}$ vs. Temperature

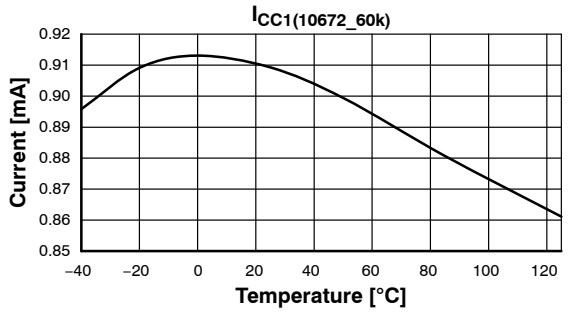


Figure 11. $I_{CC1\ (10672\_60k)}$ vs. Temperature

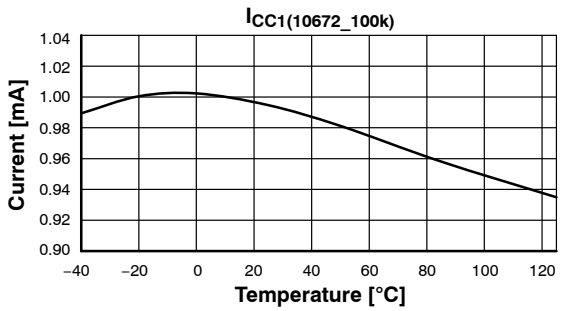


Figure 12. $I_{CC1\ (10672\_100k)}$ vs. Temperature

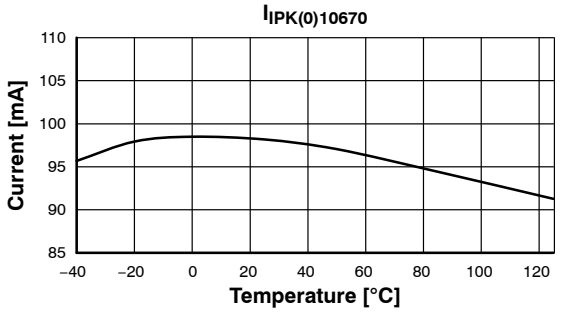


Figure 13. $I_{IPK(0)10670}$ vs. Temperature

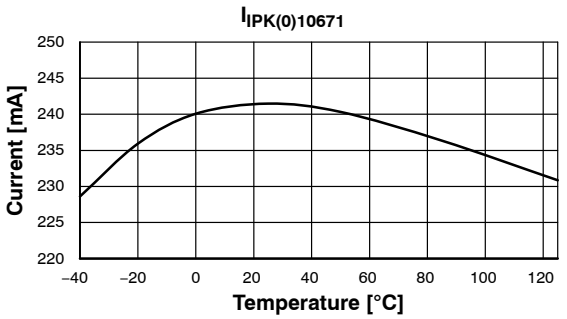


Figure 14. $I_{IPK(0)10671}$ vs. Temperature

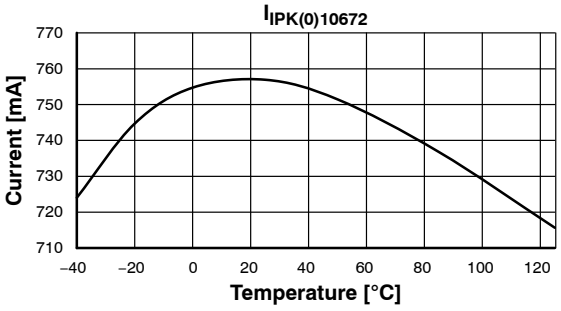


Figure 15. $I_{IPK(0)10672}$ vs. Temperature

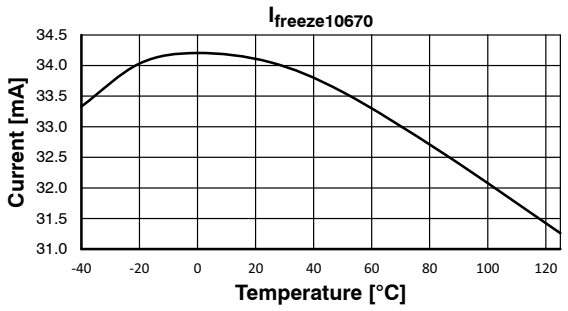


Figure 16. $I_{freeze10670}$ vs. Temperature

TYPICAL CHARACTERISTICS (continued)

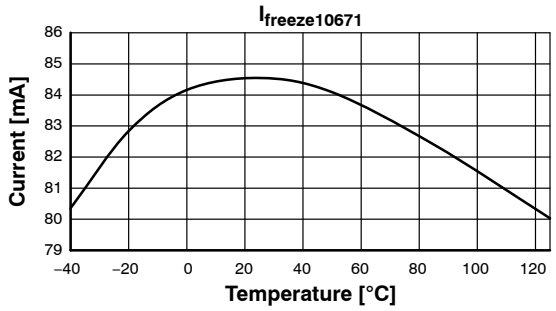


Figure 17. $I_{freeze10671}$ vs. Temperature

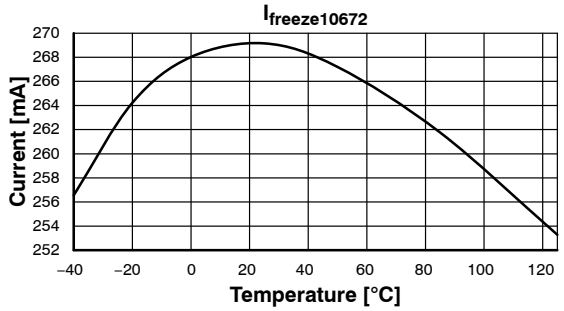


Figure 18. $I_{freeze10672}$ vs. Temperature

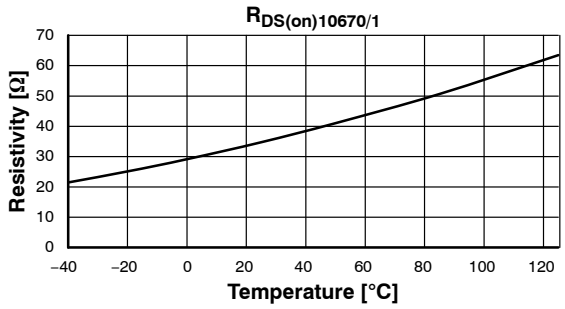


Figure 19. $R_{DS(on)10670/1}$ vs. Temperature

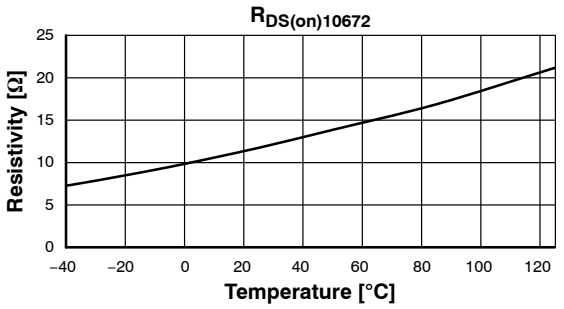


Figure 20. $R_{DS(on)10672}$ vs. Temperature

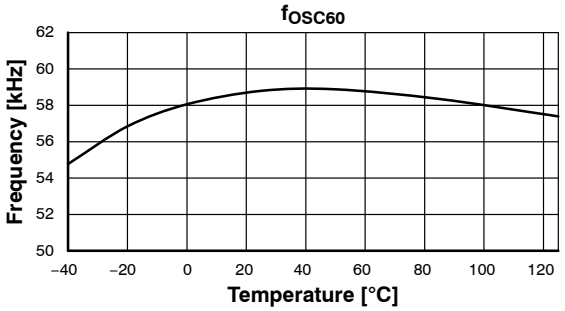


Figure 21. f_{OSC60} vs. Temperature

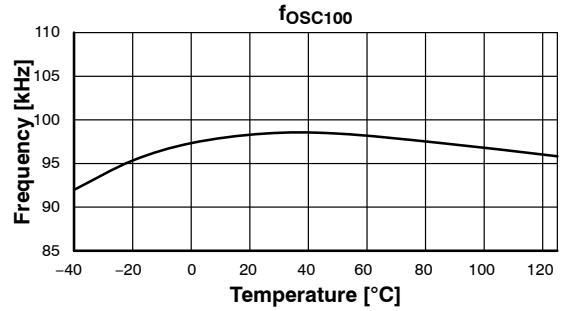


Figure 22. f_{OSC100} vs. Temperature

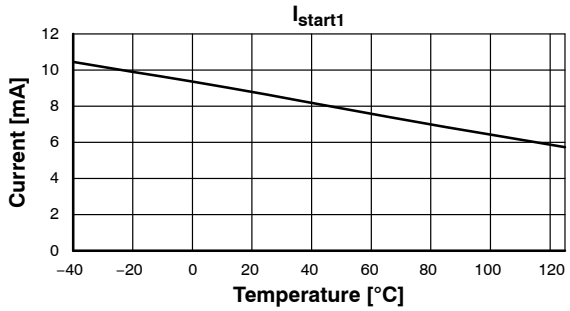


Figure 23. I_{start1} vs. Temperature

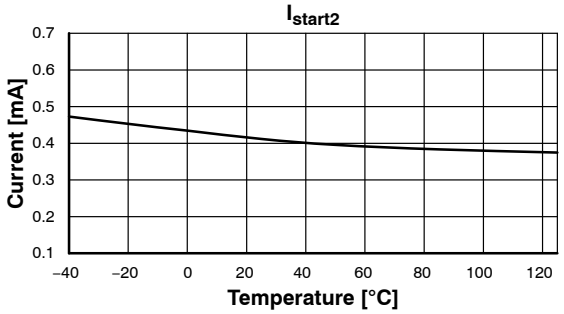


Figure 24. I_{start2} vs. Temperature

TYPICAL CHARACTERISTICS (continued)

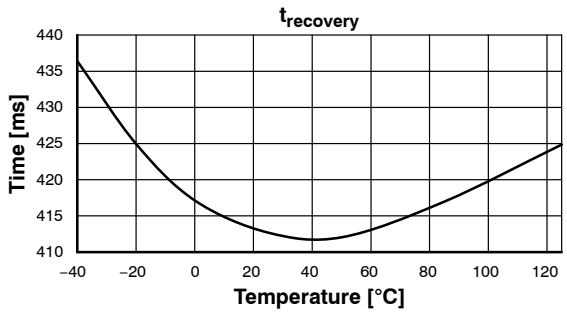


Figure 25. $t_{recovery}$ vs. Temperature

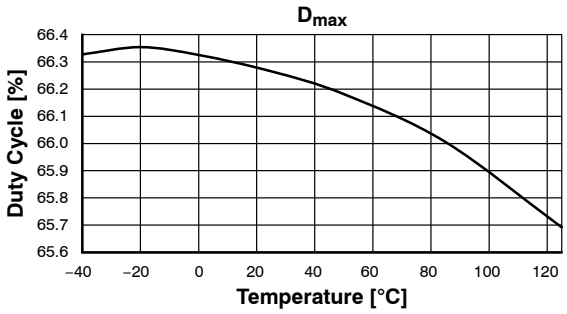


Figure 26. $D_{(max)}$ vs. Temperature

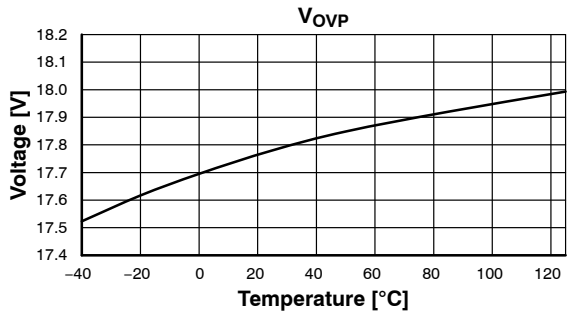


Figure 27. V_{OVP} vs. Temperature

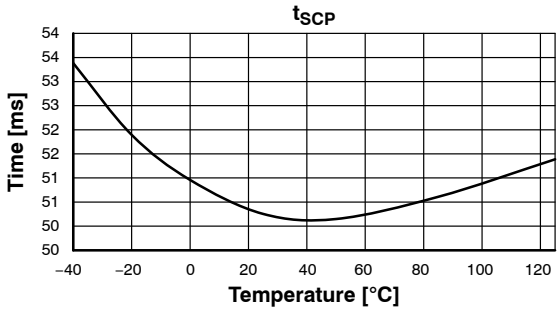


Figure 28. t_{SCP} vs. Temperature

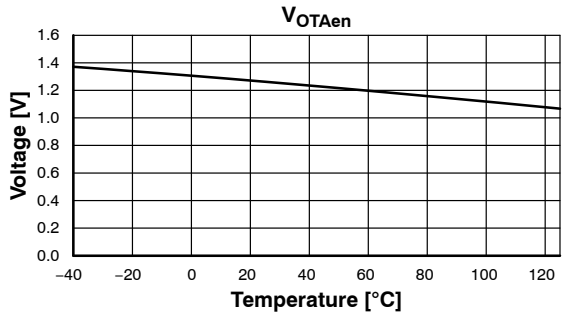


Figure 29. V_{OTAen} vs. Temperature

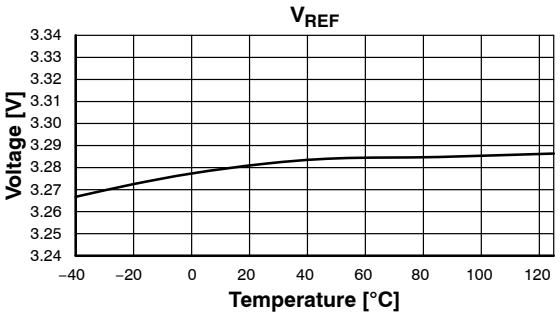


Figure 30. V_{REF} vs. Temperature

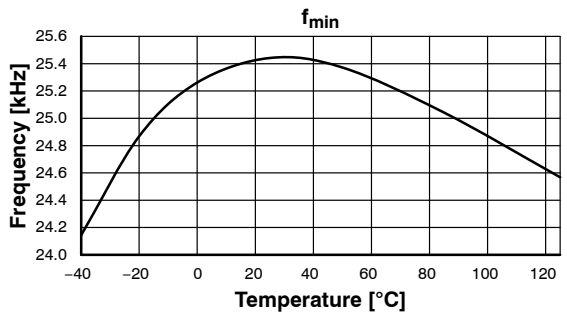


Figure 31. f_{min} vs. Temperature

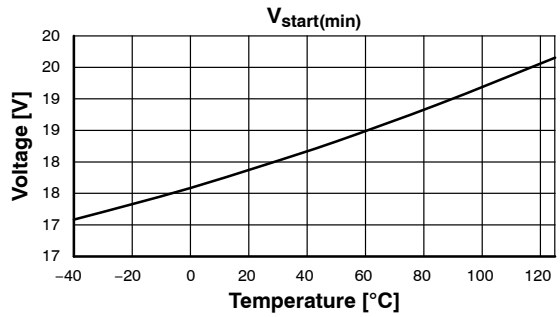


Figure 32. $V_{start(min)}$ vs. Temperature

APPLICATION INFORMATION

Introduction

The NCP1067X offers a complete current−mode control solution. The component integrates everything needed to build a rugged and cost effective Switch−Mode Power Supply (SMPS) featuring low standby power. The Quick Selection Table is on details the differences between references, mainly peak current setpoints, $R_{DS(on)}$ value and operating frequency.

- *Current−mode operation:* the controller uses current−mode control architecture.
- *700 V − _ Power MOSFET:* Due to ON Semiconductor Very High Voltage Integrated Circuit technology, the circuit hosts a high−voltage power MOSFET featuring a 34 or 12 Ω $R_{DS(on)}$ − Tj = 25°C. This value lets the designer build a power supply up to 7.8 W operated on universal mains. An internal current source delivers the startup current, necessary to crank the power supply.
- *Dynamic Self−Supply:* Due to the internal high voltage current source, this device could be used in the application without the auxiliary winding to provide supply voltage.
- *Short circuit protection:* by permanently monitoring the COMP line activity, the IC is able to detect the presence of a short−circuit, immediately reducing the output power for a total system protection. A t_{SCP} timer is started as soon as the COMP current is below threshold, $I_{COMPfault}$, which indicates the maximum peak current. If at the end of this timer the fault is still present, then the device enters a safe, auto−recovery burst mode, affected by a fixed timer recurrence, $t_{recovery}$. Once the short has disappeared, the controller resumes and goes back to normal operation.
- *Built−in VCC Over Voltage Protection:* when the auxiliary winding is used to bias the V_{CC} pin (no DSS), an internal comparator is connected to V_{CC} pin. In case the voltage on the pin exceeds a level of V_{OVP} (18 V typically), the controller immediately stops switching and waits a full timer period ($t_{recovery}$) before attempting to restart. If the fault is gone, the controller resumes operation. If the fault is still there, e.g. a broken opto−coupler, the controller protects the load through a safe burst mode.
- *Frequency jittering:* an internal low−frequency modulation signal varies the pace at which the oscillator frequency is modulated. This helps spreading out energy in conducted noise analysis.
- *Soft−Start:* a 4 ms soft−start ensures a smooth startup sequence, reducing output overshoots.
- *Skip:* if SMPS naturally exhibits a good efficiency at nominal load, they begin to be less efficient when the output power demand diminishes. By skipping un−needed switching cycles, the NCP1067X drastically reduces the power wasted during light load conditions.

Startup sequence

When the power supply is first powered from the mains outlet, the internal current source (typically 8.0 mA) is biased and charges up the V_{CC} capacitor from the drain pin. Once the voltage on this V_{CC} capacitor reaches the $V_{CC(on)}$ level (typically 9.0 V), the current source turns off and pulses are delivered by the output stage: the circuit is awake and activates the power MOSFET if the bulk voltage is above $V_{start(min)}$ (22 V dc). Figure 33 details the simplified internal circuitry.

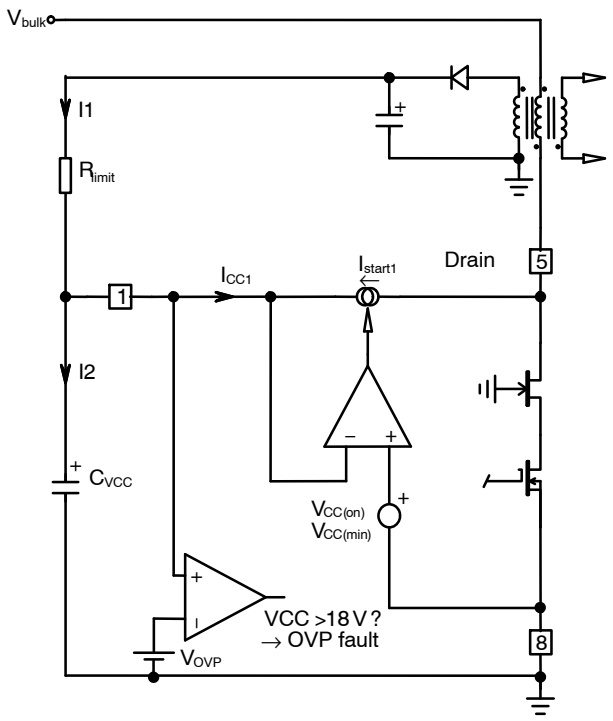


Figure 33. The Internal Arrangement of the Start−up Circuitry

Being loaded by the circuit consumption, the voltage on the V_{CC} capacitor goes down. When V_{CC} is below $V_{CC(min)}$ level (7.5 V typically), it activates the internal current source to bring V_{CC} toward $V_{CC(on)}$ level and stops again: a cycle takes place whose low frequency depends on the V_{CC} capacitor and the IC consumption. A 1.5 V ripple takes place on the V_{CC} pin whose average value equals ($V_{CC(on)}$ + $V_{CC(min)}$) / 2. Figure 34 portrays a typical operation of the DSS.

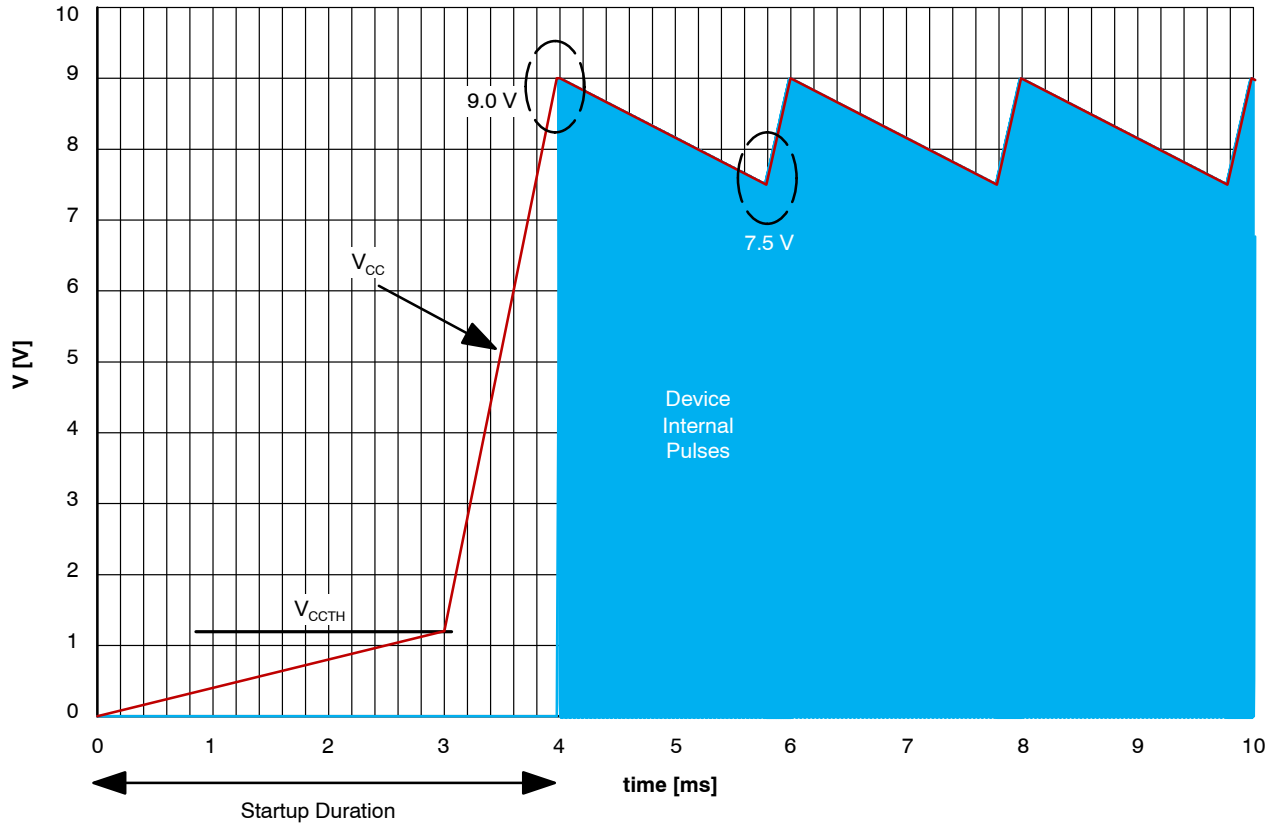


Figure 34. The Charge/Discharge Cycle Over a 1 μF V_{CC} Capacitor

As one can see, even if there is auxiliary winding to provide energy for V_{CC}, it happens that the device is still biased by DSS during start−up time or some fault mode when the voltage on auxiliary winding is not ready yet. The V_{CC} capacitor shall be dimensioned to avoid V_{CC} crosses $V_{CC(off)}$ level, which stops operation. The ΔV between $V_{CC(min)}$ and $V_{CC(off)}$ is 0.5 V. There is no current source to charge V_{CC} capacitor when driver is on, i.e. drain voltage is close to zero. Hence the V_{CC} capacitor can be calculated using

$$C_{VCC} \geq \frac{I_{CC1} D_{max}}{f_{OSC} \cdot \Delta V} \qquad \text{(eq. 1)}$$

Take the 60 kHz device as an example. C_{VCC} should be above

$$\frac{0.84\ m \cdot 72\%}{54\ kHz \cdot 0.5} = 22\ nF \qquad \text{(eq. 2)}$$

A margin that covers the temperature drift and the voltage drop due to switching inside FET should be considered, and thus a capacitor above 0.1 μF is appropriate.

The V_{CC} capacitor has only a supply role and its value does not impact other parameters such as fault duration or the frequency sweep period for instance. As one can see on Figure 33, an internal OVP comparator, protects the switcher against lethal V_{CC} runaways. This situation can occur if the feedback loop optocoupler fails, for instance, and you would like to protect the converter against an over voltage event. In that case, the over voltage protection (OVP) circuit and immediately stops the output pulses for $t_{recovery}$ duration (400 ms typically). Then a new start−up attempt takes place to check whether the fault has disappeared or not. The OVP paragraph gives more design details on this particular section.

Fault Condition – Short−circuit on V_{CC}

In some fault situations, a short−circuit can purposely occur between V_{CC} and GND. In high line conditions (V_{HV} = 370 V_{DC}) the current delivered by the startup device will seriously increase the junction temperature. For instance, since I_{start1} equals 4 mA (the min corresponds to the highest T_j), the device would dissipate 370 · 4 m 1.48 W. To avoid this situation, the controller includes a novel circuitry made of two startup levels, I_{start1} and I_{start2}. At power−up, as long as V_{CC} is below a 1.2 V level, the source delivers I_{start2} (around 400 μA typical), then, when V_{CC} reaches 1.2 V, the source smoothly transitions to I_{start1} and delivers its nominal value. As a result, in case of short−circuit between V_{CC} and GND, the power dissipation will drop to 370 · 400 μ = 148 mW. Figure 34 portrays this particular behavior.

The first startup period is calculated by the formula C · V = I · t, which implies a 1 μ · 1.2 / 400 μ = 3 ms startup time for the first sequence. The second sequence is obtained by toggling the source to 8 mA with a delta V of $V_{CC(on)} - V_{CCTH}$ = 9.0 – 1.2 = 7.8 V, which finally leads to a second startup time of 1 μ · 7.8 / 8 m = 975 μs. The total startup time becomes 3 m + 0.975 m = 3.975 ms. Please note that this calculation is approximated by the presence of the knee in the vicinity of the transition.

Fault Condition – Output Short−circuit

As soon as V_{CC} reaches $V_{CC(on)}$, drive pulses are internally enabled. If everything is correct, the auxiliary winding increases the voltage on the V_{CC} pin as the output voltage rises. During the start−sequence, the controller smoothly ramps up the peak drain current to maximum setting, i.e. I_{IPK}, which is reached after a typical period of 4 ms. When the output voltage is not regulated, the current coming through COMP pin is below $I_{COMPfault}$ level (40 μA typically), which is not only during the startup period but also anytime an overload occurs, an internal error flag is asserted, Ipflag, indicating that the system has reached its maximum current limit set point. The assertion of this flag triggers a fault counter t_{SCP} (48 ms typically). If at counter completion, I_{pflag} remains asserted, all driving pulses are stopped and the part stays off in $t_{recovery}$ duration (about 400 ms). A new attempt to re−start occurs and will last 48 ms providing the fault is still present. If the fault still affects the output, a safe burst mode is entered, affected by a low duty−cycle operation (11%). When the fault disappears, the power supply quickly resumes operation. Figure 35 depicts this particular mode:

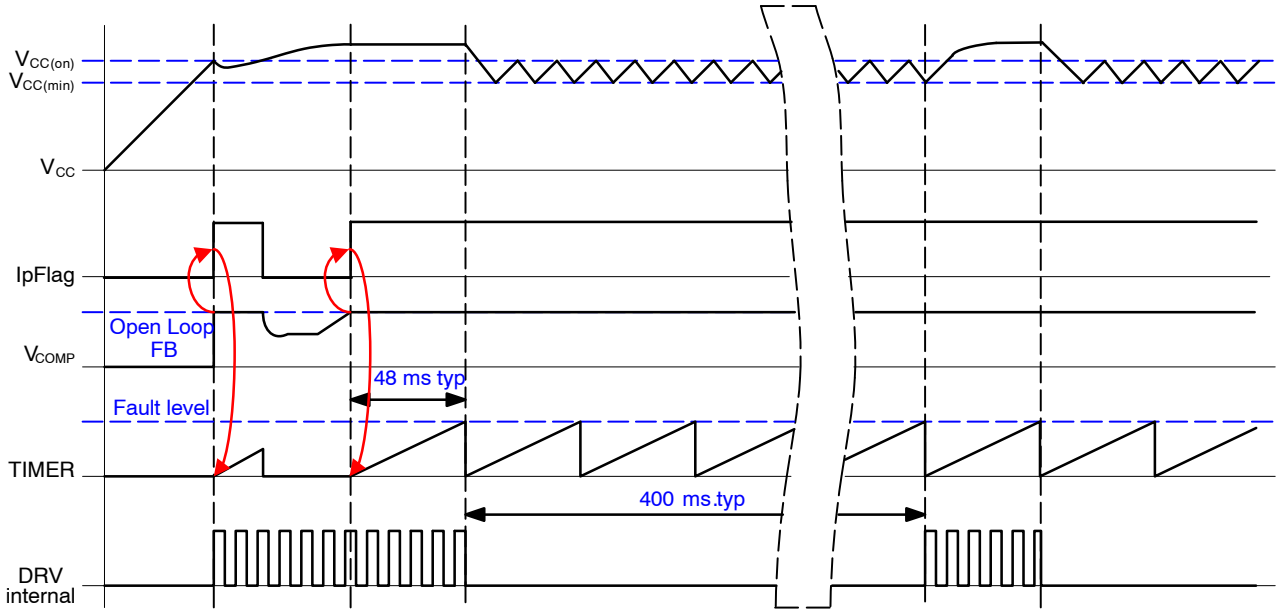


Figure 35. In Case of Short−circuit or Overload, the NCP1067X Protects Itself and the Power Supply via a Low Frequency Burst Mode. The V_{CC} is Maintained by the Current Source and Self−supplies the Controller.

Auto−recovery Over Voltage Protection

The particular NCP1067X arrangement offers a simple way to prevent output voltage runaway when the optocoupler fails. As Figure 36 shows, a comparator monitors the V_{CC} pin. If the auxiliary pushes too much voltage into the C_{VCC} capacitor, then the controller considers an OVP situation and stops the internal drivers. When an OVP occurs, all switching pulses are permanently disabled. After $t_{recovery}$ delay, it resumes the internal drivers. If the failure symptom still exists, e.g. feedback opto−coupler fails, the device keeps the auto−recovery OVP mode. It is recommended insertion of a resistor (R_{limit}) between the auxiliary dc level and the V_{CC} pin to protect the IC against high voltage spikes, which can damage the IC, and to filter out the Vcc line to avoid undesired OVP activation. R_{limit} should be carefully selected to avoid triggering the OVP as we discussed, but also to avoid disturbing the V_{CC} in low / light load conditions.

Self−supplying controllers in extremely low standby applications often puzzles the designer. Actually, if a SMPS operated at nominal load can deliver an auxiliary voltage of an arbitrary 16 V (V_{nom}), this voltage can drop below 10 V (V_{stby}) when entering standby. This is because the recurrence of the switching pulses expands so much that the low frequency re−fueling rate of the V_{CC} capacitor is not enough to keep a proper auxiliary voltage.

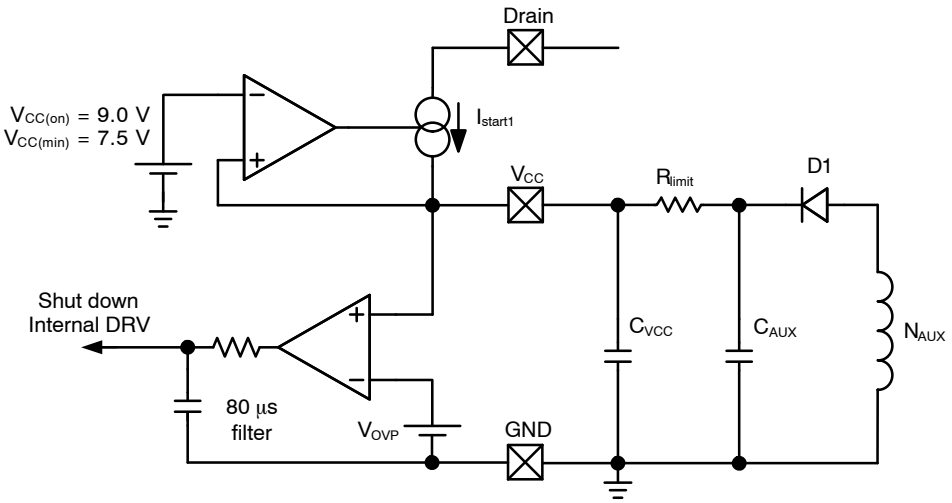


Figure 36. A More Detailed View of the NCP1067X Offers Better Insight on How to Properly Wire an Auxiliary Winding

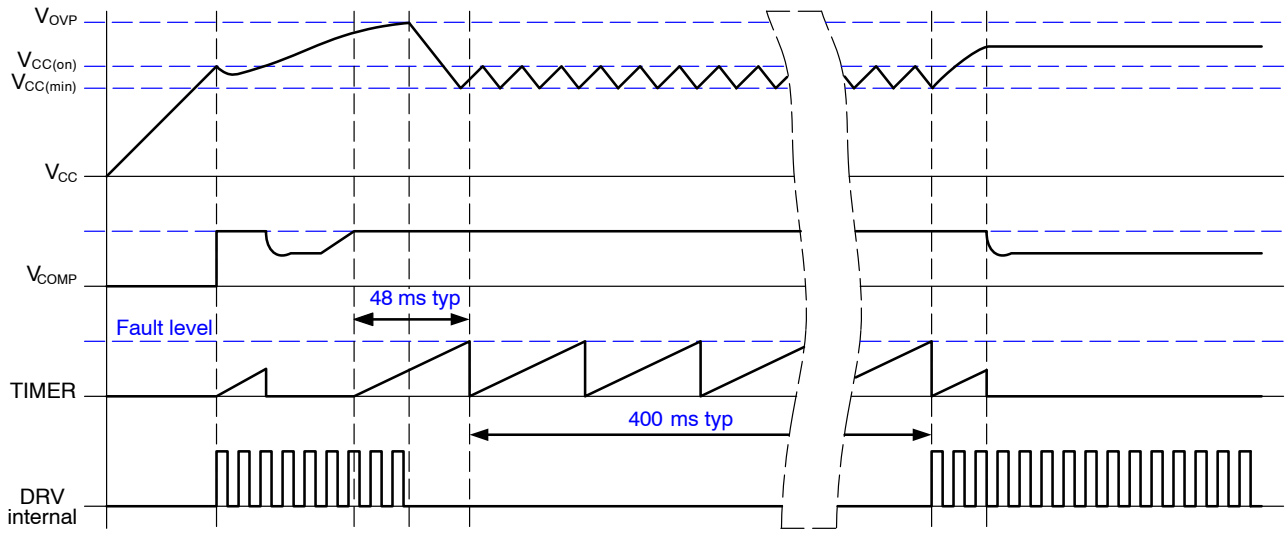


Figure 37 Describes the Main Signal Variations when the Part Operates in Auto−recovery OVP:

Figure 37. If the VCC Current Exceeds a Certain Threshold, an Auto−recovery Protection is Activated

Soft−start

The NCP1067X features a 4 ms soft−start which reduces the power−on stress but also contributes to lower the output overshoot. Figure 38 shows a typical operating waveform. The NCP1067X features a novel patented structure which offers a better soft−start ramp, almost ignoring the start−up pedestal inherent to traditional current−mode supplies:

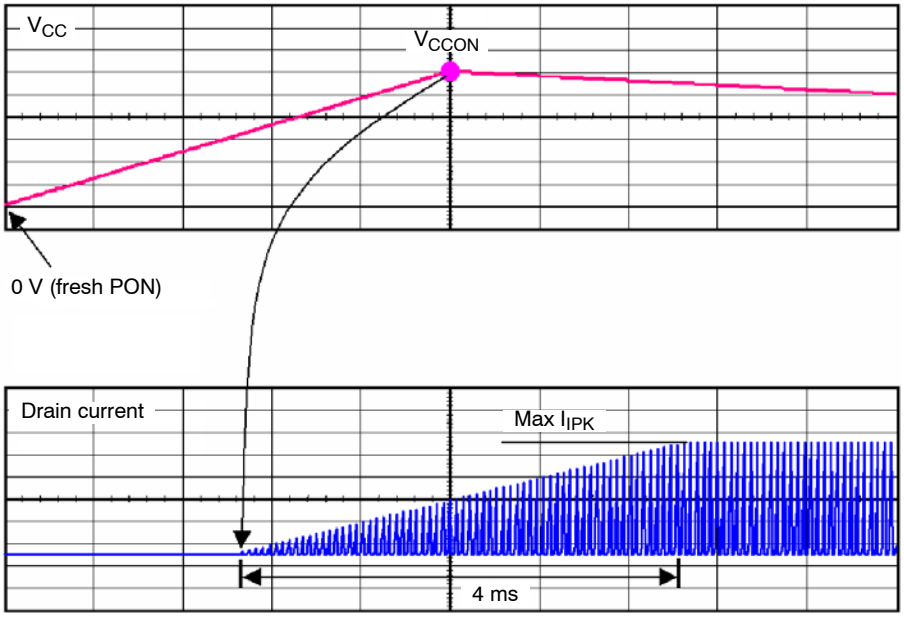


Figure 38. The 4 ms Soft−start Sequence

Jittering

Frequency jittering is a method used to soften the EMI signature by spreading the energy in the vicinity of the main switching component. The NCP1067X offers a ±6% deviation of the nominal switching frequency. The sweep sawtooth is internally generated and modulates the clock up and down with a fixed frequency of 300 Hz. Figure 39 shows the relationship between the jitter ramp and the frequency deviation. It is not possible to externally disable the jitter.

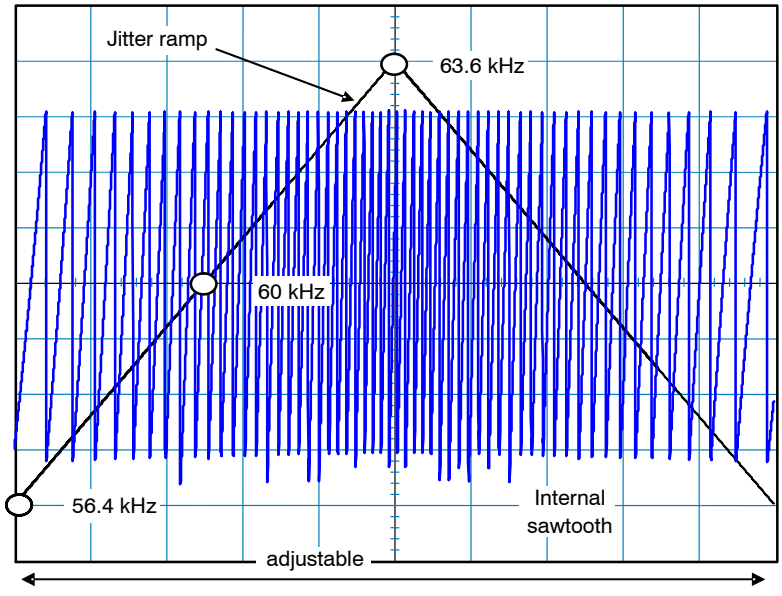


Figure 39. Modulation Effects on the Clock Signal by the Jittering Sawtooth

Ipk Reduction

The internal peak current set−point is following the COMP current information until its level reaches I_{Freeze}. Below this value, the peak current setpoint is frozen to 30% of the $I_{IPK(0)}$. This value is reached at a COMP current level of $I_{COMPskip}$ (120 μA typically). Below this point, if the output power continues to decrease, the part enters skip cycle for the best performance in no−load conditions. Figure 40 depict the adopted scheme for the part.

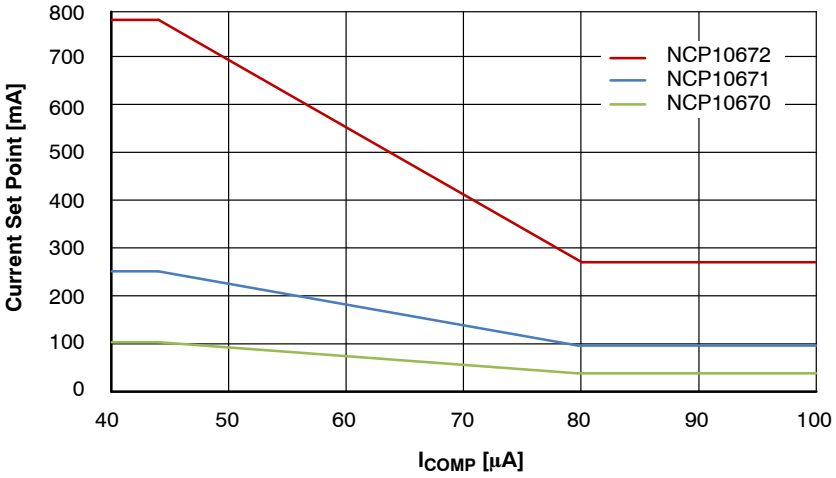


Figure 40. I_{IPK} Set−point is Frozen at Lower Power Demand

Feedback and Skip

Figure 41 depicts the relationship between COMP pin voltage and current. The COMP pin operates linearly as the absolute value of COMP current (I_{COMP}) is above 40 μA. In this linear operating range, the dynamic resistance is 17.7 kΩ typically ($R_{COMP(up)}$) and the effective pull up voltage is 2.7 V typically ($V_{COMP(REF)}$). When I_{COMP} is decreases, the COMP voltage will increase to 3.2 V.

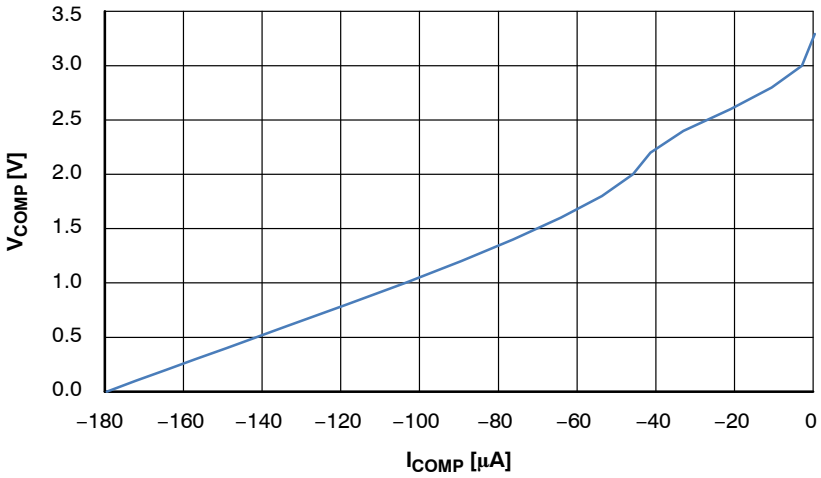


Figure 41. COMP Pin Voltage vs. Current

Figure 42 depicts the skip mode block diagram. When the COMP current information reaches $I_{COMPskip}$, the internal clock to set the flip−flop is blanked and the internal consumption of the controller is decreased. The hysteresis of internal skip comparator is minimized to lower the ripple of the auxiliary voltage for V_{CC} pin and V_{OUT} of power supply during skip mode. It easies the design of V_{CC} over load range.

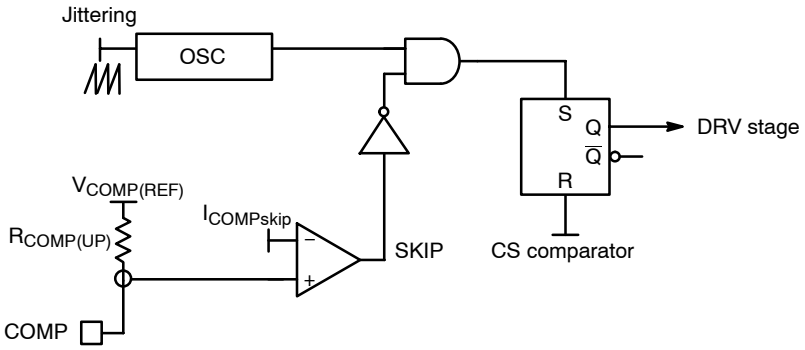


Figure 42. Skip Cycle Schematic

Ramp Compensation and Ipk Set−point

In order to allow the NCP106X to operate in CCM with a duty cycle above 50%, a fixed slope compensation is internally applied to the current−mode control.

Here we got a table of the ramp compensation, the initial current set point, and the final current set−point of different versions of switcher.

	NCP10670		NCP10671		NCP10672	
F_{sw}	60 kHz	100 kHz	60 kHz	100 kHz	60 kHz	100 kHz
S_a	2.8 mA/μs	4.7 mA/μs	8.4 mA/μs	14 mA/μs	15.6 mA/μs	26 mA/μs
$I_{IPK(Duty = 50\%)}$	83 mA		208 mA		650 mA	
$I_{IPK(0)}$	100 mA		250 mA		780 mA	

Figure 43 depicts the variation of I_{IPK} set−point vs. the power switcher duty ratio, which is caused by the internal ramp compensation.

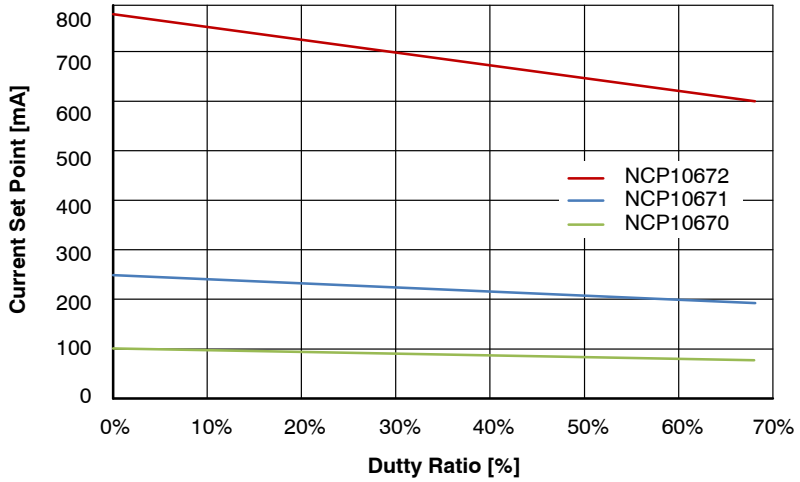


Figure 43. I_{IPK} Set−point Varies with Power Switch on Time, Which is Caused by the Ramp Compensation

FB pin function

The FB pin is used in non isolated SMPS application only. Portion of the output voltage is connected into the pin. The voltage is compared with internal V_{REF} (3.3 V) using Operation Transconductance Amplifier (Figure 44). The OTAs output is connected to COMP pin. From the outside an user defined compensation network is connected to the COMP pin. The current capability of OTA is limited to −150 μA typically. The positive current is defined by internal $R_{COMP(up)}$ resistor and $V_{COMP(ref)}$ voltage. If FB path loop is broken (i.e. the FB pin is disconnected), an internal current I_{FB} (1 μA typ.) will pull up the FB pin and the IC stops switching to avoid uncontrolled output voltage increasing.

In isolated topology, the FB pin should be connected to GND pin. In this configuration no current flows from OTA to COMP pin (OTA is disabled) so the OTA has no influence on regulation at all.

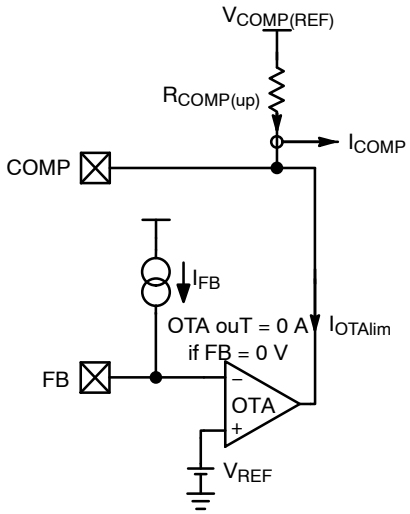


Figure 44. FB Pin Connection

Design Procedure

The design of an SMPS around a monolithic device does not differ from that of a standard circuit using a controller and a MOSFET. However, one needs to be aware of certain characteristics specific of monolithic devices. Let us follow the steps:

V_{in} min = 90 Vac or 127 Vdc once rectified, assuming a low bulk ripple

V_{in} max = 265 Vac or 375 Vdc

V_{out} = 12 V

P_{out} = 5 W

Operating mode is CCM

η = 0.8

1. The lateral MOSFET body−diode shall never be forward biased, either during start−up (because of a large leakage inductance) or in normal operation as shown in Figure 45. This condition sets the maximum voltage that can be reflected during t_{off}. As a result, the Flyback voltage which is reflected on the drain at the switch opening cannot be larger than the input voltage. When selecting components, you thus must adopt a turn ratio which adheres to the following equation:

$$N\,(V_{out} + V_f) < V_{in,\,min} \qquad \text{(eq. 3)}$$

2. In our case, since we operate from a 127 V DC rail while delivering 12 V, we can select a reflected voltage of 120 V dc maximum. Therefore, the turn ratio Np:Ns must be smaller than

$$\frac{V_{reflect}}{V_{out} + V_f} = \frac{120}{12 + 0.5} = 9.6 \qquad \text{(eq. 4)}$$

or Np:Ns < 9.6. Here we choose N = 8 in this case. We will see later on how it affects the calculation.

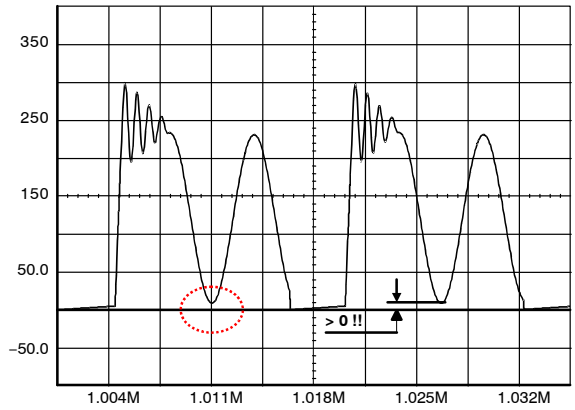


Figure 45. The Drain−Source Wave Shall Always be Positive

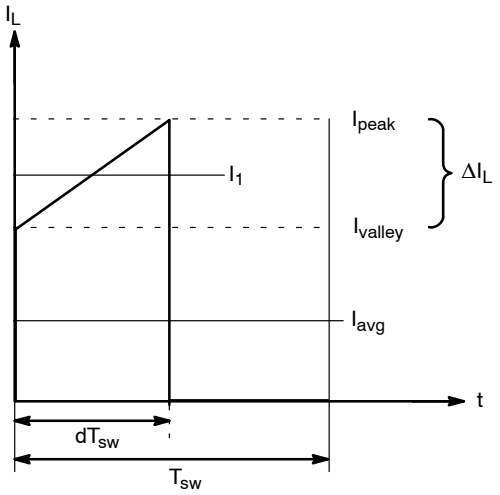


Figure 46. Primary Inductance Current Evolution in CCM

3. Lateral MOSFETs have a poorly doped body−diode which naturally limits their ability to sustain the avalanche. A traditional RCD clamping network shall thus be installed to protect the MOSFET. In some low power applications, a simple capacitor can also be used since

$$V_{drain,max} = V_{in} + N\,(V_{out} + V_f) + I_{peak}\sqrt{\frac{L_f}{C_{tot}}} \quad \text{(eq. 5)}$$

where L_f is the leakage inductance, C_{tot} the total capacitance at the drain node (which is increased by the capacitor you will wire between drain and source), N the N_P:N_S turn ratio, V_{out} the output voltage, V_f the secondary diode forward drop and finally, I_{peak} the maximum peak current. Worse case occurs when the SMPS is very close to regulation, e.g. the V_{out} target is almost reached and I_{peak} is still pushed to the maximum. For this design, we have selected our maximum voltage around 650 V (at V_{in} = 375 Vdc). This voltage is given by the *RCD* clamp installed from the drain to the bulk voltage. We will see how to calculate it later on.

4. Calculate the maximum operating duty−cycle for this flyback converter operated in CCM:

$$d_{max} = \frac{N\,(V_{out} + V_f)}{N\,(V_{out} + V_f) + V_{in,min}} = \frac{1}{1 + \dfrac{V_{in,min}}{N\,(V_{out}+V_f)}} = 0.44 \quad \text{(eq. 6)}$$

5. To obtain the primary inductance, we have the choice between two equations:

$$L = \frac{(V_{in}\,d)^2}{f_{sw}\,K\,P_{in}} \quad \text{(eq. 7)}$$

where

$$K = \frac{\Delta I_L}{I_{Lavg}} \quad \text{(eq. 8)}$$

and defines the amount of ripple we want in CCM (see Figure 46).

- *Small K*: deep CCM, implying a large primary inductance, a low bandwidth and a large leakage inductance.
- *Large K*: approaching DCM where the RMS losses are worse, but smaller inductance, leading to a better leakage inductance.

From eq.17, a *K* factor of 1 (50% ripple), gives an inductance of:

$$L = \frac{(127 \cdot 0.44)^2}{60k \cdot 1 \cdot 5)} = 10.04\ mH \quad \text{(eq. 9)}$$

$$\Delta I_L = \frac{V_{in}d}{LF_{SW}} = \frac{127 \cdot 0.44}{10.04\ m \cdot 60\ k}\ 92.8\ mA \quad \text{(eq. 10)}$$

peak to peak

The peak current can be evaluated to be:

$$I_{peak} = \frac{I_{avg}}{d} + \frac{\Delta I_L}{2} = \frac{49.2\ m}{0.44} + \frac{92.8\ m}{2} = 158\ mA \quad \text{(eq. 11)}$$

On , I_1 can also be calculated:

$$I_{Lavg} = I_{peak} - \frac{\Delta I_L}{2} = 158\ m - \frac{92.8\ m}{2} = 111.6\ mA \quad \text{(eq. 12)}$$

6. Based on the above numbers, we can now evaluate the conduction losses:

$$I_{d,rms} = \sqrt{d\left(I_{peak}^2 - I_{peak}\Delta I_L + \frac{\Delta I_L^2}{3}\right)} = \sqrt{d\left(I_{peak}^2 - I_{peak}\Delta I_L + \frac{\Delta I_L^2}{3}\right)} = 57\ mA \quad \text{(eq. 13)}$$

If we take the maximum $R_{ds(on)}$ for a 125°C junction temperature, i.e. 34 Ω, then conduction losses worse case are:

$$P_{cond} = I_{d,dms}{}^2\,R_{ds\ (on)} = 110mW \quad \text{(eq. 14)}$$

7. Off−time and on−time switching losses can be estimated based on the following calculations:

$$P_{off} = \frac{I_{peak}\,(V_{bulk} + V_{clamp})\,t_{off}}{2T_{SW}} = \frac{0.158 \cdot (127 + 100 \cdot 2) \cdot 10\ n}{2 \cdot 16.7\ \mu} = 15.5\ mW \quad \text{(eq. 15)}$$

Where, assume the V_{clamp} is equal to 2 times of reflected voltage.

$$P_{on} = \frac{I_{valley}\,(V_{bulk} + N\,(V_{out} + V_f))\,t_{on}}{6T_{SW}} = \frac{0.0464 \cdot (127 + 100 \cdot 2) \cdot 20\ n}{6 \cdot 16.7\ \mu} = 2.1\ mW \quad \text{(eq. 16)}$$

It is noted that the overlap of voltage and current seen on MOSFET during turning on and off duration is dependent on the snubber and parasitic capacitance seen from drain pin. Therefore the t_{off} and t_{on} in eq. 15 and eq. 16 have to be modified after measuring on the bench.

8. The theoretical total power is then
117 + 15.5 + 2.1 = 127.6 mW
9. If the NCP106X operates at DSS mode, then the losses caused by DSS mode should be counted as losses of this device on the following calculation:

$$P_{DSS} = I_{cc1} \cdot V_{in,max} = 0.8\ m \cdot 375 = 300\ mW \quad \text{(eq. 17)}$$

MOSFET Protection

As in any Flyback design, it is important to limit the drain excursion to a safe value, e.g. below the MOSFET BVdss which is 700 V. Figure 47 *a–b–c* present possible implementations:

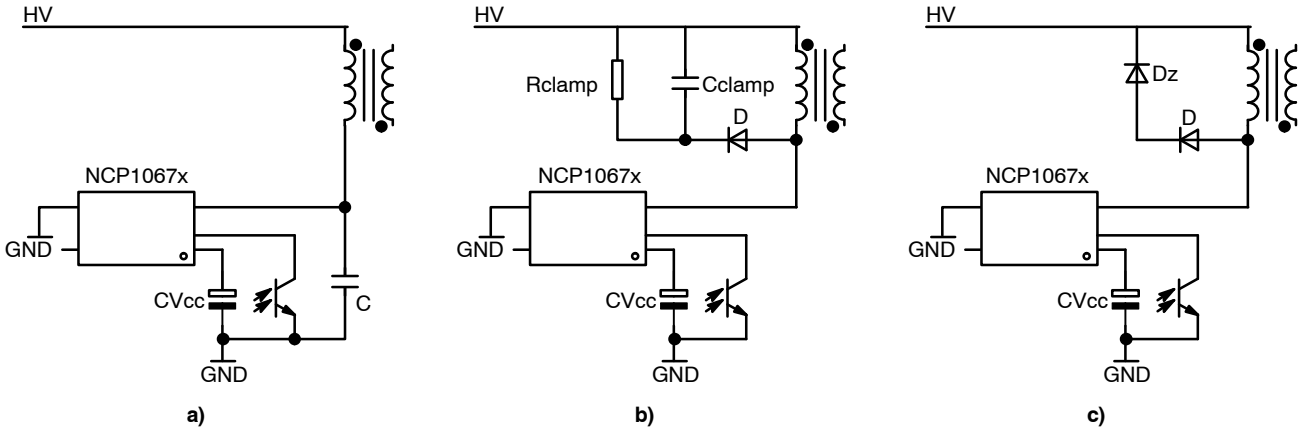


Figure 47. Different Options to Clamp the Leakage Spike

Figure 47a: the simple capacitor limits the voltage according to the lateral MOSFET body−diode shall never be forward biased, either during start−up (because of a large leakage inductance) or in normal operation as shown by Figure 45. This condition sets the maximum voltage that can be reflected during t_{off}. As a result, the flyback voltage which is reflected on the drain at the switch opening cannot be larger than the input voltage. When selecting components, you must adopt a turn ratio which adheres to the following equation *eq. 5*. This option is only valid for low power applications, e.g. below 5 W, otherwise chances exist to destroy the MOSFET. After evaluating the leakage inductance, you can compute C with (eq. 6). Typical values are between 100 pF and up to 470 pF. Large capacitors increase capacitive losses…

Figure 47b: the most standard circuitry is called the *RCD* network. You can calculate R_{clamp} and C_{clamp} using the following formula:

$$R_{clamp} = \frac{2\, V_{clamp}\, (V_{clamp} + (V_{out} + V_f)\, N)}{L_{leak}\, I_{leak}^{2}\, F_{sw}} \qquad \text{(eq. 18)}$$

$$C_{clamp} = \frac{V_{clamp}}{V_{ripple}\, F_{sw}\, R_{clamp}} \qquad \text{(eq. 19)}$$

V_{clamp} is usually selected 50 – 80 V above the reflected value N x $(V_{out} + V_f)$. The diode needs to be a fast one and a MUR160 represents a good choice. One major drawback of the RCD network lies in its dependency upon the peak current. Worse case occurs when I_{peak} and V_{in} are maximum and V_{out} is close to reach the steady−state value.

Figure 47c: this option is probably the most expensive of all three but it offers the best protection degree. If you need a very precise clamping level, you must implement a zener diode or a TVS. There are little technology differences behind a standard zener diode and a TVS. However, the die area is far bigger for a transient suppressor than that of zener. A 5 W zener diode like the 1N5388B will accept 180 W peak power if it lasts less than 8.3 ms. If the peak current in the worse case (e.g. when the PWM circuit maximum current limit works) multiplied by the nominal zener voltage exceeds these 180 W, then the diode will be destroyed when the supply experiences overloads. A transient suppressor like the P6KE200 still dissipates 5 W of continuous power but is able to accept surges up to 600 W @ 1 ms. Select the zener or TVS clamping level between 40 to 80 volts above the reflected output voltage when the supply is heavily loaded.

As a good design practice, it is recommended to implement one of this protection to make sure Drain pin voltage doesn't go above 650 V (to have some margin between Drain pin voltage and BVdss) during most stringent operating conditions (high Vin and peak power).

Power Dissipation and Heatsinking

The NCP1067X welcomes two dissipating terms, the DSS current−source (when active) and the MOSFET. Thus, $P_{tot} = P_{DSS} + P_{MOSFET}$. It is mandatory to properly manage the heat generated by losses. If no precaution is taken, risks exist to trigger the internal thermal shutdown (TSD). To help dissipating the heat, the PCB designer must foresee large copper areas around the package. When the package is surrounded by a surface approximately 200 mm^2 of 35 μm copper, the maximum power the device can thus evacuate is:

$$P_{max} = \frac{t_{jmax} - t_{ambmax}}{R_{\theta JA}} \qquad \text{(eq. 20)}$$

which gives around 862 mW for an ambient of 50°C and a maximum junction of 150°C. If the surface is not large enough, the $R_{\theta JA}$ is growing and the maximum power the device can evacuate decreases. Figure 48 gives a possible layout to help drop the thermal resistance.

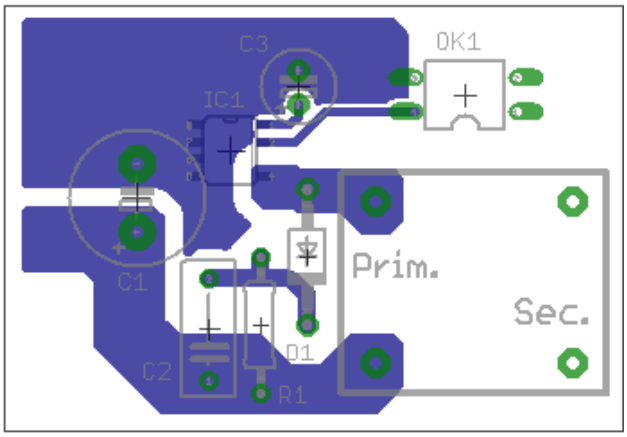


Figure 48. A Possible PCB Arrangement to Reduce the Thermal Resistance Junction−to−Ambient

Bill of Material:

C1 Bulk capacitor, input DC voltage is connected to the capacitor
C2, R1, D1 Clamping elements
C3 Vcc capacitor
OK1 Optocoupler

ORDERING INFORMATION

Device	Marking	Frequency	$R_{DS(on)}$	$I_{IPK(0)}$	Package Type	Shipping†
NCP10670BD060R2G	P10670060	60 kHz	34	100 mA	SOIC−8 MISSING PIN 3 (Pb−Free)	2500 / Tape & Reel
NCP10670BD100R2G	P10670100	100 kHz	34	100 mA		2500 / Tape & Reel
NCP10671BD060R2G	P10671060	60 kHz	34	250 mA		2500 / Tape & Reel
NCP10671BD100R2G	P10671100	100 kHz	34	250 mA		2500 / Tape & Reel
NCP10672BD060R2G	P10672060	60 kHz	12	780 mA		2500 / Tape & Reel
NCP10672BD100R2G	P10672100	100 kHz	12	780 mA		2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

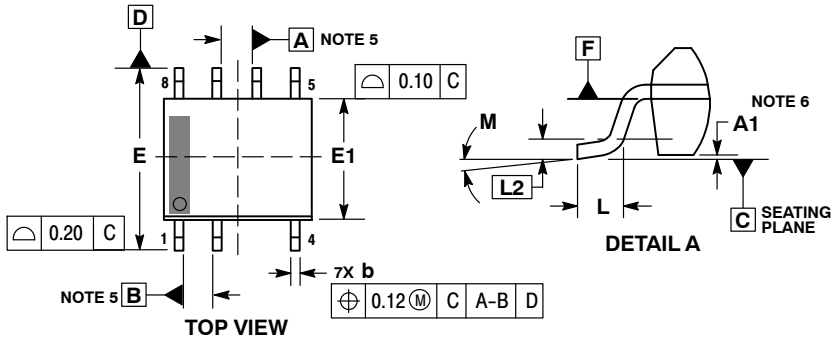
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

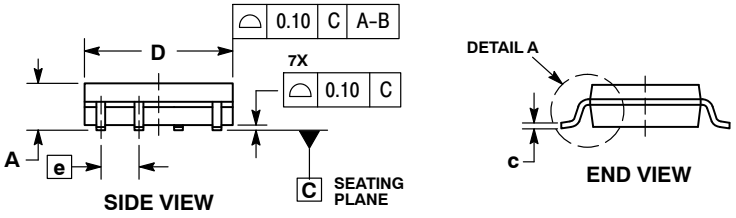
ON Semiconductor®

SCALE 1:1

SOIC8 MISSING PIN 3
CASE 751EV
ISSUE O

DATE 19 SEP 2017

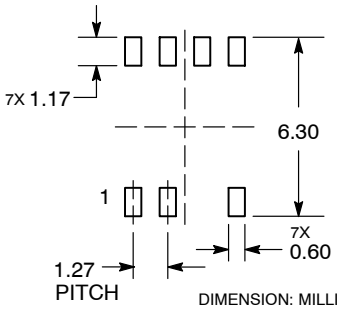




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D & E1 DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM F.
5. DATUMS A AND B ARE TO BE DETERMINED AT DATUM F.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

	MILLIMETERS	
DIM	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
b	0.33	0.51
c	0.19	0.25
D	4.80	5.00
E	5.80	6.20
E1	3.80	4.00
e	1.27 BSC	
L	0.40	1.27
L2	0.25 BSC	
M	0 °	8 °

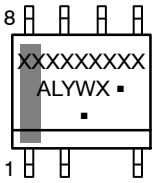
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G”, may or not be present. Some products may not follow the Generic Marking.

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