Ordering number : ENA1764B

SANYO Semiconductors
DATA SHEET
An ON Semiconductor Company

LV5680P — Monolithic Linear IC For Car Audio Systems Multi-Power Supply System IC

Overview

The LV5680P is a multi-power supply system IC that provides four regulator outputs and two high side switches as well as a number of protection functions including overcurrent protection, overvoltage protection and overheat protection. It is an optimal power supply IC for car audio and car entertainment systems and similar products.

Features

- Four regulator output systems
  - For microcontroller: 5.0V output voltage, 200mA maximum output current
  - For CD drive: 8.0V output voltage, 1300mA maximum output current
  - For illumination: 8 to 12V output voltage (output can be set with external resistors), 300mA maximum output current
  - For audio systems: 8 to 9V output voltage (output voltage can be set with external resistors), 300mA maximum output current
- Two V_{CC}-linked high side switch systems
  - EXT: 350mA maximum output current, 0.5V voltage difference between input and output.
  - ANT: 300mA maximum output current, 0.5V voltage difference between input and output.
- Two V_{DD} 5V-linked high side switch systems
  - SW5V: 200mA maximum output current, 0.2V voltage difference between input and output.
  - ACC (accessory voltage detection output): 100mA maximum output current, 0.2V voltage difference between input and output.
- Overcurrent protection function
- Overvoltage protection function, typ 21V (excluding V_{DD} 5V output)
- Overheat protection function, typ 175ºC
- On-chip accessory voltage detection circuit
- P-channel LDMOS used for power output block

(Warning) The protector functions only improve the IC's tolerance and they do not guarantee the safety of the IC if used under the conditions out of safety range or ratings. Use of the IC such as use under over current protection range or thermal shutdown state may degrade the IC's reliability and eventually damage the IC.

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Conditions	Conditions		Ratings	Unit
Supply voltage	V_{CC} max			36	V
Peak supply voltage	V_{CC} peak	See below for the waveform applied.		50	V
Allowable Power dissipation	Pd max	Independent IC	Ta ≤ 25°C	1.5	W
		Al heat sink *		5.6	W
		With an infinity heat sink		32.5	W
Junction temperature	Tj max			150	°C
Operating ambient temperature	Topr			-40 to +85	°C
Storage temperature	Tstg			-55 to +150	°C

* : When the Aluminum heat sink (50mm × 50mm × 1.5mm) is used

Allowable Operating range at Ta = 25°C

Parameter	Conditions	Ratings	Unit
Operating supply voltage 1	V_{DD} output, SW output, ACC output	7.5 to 16	V
Operating supply voltage 2	ILM output at 10V	12 to 16	V
	ILM output at 8V	10 to 16	V
Operating supply voltage 3	Audio output at 9V	10 to 16	V
Operating supply voltage 4	CD output (CD output current = 1.3A)	10.5 to 16	V
	CD output (CD output current ≤ 1A)	10 to 16	V

Electrical Characteristics at V_{CC} = 14.4V, Ta = 25°C(*6)

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Current drain	I_{CC}	V_{DD} no load, CTRL1/2 =「L/L」, ACC = 0V		400	800	μA
CTRL1 Input						
Low input voltage	$V_{IL}1$		0		0.5	V
M1 input voltage	$V_{IM1}1$		0.8	1.1	1.4	V
M2 input voltage	$V_{IM2}1$		1.9	2.2	2.5	V
High input voltage	$V_{IH}1$		2.9	3.3	5.5	V
Input impedance	$R_{IH}1$		350	500	650	kΩ
CTRL2 Input						
Low input voltage	$V_{IL}2$		0		0.5	V
M input voltage	$V_{IM}2$		1.1	1.65	2.1	V
High input voltage	$V_{IH}2$		2.5	3.3	5.5	V
Input impedance	$R_{IH}2$		350	500	650	kΩ
V_{DD} 5V Output *1		**The V_{DD} 5V output supplies the output currents of SW 5V and ACC 5V.**				
Output voltage 1	V_O1	I_O1 = 200mA, I_O7, I_O8 = 0A	4.75	5.0	5.25	V
Output voltage 2	V_O1’	I_O1 = 200mA, I_O7 = 200mA, I_O8 = 100mA	4.75	5.0	5.25	V
Output total current	Ito1	V_O1 ≥ 4.75V, Ito1 = I_O1+I_O7+I_O8	500			mA
Line regulation	$\Delta V_{OLN}1$	7.5V < V_{CC} < 16V, I_O1 = 200mA *2		30	90	mV
Load regulation	$\Delta V_{OLD}1$	1mA < I_O1 < 200mA *2		70	150	mV
Dropout voltage 1	$V_{DROP}1$	I_O1 = 200mA *2		1.0	1.5	V
Dropout voltage 2	$V_{DROP}1$’	I_O1 = 100mA *2		0.7	1.05	V
Dropout voltage 3	$V_{DROP}1$”	I_O1+I_O7+I_O8 = 500mA		2.5	3.75	V
Ripple rejection	$R_{REJ}1$	f = 120Hz, I_O1 = 200mA *2	40	50		dB
CD Output ; CTRL2 =「H」						
Output voltage	V_O2	I_O2 = 1000mA	7.6	8.0	8.4	V
Output current	I_O2	V_O2 ≥ 7.6V	1300			mA
Line regulation	$\Delta V_{OLN}2$	10.5V < V_{CC} < 16V, I_O2 = 1000mA		50	100	mV

*1 : The V_{DD} 5V output also supplies the output currents of SW 5V and ACC 5V. Therefore, the current supply capability of the V_{DD} 5V output and its other electrical characteristics are affected by the output statuses of SW 5V and ACC 5V.

*2 : SW 5V and ACC 5V are not subject to a load.

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Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Load regulation	$\Delta V_{OLD}2$	10mA < I_O2 < 1000mA		100	200	mV
Dropout voltage 1	$V_{DROP}2$	I_O2 = 1000mA		1.0	1.5	V
Dropout voltage 2	$V_{DROP}2$’	I_O2 = 500mA		0.5	0.75	V
Ripple rejection	$R_{REJ}2$	f = 120Hz, I_O2 = 1000mA	40	50		dB
AUDIO (8-9V) Output ; CTRL2 =⌈M⌋						
AUDIO_F pin voltage	V_I3		1.222	1.260	1.298	V
AUDIO_F pin inflow current	$I_{IN}3$		-1		1	μA
AUDIO output voltage 1	V_O3	I_O3 = 200mA, R2 = 30kΩ, R3 = 5.6kΩ *3	7.65	8.0	8.35	V
AUDIO output voltage 2	V_O3’	I_O3 = 200mA, R2 = 27kΩ, R3 = 4.7kΩ *3	8.13	8.5	8.87	V
AUDIO output voltage 3	V_O3”	I_O3 = 200mA, R2 = 24kΩ, R3 = 3.9kΩ *3	8.6	9.0	9.4	V
AUDIO output current	I_O3		300			mA
Line regulation	$\Delta V_{OLN}3$	10V < V_{CC} < 16V, I_O3 = 200mA		30	90	mV
Load regulation	$\Delta V_{OLD}3$	1mA < I_O3 < 200mA		70	150	mV
Dropout voltage 1	$V_{DROP}3$	I_O3 = 200mA		0.3	0.45	V
Dropout voltage 2	$V_{DROP}3$’	I_O3 = 100mA		0.15	0.23	V
Ripple rejection	$R_{REJ}3$	f = 120Hz, I_O3 = 200mA	40	50		dB
ILM (8-12V) Output ; CTRL1 =⌈M1⌋						
ILM_F pin voltage	V_I4		1.222	1.260	1.298	V
ILM output voltage 1	V_O4	I_O4 = 200mA	11.4	12.0	12.6	V
ILM output voltage 2	V_O4’	I_O4 = 200mA, R1 = 270kΩ *4	8.5	10.0	11.5	V
ILM output voltage 3	V_O4”	I_O4 = 200mA, R1 = 100kΩ *4	6.8	8.0	9.2	V
ILM output current	I_O4	R1 = 270kΩ	300			mA
Line regulation	$\Delta V_{OLN}4$	12V < V_{CC} < 16V, I_O4 = 200mA, R1 = 270kΩ		30	90	mV
Load regulation	$\Delta V_{OLD}4$	1mA < I_O4 < 200mA		70	150	mV
Dropout voltage 1	$V_{DROP}4$	I_O4 = 200mA		0.7	1.05	V
Dropout voltage 2	$V_{DROP}4$’	I_O4 = 100mA		0.35	0.53	V
Ripple rejection	$R_{REJ}4$	f = 120Hz, I_O4 = 200mA	40	50		dB
Remoto (EXT) ; CTRL1 =⌈M2⌋						
Output voltage	V_O5	I_O5 = 350mA	V_{CC}-1.0	V_{CC}-0.5		V
Output current	I_O5	$V_O5 \geq V_{CC}$-1.0	350			mA
ANT remoto ; CTRL1 =⌈H⌋						
Output voltage	V_O6	I_O6 = 300mA	V_{CC}-1.0	V_{CC}-0.5		V
Output current	I_O6	$V_O6 \geq V_{CC}$-1.0	300			mA
SW 5V Output ; CTRL2 =⌈M⌋						
Output voltage 1	V_O7	I_O7 = 1mA, I_O1, I_O8 = 0A *5	V_O1-0.25	V_O1		V
Output voltage 2	V_O7’	I_O7 = 200mA, I_O1, I_O8 = 0A *5	V_O1-0.45	V_O1-0.2		V
Output current	I_O7	$V_O7 \geq 4.55$	200			mA
ACC Detection ; ACC Integration 5V output						
ACC detection voltage	$V_{TH}8$		2.8	3.0	3.2	V
Hysteresis width	$V_{HIS}8$		0.2	0.3	0.4	V
Input impedance	ZI8	(Pull-down resistance internal)	42	60	78	kΩ
ACC output voltage 1	V_O8	I_O8 = 0.5mA, I_O1, I_O7 = 0A *5	V_O1-0.25	V_O1		V
ACC output voltage 2	V_O8’	I_O8 = 100mA, I_O1, I_O7 = 0A *5	V_O1-0.45	V_O1-0.2		V
ACC output voltage	I_O8	$V_O8 \geq 4.55$	100			mA

*3 : When a component with a resistance accuracy of ±1% is used

<Reference> When a component with a resistance accuracy of ±0.5% is used, V_O3” is 8.67V ≤ 9.0V ≤ 9.33V.

*4 : When a component with a resistance accuracy of ±1% is used

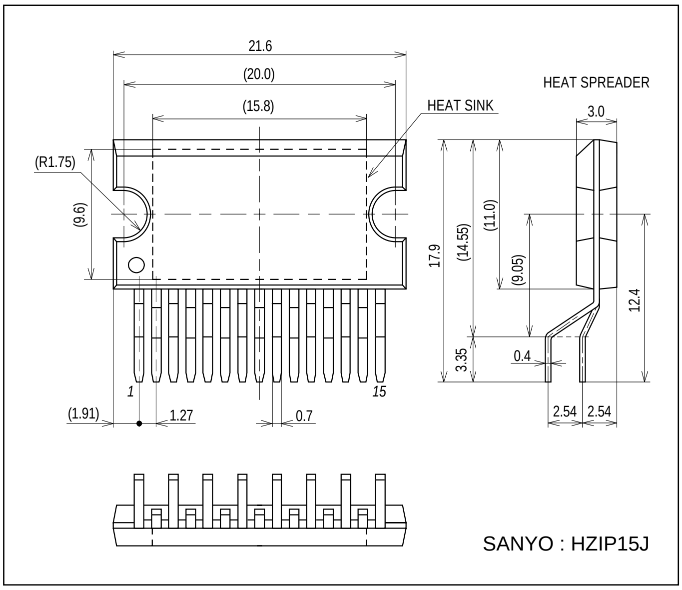
The absolute accuracy of the internal resistance is ±15%.

*5 : Since the SW 5V and ACC 5V are output from V_{DD} 5V through the SW, the voltage drops by an amount equivalent to the ON resistance of the SW.

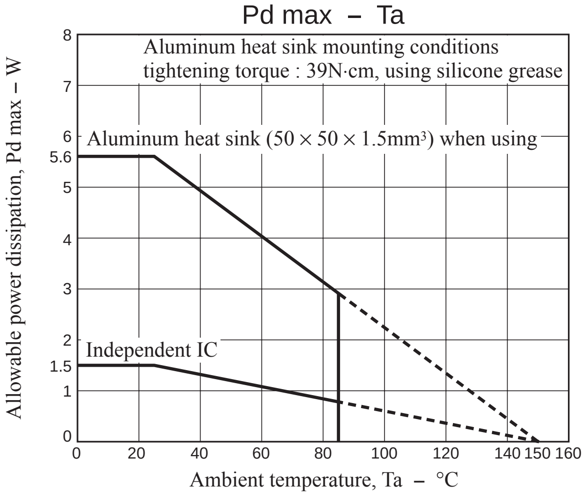
*6: The entire specification has been defined based on the tests performed under the conditions where Tj and Ta (=25°C) are almost equal. There tests were performed with pulse load to minimize the increase of junction temperature (Tj).

Package Dimensions

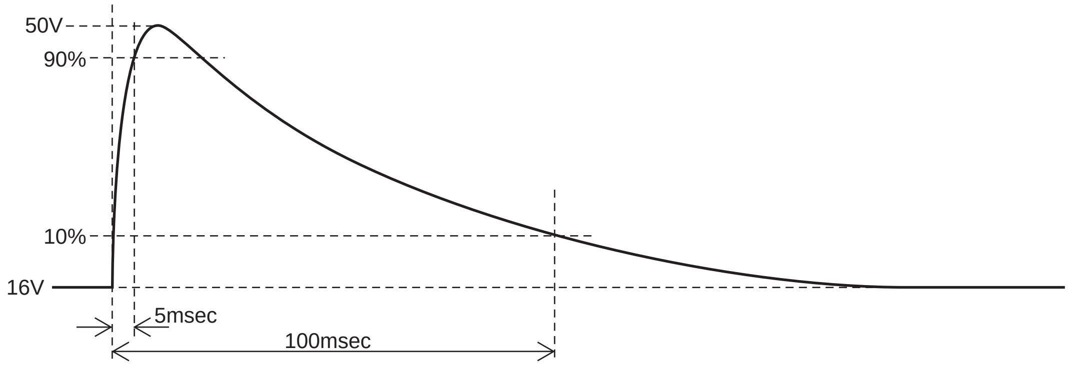
unit : mm (typ)
3395



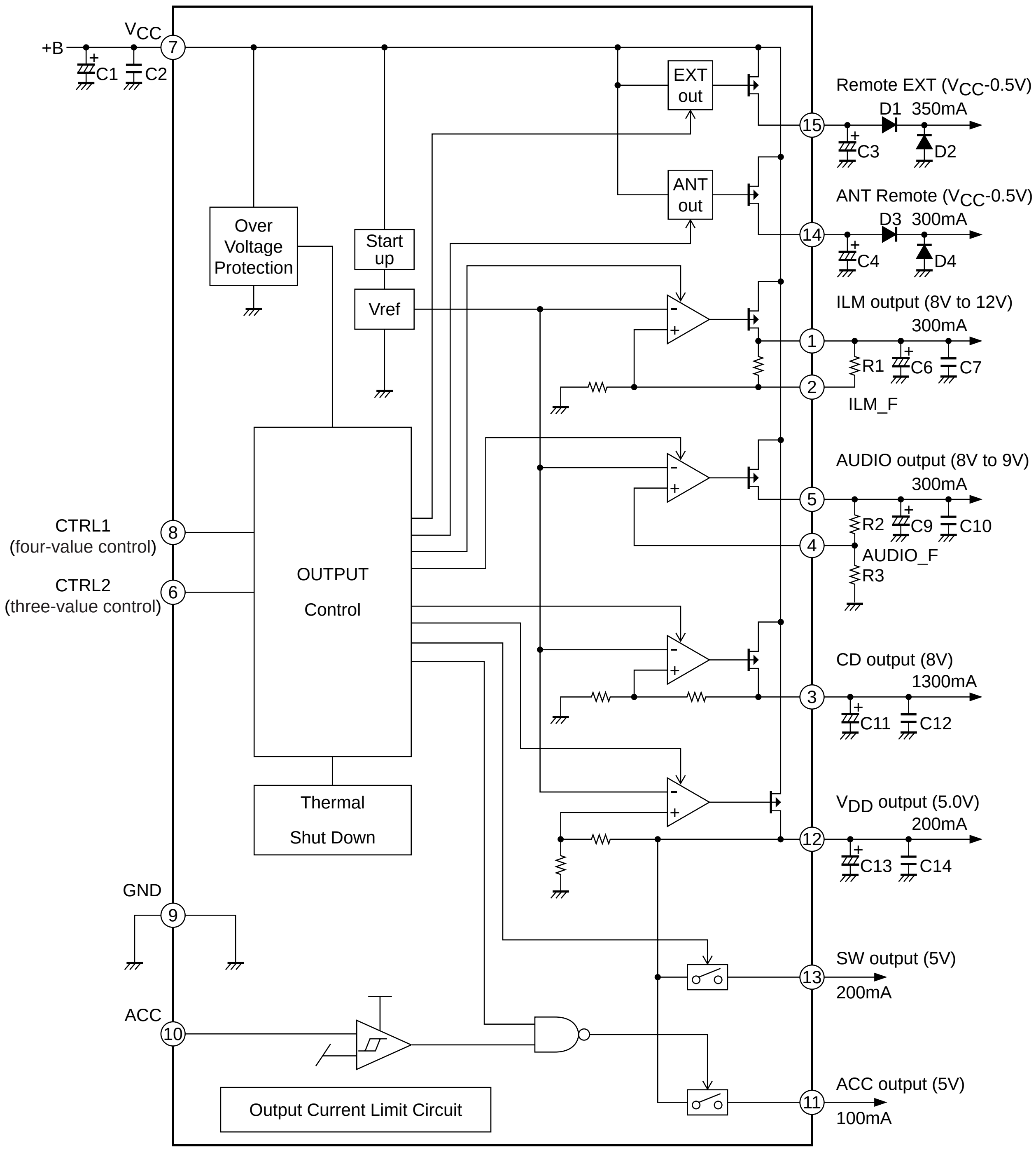
• Allowable power dissipation derating curve



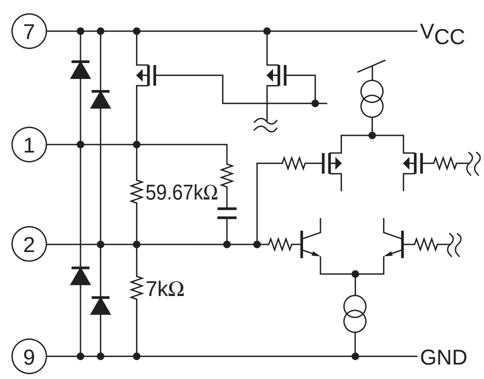
• Waveform applied during surge test



Block Diagram



Pin Function

Pin No.	Pin name	Description	Equivalent Circuit
1	ILM	ILM output pin ON when CTRL1 = M1, M2, H 12.0V/300mA	
2	ILM_F	ILM output voltage adjustment pin	

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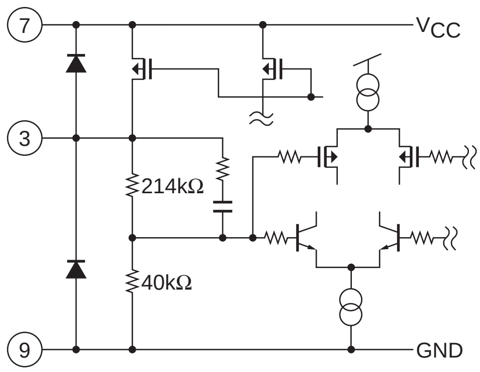
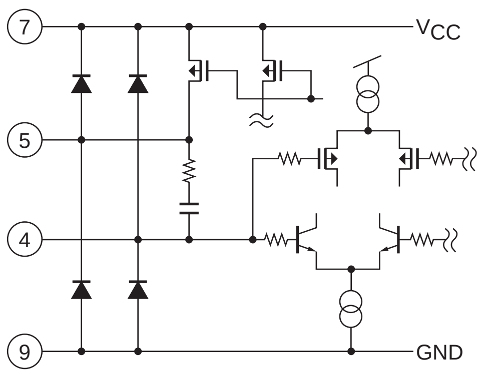
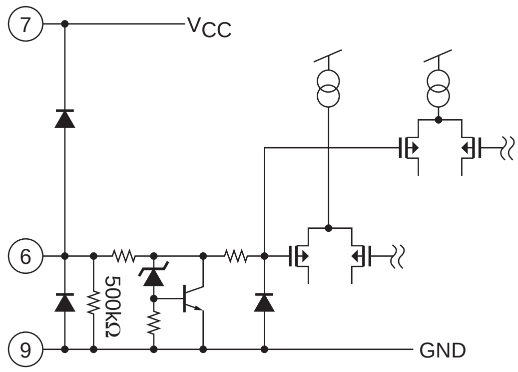
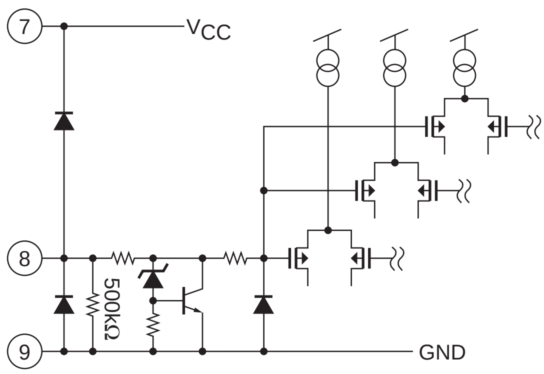
Pin No.	Pin name	Description	Equivalent Circuit
3	CD	CD output pin ON when CTRL2 = M, H 8.0V/1.3A	
4	AUDIO_F	AUIDO output voltage adjustment pin	
5	AUDIO	AUDIO output pin ON when CTRL2 = M, H	
6	CTRL2	CTRL2 input pin three-value input	
7	V_{CC}	Supply terminal	
8	CTRL1	CTRL1 input pin four-value input	
9	GND	GND pin	

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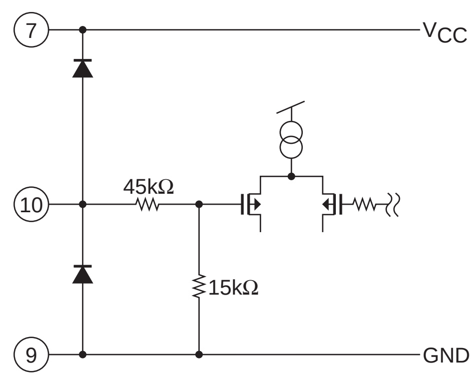
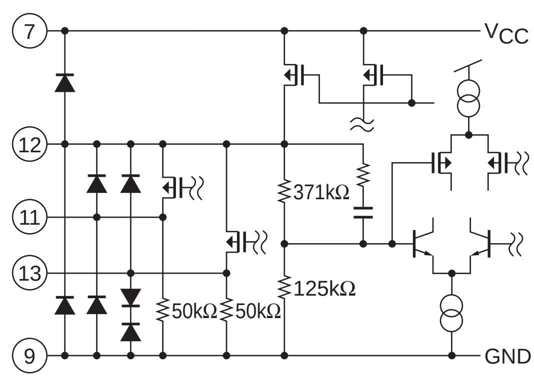
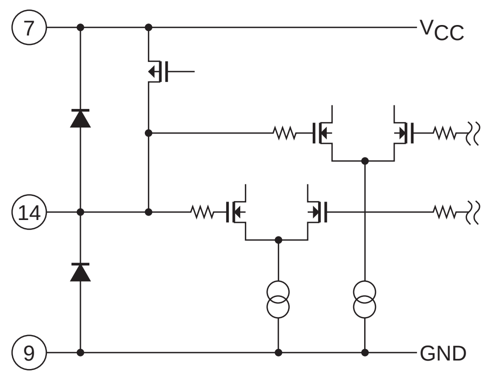
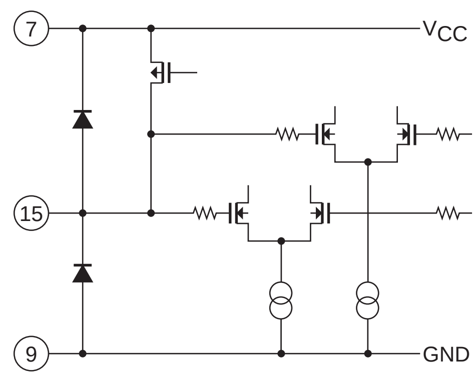
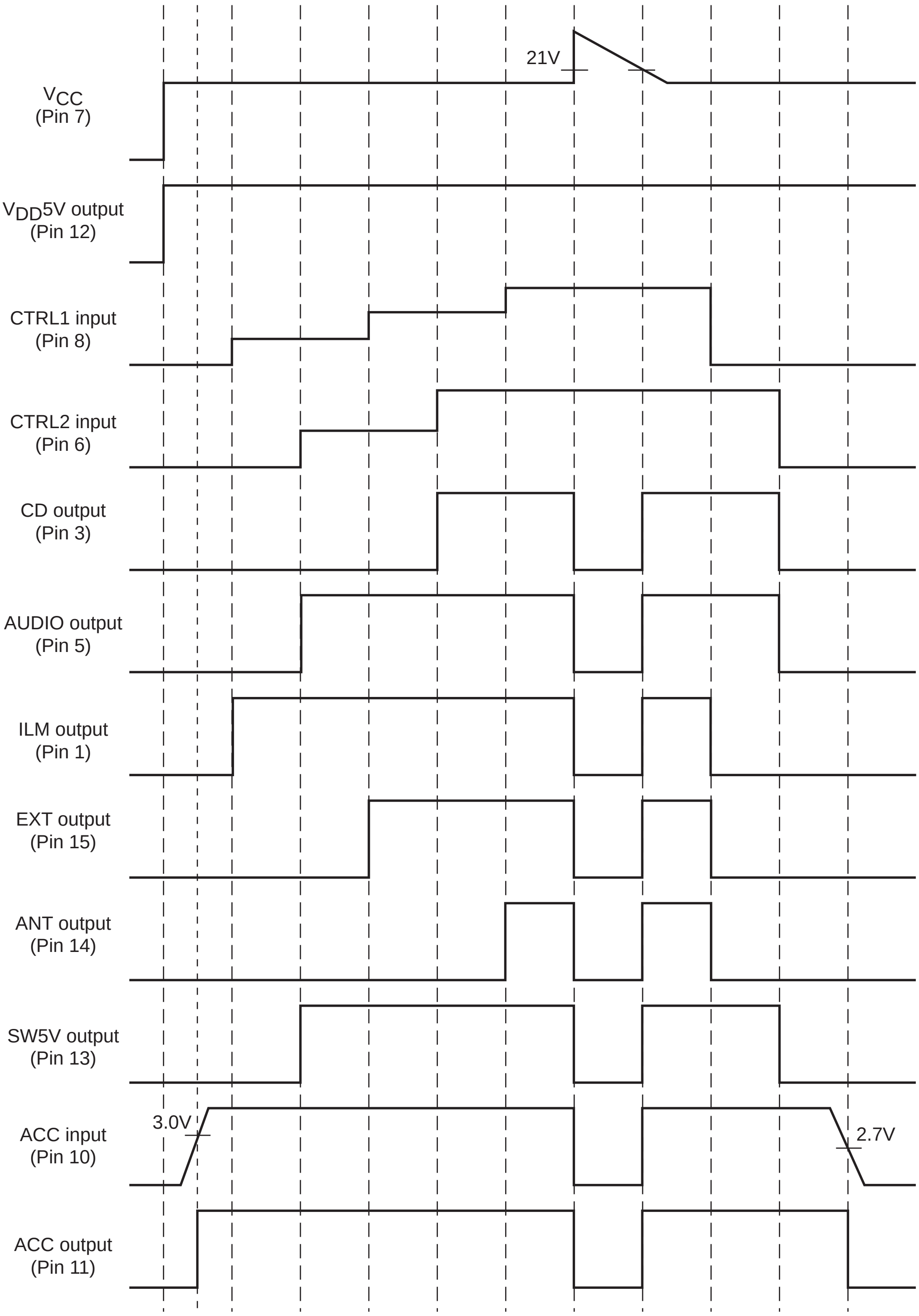
Pin No.	Pin name	Description	Equivalent Circuit
10	ACC	Accessory input	
11	ACC5V	Accessory detection output ON when ACC > 3V	
12	V_{DD}5V	V_{DD}5V output pin 5.0V/200mA	
13	SW5V	SW5V output pin ON when CTRL2 = M, H	
14	ANT	ANT output pin ON when CTRL1 = H V_{CC}-0.5V/300mA	
15	EXT	EXT output pin ON when CTRL1 = M2, H V_{CC}-0.5V/350mA	

CTRL Pin Output Truth Table

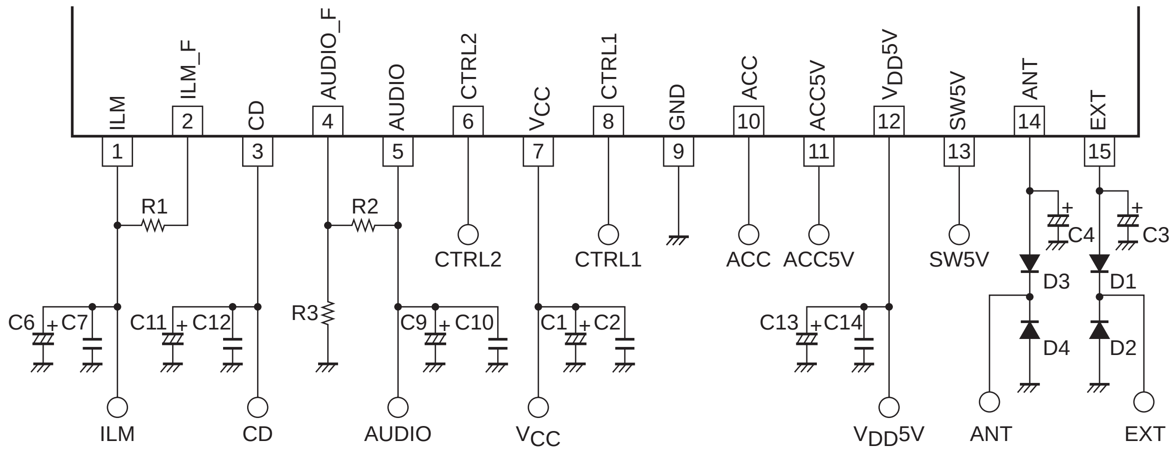
CTRL1	ANT	EXT	ILM
L	OFF	OFF	OFF
M1	OFF	OFF	ON
M2	OFF	ON	ON
H	ON	ON	ON

CTRL2	CD	AUDIO	SW5
L	OFF	OFF	OFF
M	OFF	ON	ON
H	ON	ON	ON

Timing Chart



Recommended Operation Circuit

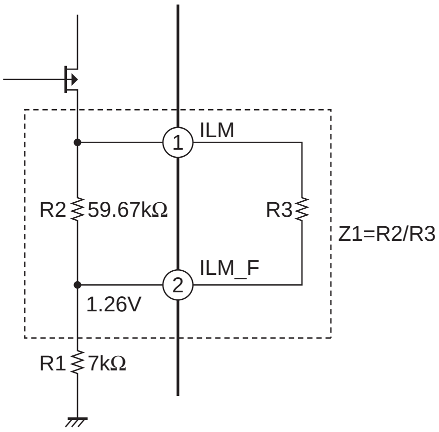


Peripheral parts list

Name of part	Description	Recommended value	Remarks
C1	Power supply bypass capacitor	100μF or more	These capacitors must be placed near the V_{CC} and GND pins.
C2	Oscillation prevention capacitor	0.22μF or more	
C3	EXT output stabilization capacitor	2.2μF or more	
C4	ANT output stabilization capacitor	2.2μF or more	
C6, C9, C11, C13	Output stabilization capacitor	4.7μF or more	Electrolytic capacitor *
C7, C10, C12, C14	Output stabilization capacitor	0.22μF or more	Ceramic capacitor *
R1	Resistor for ILM voltage adjustment	ILM output voltage R1:without = 12.0V :270kΩ = 10.0V :100kΩ = 8.0V	A resistor with resistance accuracy as low as less than ±1% must be used.
R2, R3	Resistor for AUDIO voltage setting	AUDIO output voltage R2/R3:30kΩ/5.6kΩ = 8.0V :27kΩ/4.7kΩ = 8.5V :24kΩ/3.9kΩ = 9.0V	A resistor with resistance accuracy as low as less than ±1% must be used.
D1, D2, D3, D4	Diode for internal device breakdown protection		

* : In order to stabilize the regulator outputs, it is recommended that the electrolytic capacitor and ceramic capacitor be connected in parallel. Furthermore, the values listed above do not guarantee stabilization during the overcurrent protection operations of the regulator, so oscillation may occur during an overcurrent protection operation.

• ILM output voltage setting method



The ILM_F voltage is determined by the internal band gap voltage of the IC (typ = 1.26V).

Formula for ILM voltage calculation

$$Z_1 = R_2//R_3 = \frac{R_2 \cdot R_3}{R_2 + R_3}$$

$$ILM = \frac{1.26[V]}{R_1} \times Z_1 + 1.26[V]$$

$$Z_1 = \frac{(ILM - 1.26) \cdot R_1}{1.26} \qquad R_3 = \frac{R_2 \cdot Z_1}{R_2 - Z_1}$$

Example : ILM = 9V setting method

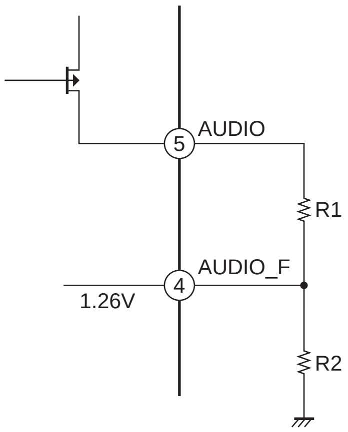
$$Z_1 = \frac{(9V - 1.26V) \cdot 7k\Omega}{1.26V} \cong 43k\Omega$$

When R3 = 150k, the ILM output voltage will be as follows:

$$Z_1' = \frac{59.67k\Omega \cdot 150k\Omega}{59.67k\Omega + 150k\Omega} \cong 42.69k\Omega$$

$$ILM = \frac{1.26V}{7k\Omega} \times 42.69k\Omega + 1.26V \cong \boxed{8.94V}$$

• AUDIO output voltage setting method



The AUDIO_F voltage is determined by the internal band gap voltage of the IC (typ = 1.26V).

Formula for AUDIO voltage calculation

$$AUDIO = \frac{1.26[V]}{R_2} \times R_1 + 1.26[V]$$

$$\frac{R_1}{R_2} = \frac{(AUDIO - 1.26)}{1.26}$$

The circuit must be designed in such a way that the R1:R2 ratio satisfies the formula given above for the AUDIO voltage that has been set.

Example : AUDIO = 8.5V setting method

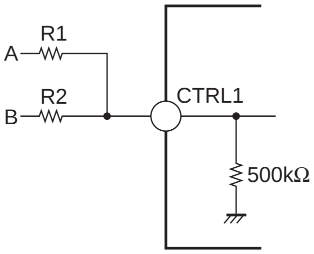
$$\frac{R_1}{R_2} = \frac{(8.5 - 1.26)}{1.26} \cong 5.75$$

$$\frac{R_1}{R_2} = \frac{27k\Omega}{4.7k\Omega} \cong 5.74$$

$$AUDIO = 1.26V \times 5.74 + 1.26V \cong \boxed{8.49V}$$

Note : In the above, the typical values are given in all instances for the values used and, as such, they will vary due to the effects of production-related variations of the IC and external resistors.

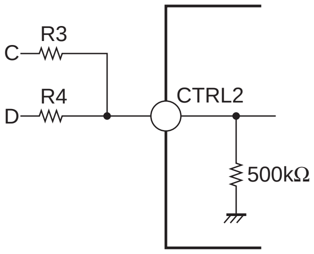
• CTRL1 Application Circuit Example



(1) 3.3V input: R1 = 4.7kΩ, R2 = 10kΩ

A	B	CTRL1
0V	0V	0V
0V	3.3V	1.05V
3.3V	0V	2.23V
3.3V	3.3V	3.20V

• CTRL2 Application Circuit Example



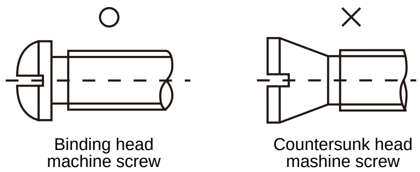
(1) 3.3V input: R3 = R4 = 4.7kΩ

A	B	CTRL2
0V	0V	0V
0V	3.3V	1.61V
3.3V	0V	1.61V
3.3V	3.3V	3.29V

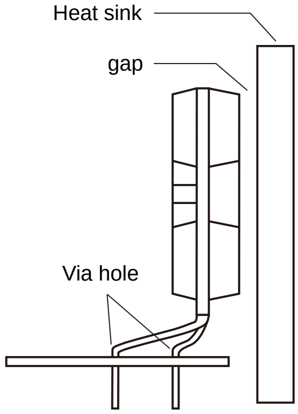
HZIP15J Heat sink attachment

Heat sinks are used to lower the semiconductor device junction temperature by leading the head generated by the device to the outer environment and dissipating that heat.

a. Unless otherwise specified, for power ICs with tabs and power ICs with attached heat sinks, solder must not be applied to the heat sink or tabs.



b. Heat sink attachment
 · Use flat-head screws to attach heat sinks.
 · Use also washer to protect the package.
 · Use tightening torques in the ranges 39-59Ncm(4-6kgcm) .
 · If tapping screws are used, do not use screws with a diameter larger than the holes in the semiconductor device itself.
 · Do not make gap, dust, or other contaminants to get between the semiconductor device and the tab or heat sink.
 · Take care a position of via hole .
 · Do not allow dirt, dust, or other contaminants to get between the semiconductor device and the tab or heat sink.
 · Verify that there are no press burrs or screw-hole burrs on the heat sink.
 · Warping in heat sinks and printed circuit boards must be no more than 0.05 mm between screw holes, for either concave or convex warping.
 · Twisting must be limited to under 0.05 mm.
 · Heat sink and semiconductor device are mounted in parallel.
 Take care of electric or compressed air drivers
 · The speed of these torque wrenches should never exceed 700 rpm, and should typically be about 400 rpm.



c. Silicone grease
 · Spread the silicone grease evenly when mounting heat sinks.
 · Sanyo recommends YG-6260 (Momentive Performance Materials Japan LLC)

d. Mount
 · First mount the heat sink on the semiconductor device, and then mount that assembly on the printed circuit board.
 · When attaching a heat sink after mounting a semiconductor device into the printed circuit board, when tightening up a heat sink with the screw, the mechanical stress which is impossible to the semiconductor device and the pin doesn't hang.

e. When mounting the semiconductor device to the heat sink using jigs, etc.,
 · Take care not to allow the device to ride onto the jig or positioning dowel.
 · Design the jig so that no unreasonable mechanical stress is not applied to the semiconductor device.

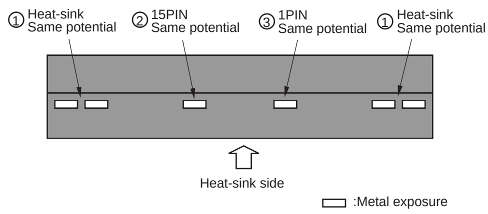
f. Heat sink screw holes
 · Be sure that chamfering and shear drop of heat sinks must not be larger than the diameter of screw head used.
 · When using nuts, do not make the heat sink hole diameters larger than the diameter of the head of the screws used. A hole diameter about 15% larger than the diameter of the screw is desirable.
 · When tap screws are used, be sure that the diameter of the holes in the heat sink are not too small. A diameter about 15% smaller than the diameter of the screw is desirable.

g. There is a method to mount the semiconductor device to the heat sink by using a spring band. But this method is not recommended because of possible displacement due to fluctuation of the spring force with time or vibration.

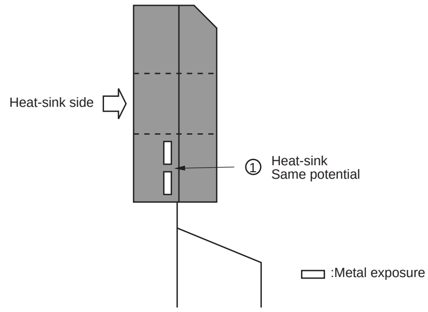
Caution for implementing LV5680P to a system board

The package of LV5680P is HZIP15J which has some metal exposures other than connection pins and heatsink as shown in the diagram below. The electrical potentials of (2) and (3) are the same as those of pin 15 and pin 1, respectively. (2) (=pin 15) is the V_{CC} pin and (3) (=pin 1) is the ILM (regulator) output pin. When you implement the IC to the set board, make sure that the bolts and the heatsink are out of touch from (2) and (3). If the metal exposures touch the bolts which has the same electrical potential with GND, GND short occurs in ILM output and V_{CC}. The exposures of (1) are connected to heatsink which has the same electrical potential with substrate of the IC chip (GND). Therefore, (1) and GND electrical potential of the set board can connect each other.

• HZIP15J outline

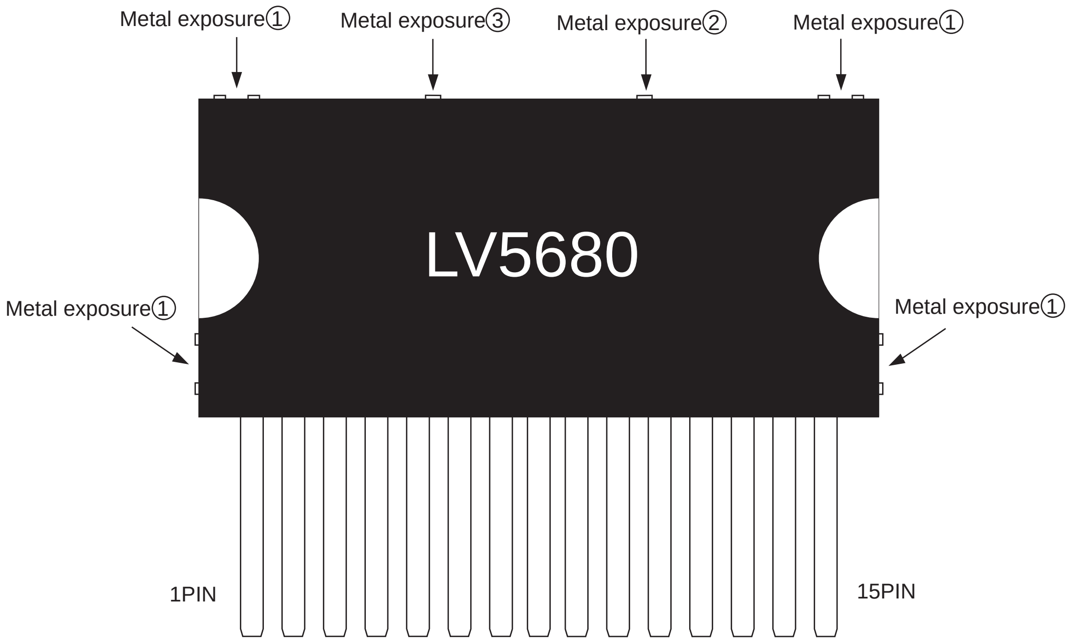


<Top view of HZIP15J>



<Side view of HZIP15J>

• Frame diagram (LV5680P) *In the system power supply other than LV5680P, pin assignment may differ.



This catalog provides information as of October, 2011. Specifications and information herein are subject to change without notice.