



# PMDPB58UPE

20 V dual P-channel Trench MOSFET

3 February 2016

Product data sheet

## 1. General description

Dual small-signal P-channel enhancement mode Field-Effect Transistor (FET) in a leadless medium power DFN2020-6 (SOT1118) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

## 2. Features and benefits

- Low threshold voltage
- Very fast switching
- Trench MOSFET technology
- 2 kV ElectroStatic Discharge (ESD) protection

## 3. Applications

- Relay driver
- High-speed line driver
- High-side load switch
- Switching circuits

## 4. Quick reference data

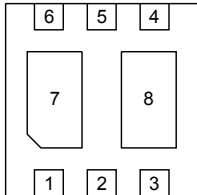
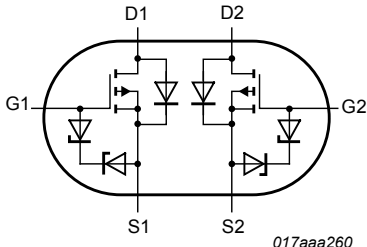
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Per transistor</b>						
$V_{DS}$	drain-source voltage	$T_j = 25\text{ °C}$	-	-	-20	V
$V_{GS}$	gate-source voltage		-8	-	8	V
$I_D$	drain current	$V_{GS} = -4.5\text{ V}; T_{amb} = 25\text{ °C}; t \leq 5\text{ s}$	[1]	-	-4.5	A
<b>Static characteristics (per transistor)</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = -4.5\text{ V}; I_D = -2\text{ A}; T_j = 25\text{ °C}$	-	58	67	m $\Omega$

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm<sup>2</sup>.

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source TR1	 <p>Transparent top view <b>DFN2020-6 (SOT1118)</b></p>	 <p>017aaa260</p>
2	G1	gate TR1		
3	D2	drain TR2		
4	S2	source TR2		
5	G2	gate TR2		
6	D1	drain TR1		
7	D1	drain TR1		
8	D2	drain TR2		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMDPB58UPE	DFN2020-6	DFN2020-6: plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals; body 2 x 2 x 0.65 mm	SOT1118

## 7. Marking

Table 4. Marking codes

Type number	Marking code
PMDPB58UPE	2A

## 8. Limiting values

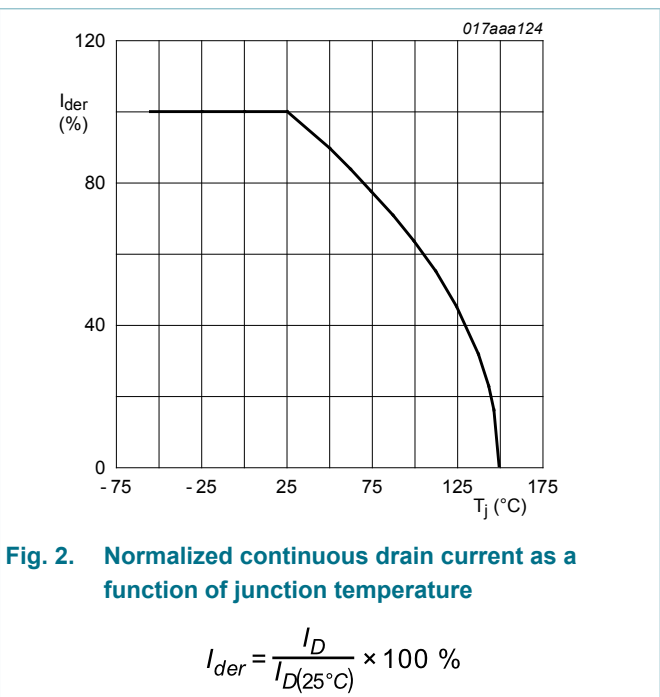
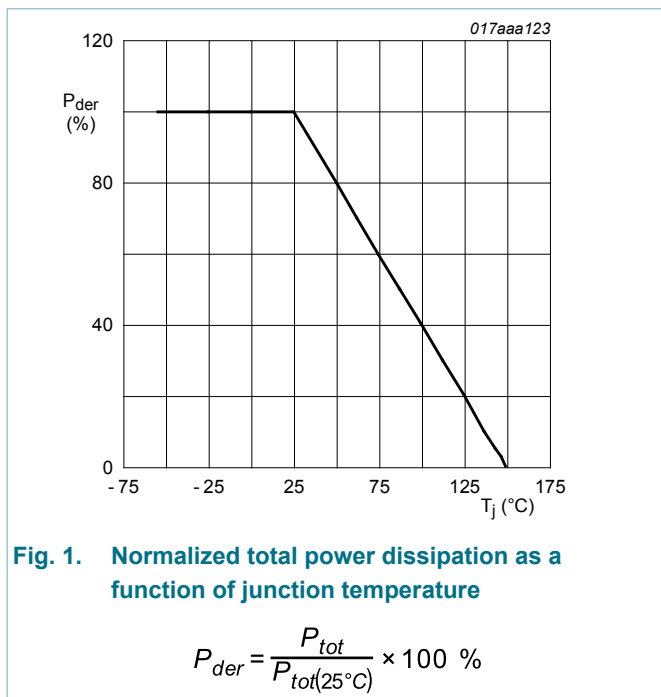
Table 5. Limiting values

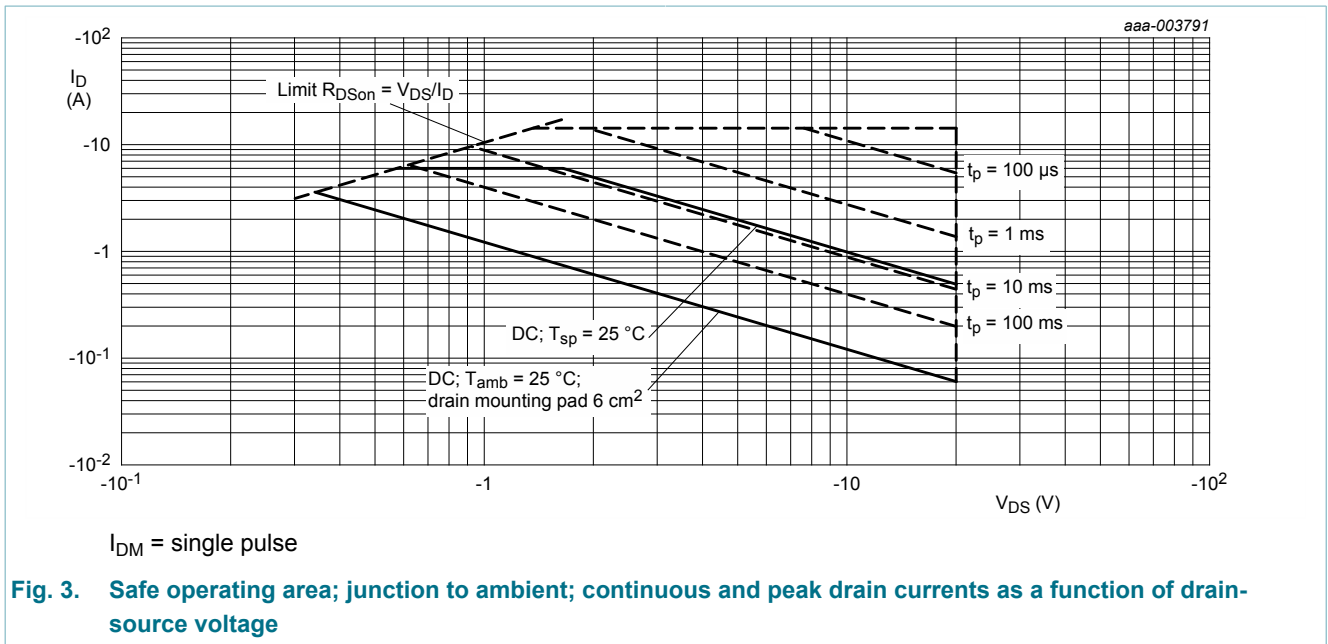
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
<b>Per transistor</b>						
$V_{DS}$	drain-source voltage	$T_j = 25\text{ °C}$	-	-20	V	
$V_{GS}$	gate-source voltage		-8	8	V	
$I_D$	drain current	$V_{GS} = -4.5\text{ V}; T_{amb} = 25\text{ °C}; t \leq 5\text{ s}$	[1]	-	-4.5	A
		$V_{GS} = -4.5\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	-3.6	A
		$V_{GS} = -4.5\text{ V}; T_{amb} = 100\text{ °C}$	[1]	-	-2.3	A

Symbol	Parameter	Conditions		Min	Max	Unit
I <sub>DM</sub>	peak drain current	T <sub>amb</sub> = 25 °C; single pulse; t <sub>p</sub> ≤ 10 μs		-	-14.4	A
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = 25 °C	[2]	-	515	mW
			[1]	-	1210	mW
		T <sub>sp</sub> = 25 °C		-	8330	mW
<b>Per device</b>						
T <sub>j</sub>	junction temperature			-55	150	°C
T <sub>amb</sub>	ambient temperature			-55	150	°C
T <sub>stg</sub>	storage temperature			-65	150	°C
<b>Source-drain diode</b>						
I <sub>S</sub>	source current	T <sub>amb</sub> = 25 °C	[1]	-	-1.3	A
<b>ESD maximum rating</b>						
V <sub>ESD</sub>	electrostatic discharge voltage	HBM; C = 100 pF; R = 1.5 kΩ	[3]	-	2000	V

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm<sup>2</sup>.
- [2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.
- [3] Measured between all pins.





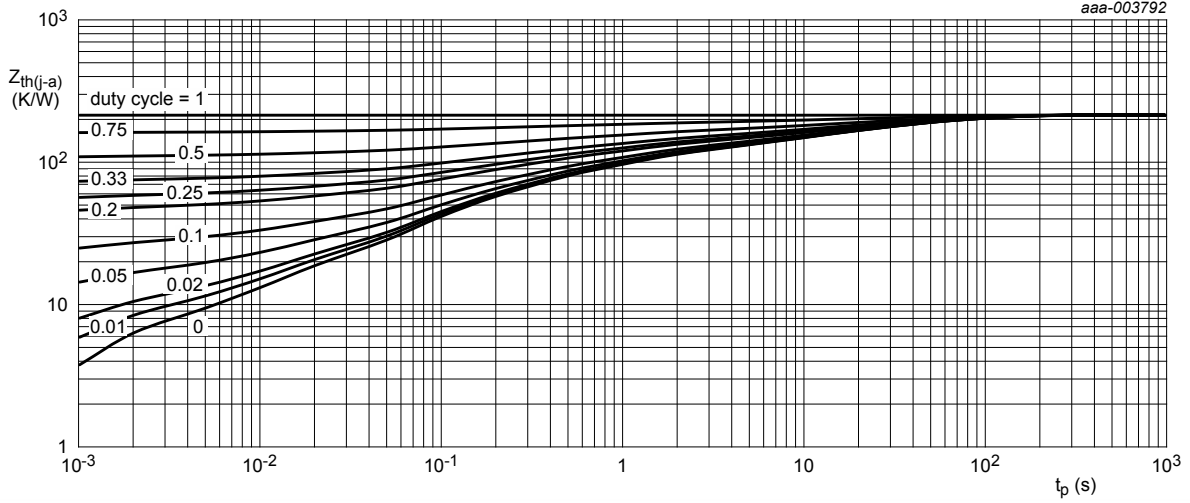
## 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
<b>Per transistor</b>							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	212	244	K/W
			[2]	-	90	104	K/W
		in free air; $t \leq 5\text{ s}$	[2]	-	55	64	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	11	15	K/W

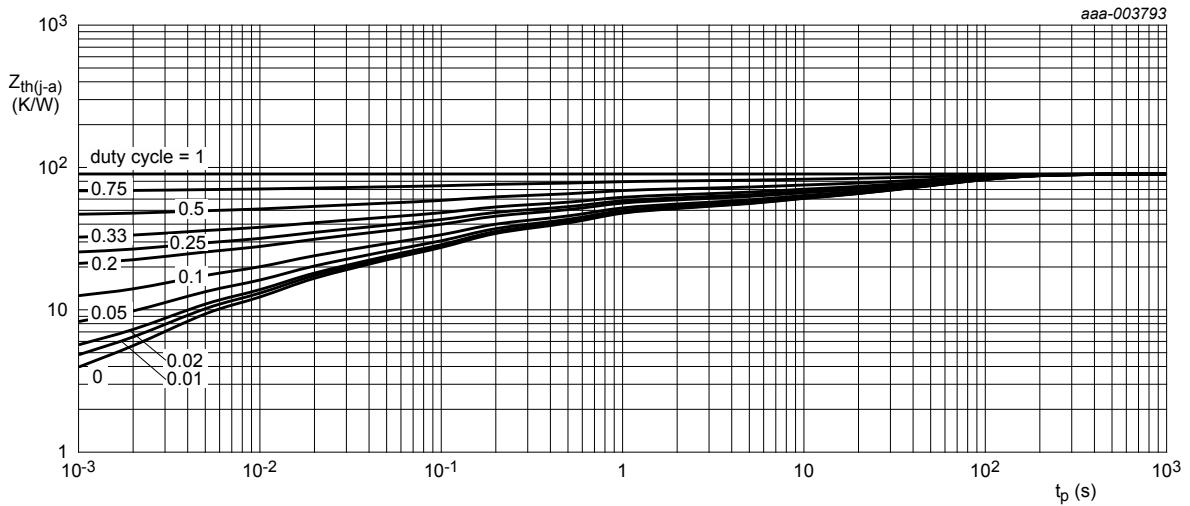
[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain  $6\text{ cm}^2$ .



FR4 PCB, standard footprint

**Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values**



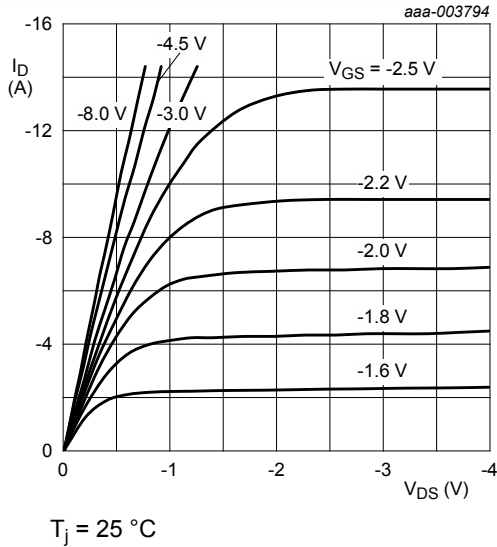
FR4 PCB, mounting pad for drain 6 cm<sup>2</sup>

**Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values**

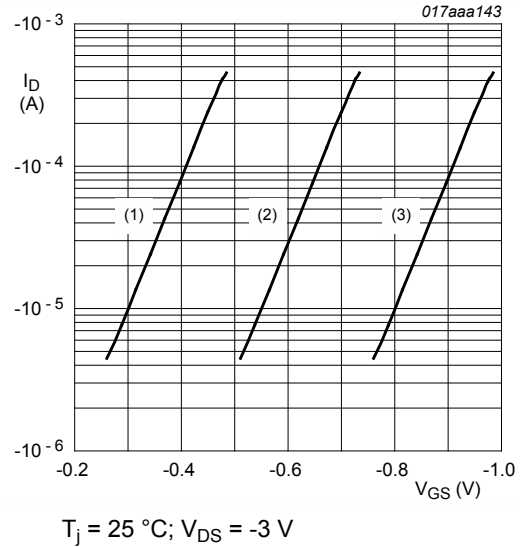
## 10. Characteristics

Table 7. Characteristics

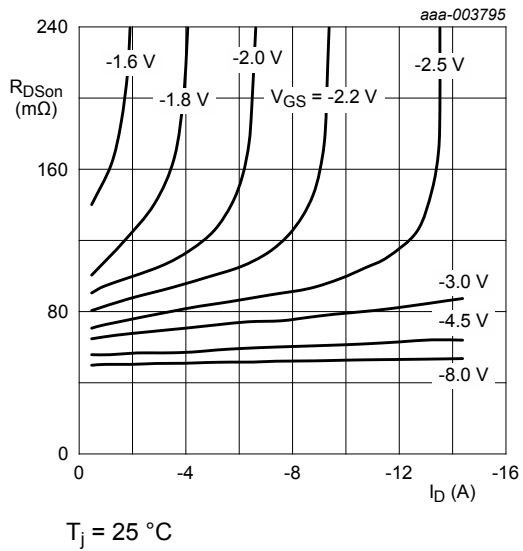
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics (per transistor)</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = -250 \mu A$ ; $V_{GS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$	-20	-	-	V
$V_{GSth}$	gate-source threshold voltage	$I_D = -250 \mu A$ ; $V_{DS} = V_{GS}$ ; $T_j = 25 \text{ }^\circ C$	-0.45	-0.7	-0.95	V
$I_{DSS}$	drain leakage current	$V_{DS} = -20 V$ ; $V_{GS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$	-	-	-1	$\mu A$
		$V_{DS} = -20 V$ ; $V_{GS} = 0 V$ ; $T_j = 150 \text{ }^\circ C$	-	-	-10	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 8 V$ ; $V_{DS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$	-	-	10	$\mu A$
		$V_{GS} = -8 V$ ; $V_{DS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$	-	-	-10	$\mu A$
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = -4.5 V$ ; $I_D = -2 A$ ; $T_j = 25 \text{ }^\circ C$	-	58	67	m $\Omega$
		$V_{GS} = -4.5 V$ ; $I_D = -2 A$ ; $T_j = 150 \text{ }^\circ C$	-	82	95	m $\Omega$
		$V_{GS} = -2.5 V$ ; $I_D = -1.5 A$ ; $T_j = 25 \text{ }^\circ C$	-	74	95	m $\Omega$
		$V_{GS} = -1.8 V$ ; $I_D = -1 A$ ; $T_j = 25 \text{ }^\circ C$	-	97	137	m $\Omega$
$g_{fs}$	forward transconductance	$V_{DS} = -10 V$ ; $I_D = -2 A$ ; $T_j = 25 \text{ }^\circ C$	-	9	-	S
<b>Dynamic characteristics (per transistor)</b>						
$Q_{G(tot)}$	total gate charge	$V_{DS} = -10 V$ ; $I_D = -2 A$ ; $V_{GS} = -4.5 V$ ; $T_j = 25 \text{ }^\circ C$	-	6.3	9.5	nC
$Q_{GS}$	gate-source charge		-	1.2	-	nC
$Q_{GD}$	gate-drain charge		-	0.9	-	nC
$C_{iss}$	input capacitance	$V_{DS} = -10 V$ ; $f = 1 \text{ MHz}$ ; $V_{GS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$	-	804	-	pF
$C_{oss}$	output capacitance		-	95	-	pF
$C_{rss}$	reverse transfer capacitance		-	66	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = -10 V$ ; $I_D = -2 A$ ; $V_{GS} = -4.5 V$ ; $R_{G(ext)} = 6 \Omega$ ; $T_j = 25 \text{ }^\circ C$	-	7	-	ns
$t_r$	rise time		-	15	-	ns
$t_{d(off)}$	turn-off delay time		-	41	-	ns
$t_f$	fall time		-	14	-	ns
<b>Source-drain diode (per transistor)</b>						
$V_{SD}$	source-drain voltage	$I_S = -0.5 A$ ; $V_{GS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$	-	-0.7	-1.2	V



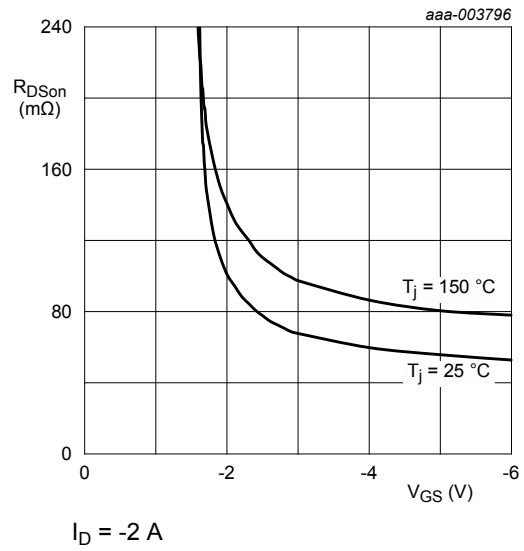
**Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values**



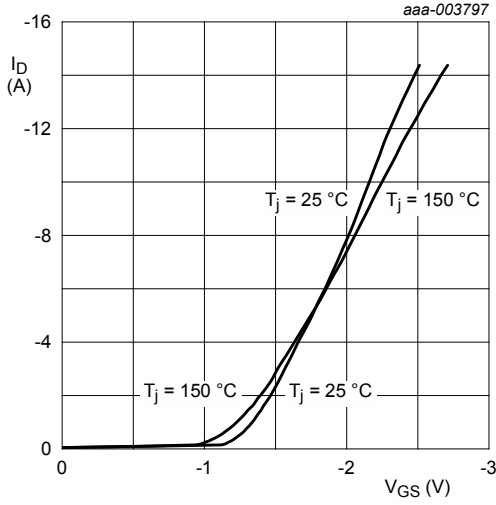
**Fig. 7. Sub-threshold drain current as a function of gate-source voltage**  
 (1) minimum values  
 (2) typical values  
 (3) maximum values



**Fig. 8. Drain-source on-state resistance as a function of drain current; typical values**

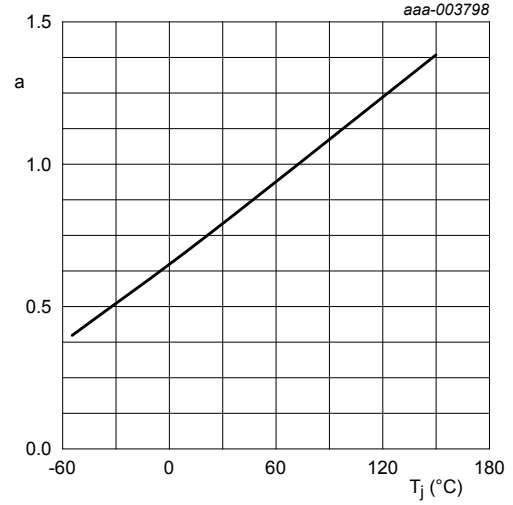


**Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values**



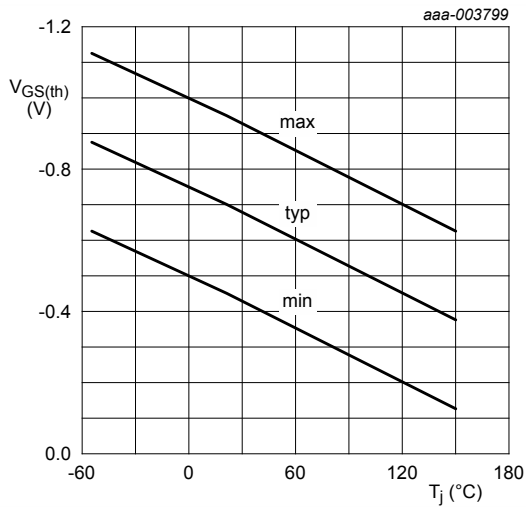
$$V_{DS} > I_D \times R_{DSon}$$

**Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values**



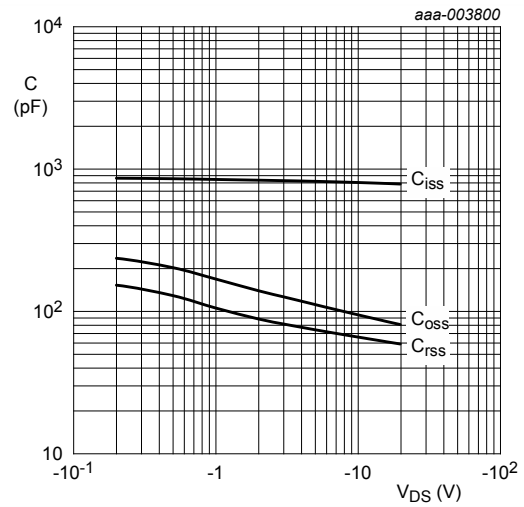
**Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values**

$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$$



$$I_D = -0.25 \text{ mA}; V_{DS} = V_{GS}$$

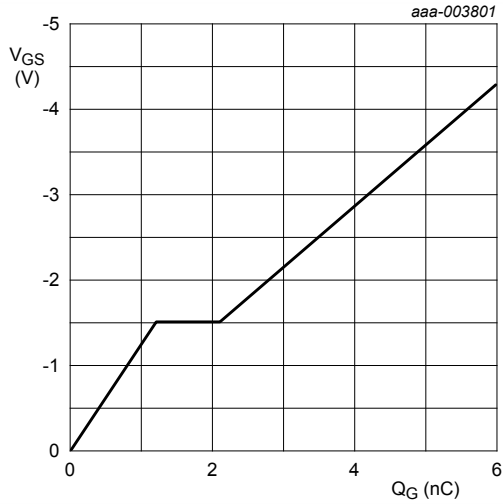
**Fig. 12. Gate-source threshold voltage as a function of junction temperature**



$$f = 1 \text{ MHz}; V_{GS} = 0 \text{ V}$$

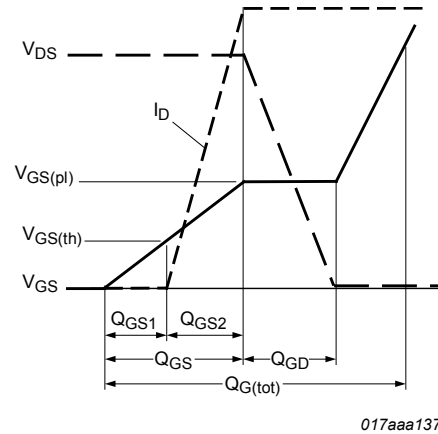
**Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**



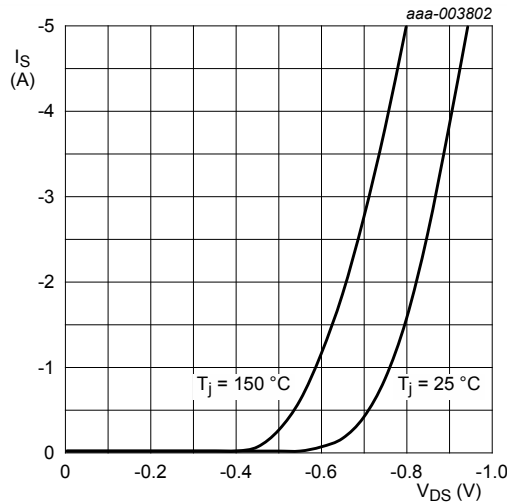


$I_D = -2 \text{ A}; V_{DS} = -10 \text{ V}; T_{amb} = 25 \text{ }^\circ\text{C}$

**Fig. 14. Gate-source voltage as a function of gate charge; typical values**



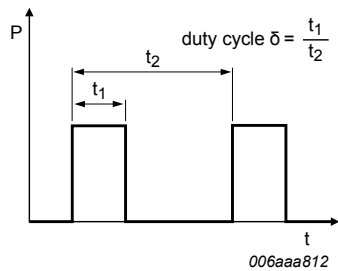
**Fig. 15. Gate charge waveform definitions**



$V_{GS} = 0 \text{ V}$

**Fig. 16. Source current as a function of source-drain voltage; typical values**

## 11. Test information



**Fig. 17. Duty cycle definition**

### 12. Package outline

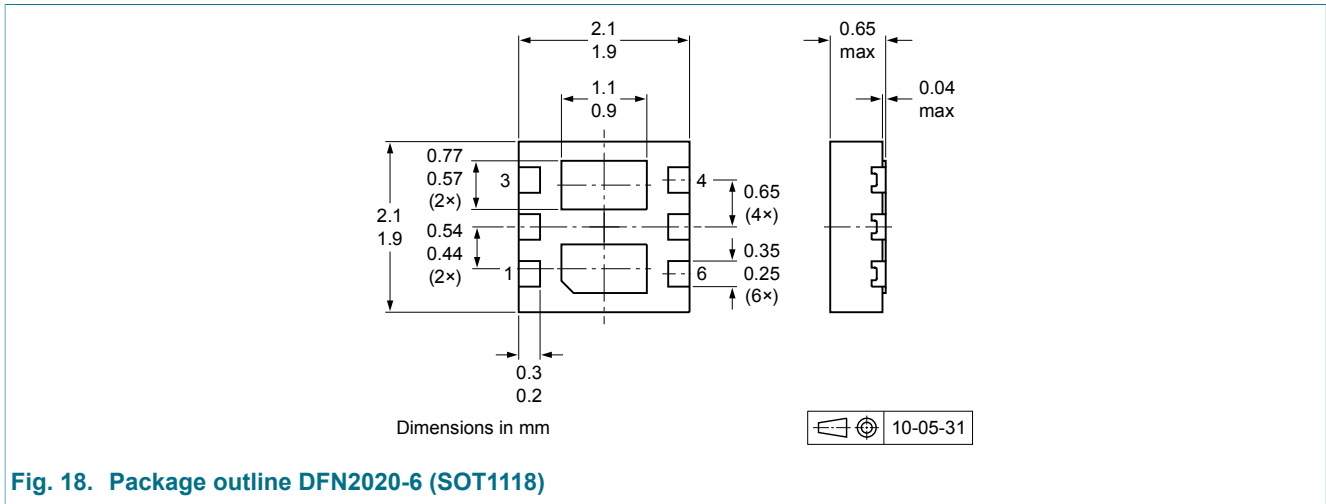


Fig. 18. Package outline DFN2020-6 (SOT1118)

### 13. Soldering

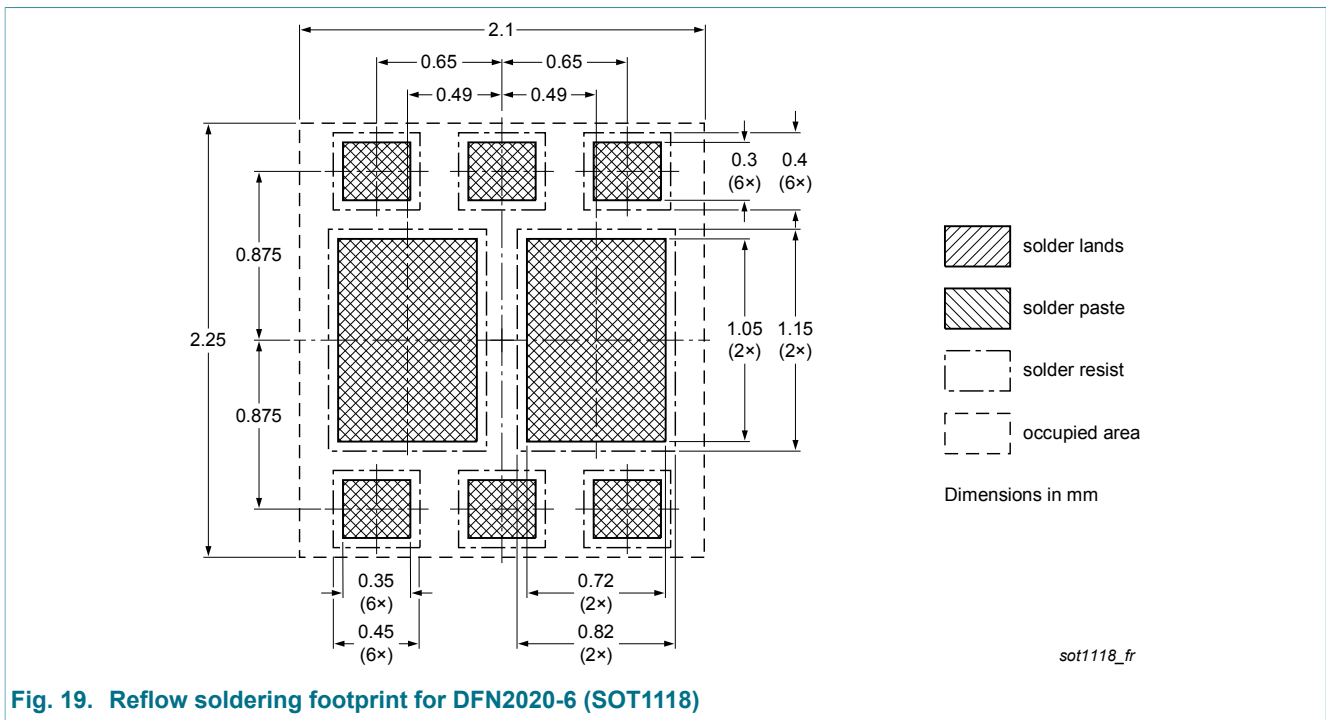


Fig. 19. Reflow soldering footprint for DFN2020-6 (SOT1118)

## 14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMDPB58UPE v.2	20160203	Product data sheet	-	PMDPB58UPE v.1
Modifications:	• Figure 9: corrected			
PMDPB58UPE v.1	20120619	Product data sheet	-	-

## 15. Legal information

### 15.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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