ESDALC5-1BM2, ESDALC5-1BT2

Single line low capacitance Transil™, transient surge voltage suppressor (TVS) for ESD protection

Datasheet - production data

Features

- Single line low capacitance Transil diode
- Bidirectional ESD protection
- Breakdown voltage V_{BR} = 5.8 V min
- Low diode capacitance (26 pF typ. at 0 V)
- Low leakage current < 60 nA at 5 V
- Very small PCB area: 0.6 mm²

Applications

Where transient overvoltage protection in ESD sensitive equipment is required, such as:

- Computers
- Printers
- Communication systems
- Cellular phone handsets and accessories
- Video equipment

Benefits

- High ESD protection level
- High integration
- Suitable for high density boards
- Lead-free packages
- ECOPACK®2 compliant components

Complies with the following standards

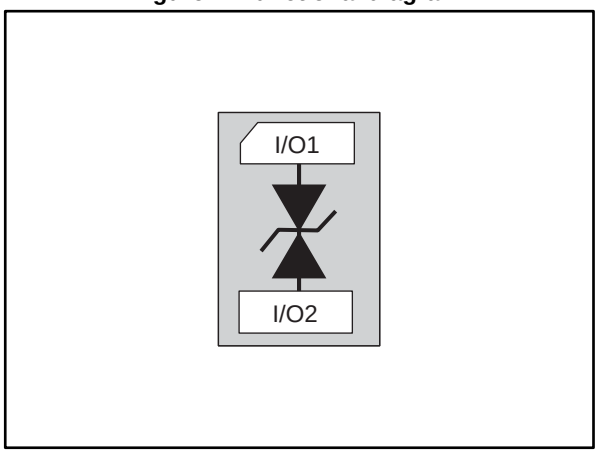
- IEC 61000-4-2 (exceeds level 4)
  - 30 kV (air discharge)
  - 30 kV (contact discharge)
- MIL STD 883G - Method 3015-7: class 3
  - Human body model

Description

The ESDALC5-1BM2 (SOD882) and ESDALC5-1BT2 (SOD882T) are bidirectional single-line TVS diodes designed to protect data lines or other I/O ports against ESD transients.

These devices are ideal for applications where both reduced line capacitance and board space saving are required.

Figure 1: Functional diagram



TM: Transil is a trademark of STMicroelectronics

This is information on a product in full production.

1 Characteristics

Table 1: Absolute maximum ratings (T_{amb} = 25 °C)

Symbol	Parameter		Value	Unit
V_{PP}	Peak pulse voltage	IEC 61000-4-2: Contact discharge Air discharge	 30 30	kV
P_{PP}	Peak pulse power	8/20µs, T_j initial = T_{amb}	150	W
I_{PP}	Peak pulse current	8/20µs	9	A
T_{stg}	Storage temperature range		-65 to +150	°C
T_j	Junction temperature		-55 to +150	
T_L	Maximum lead temperature for soldering during 10 s		260	

Figure 2: Electrical characteristics (definitions)

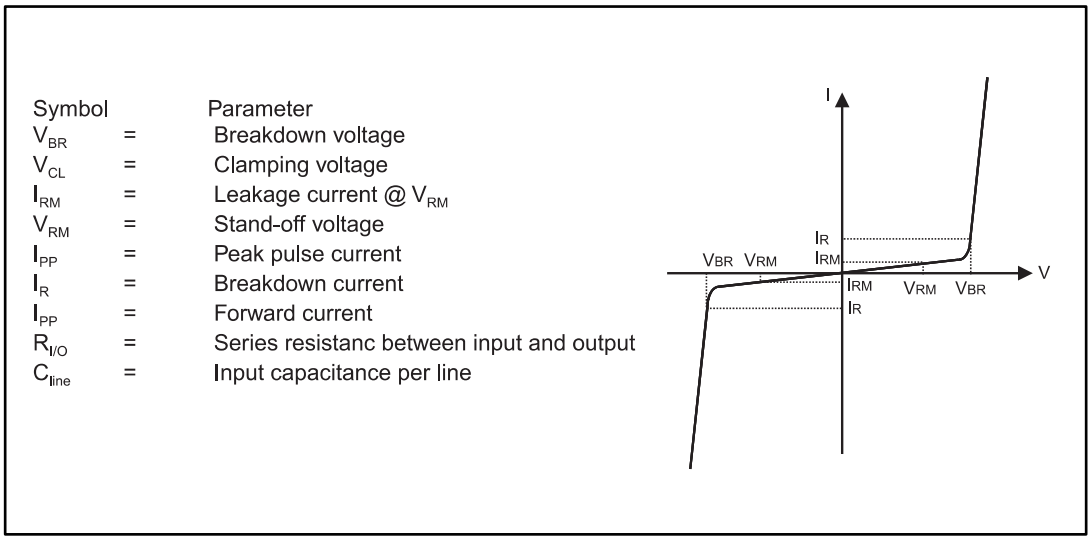


Table 2: Electrical characteristics (T_{amb} = 25 °C)

Symbol	Test condition	Min.	Typ.	Max.	Unit
V_{BR}	From I/O1 to I/O2, IR = 1 mA	11	13	17	V
	From I/O2 to I/O1, IR = 1 mA	5.8	8	11	
I_{RM}	V_{RM} = 5 V			60	nA
R_d	Dynamic resistance, pulse width 100 ns From I/O1 to I/O2 From I/O2 to I/O1		 0.25 0.23		Ω
C_{line}	F = 1 MHz, V_R = 0 V		26	30	pF
V_{CL}	8 kV contact discharge after 30 ns IEC 61000 4-2 From I/O1 to I/O2 From I/O2 to I/O1		 16 11		V

1.1 Characteristics (curves)

Figure 3: Peak pulse power dissipation versus initial junction temperature (maximum values)

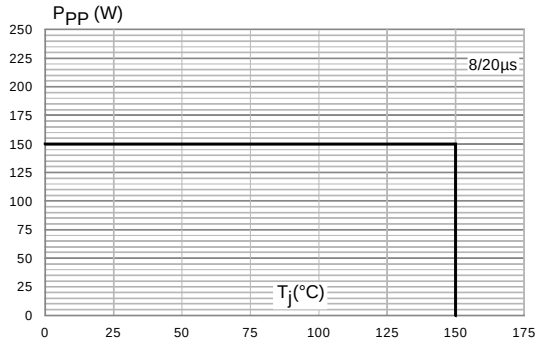


Figure 4: Leakage current versus junction temperature (typical values)

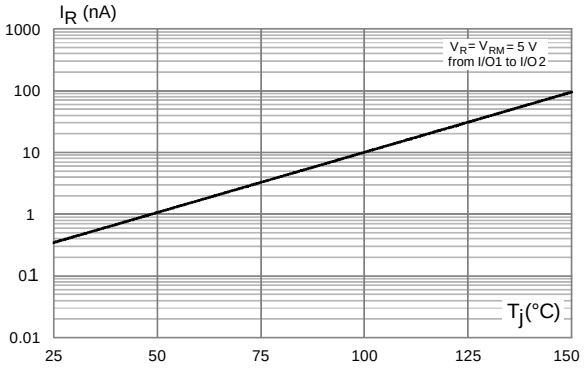


Figure 5: Leakage current versus junction temperature (typical values)

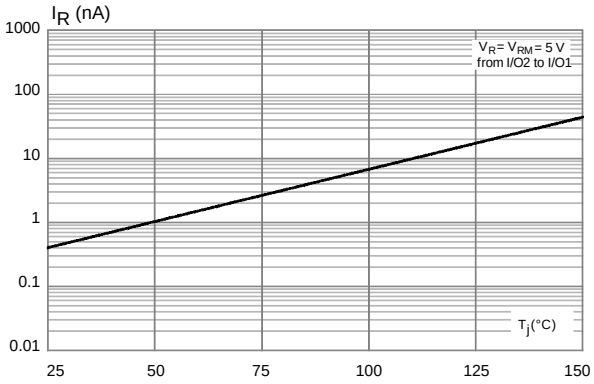


Figure 6: Peak pulse power versus exponential pulse duration (direct)

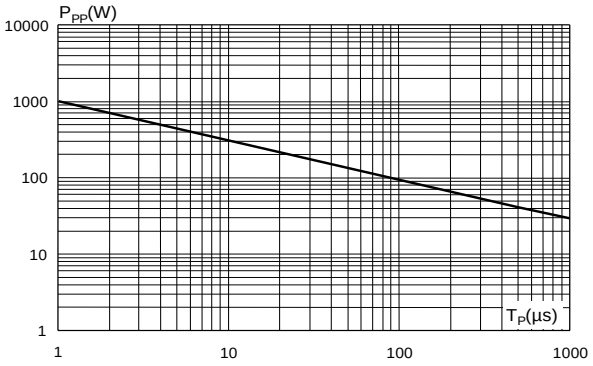


Figure 7: Clamping voltage versus peak pulse current (typical values)

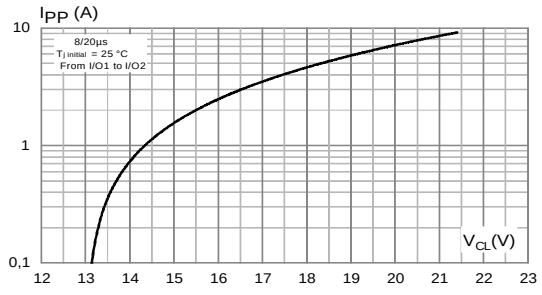


Figure 8: Clamping voltage versus peak pulse current (typical values)

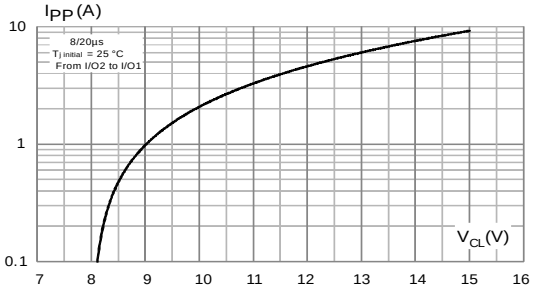


Figure 9: Junction capacitance versus reverse applied voltage (typical values from I/O1 to I/O2)

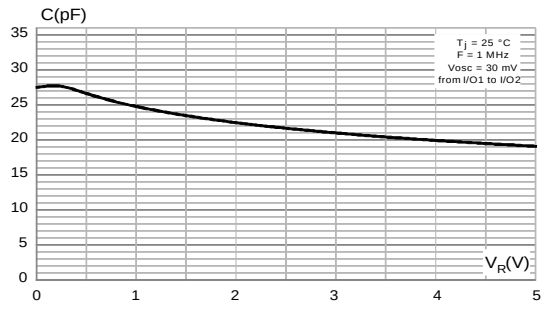


Figure 10: Junction capacitance versus reverse applied voltage (typical values from I/O2 to I/O1)

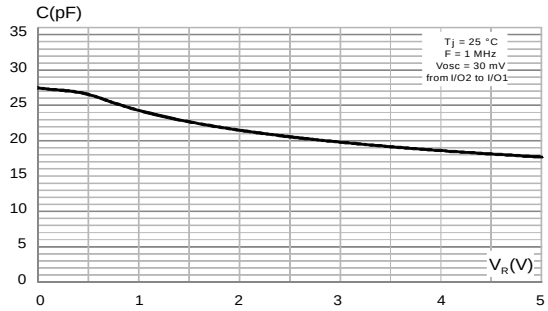


Figure 11: ESD response to IEC 61000-4-2 (+8 kV air discharge)

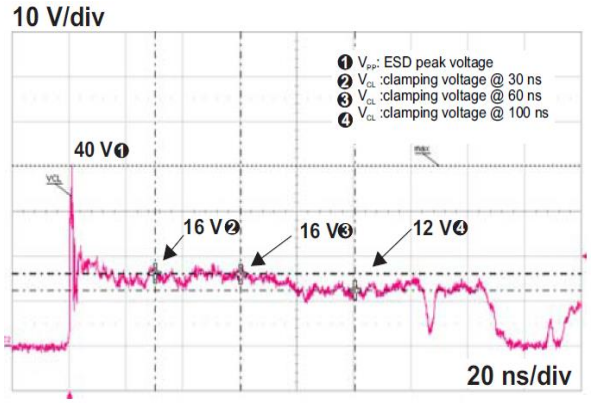


Figure 12: ESD response to IEC 61000-4-2 (-8 kV air discharge)

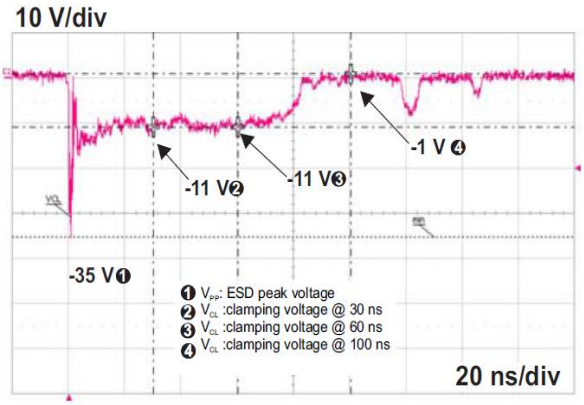


Figure 13: S21 attenuation measurement result

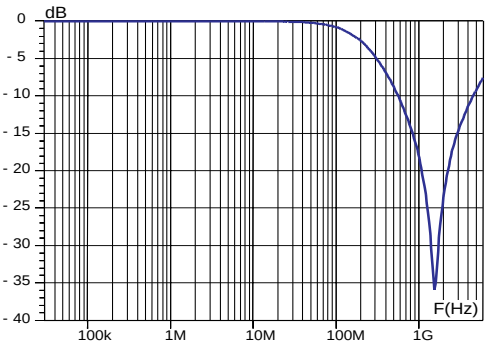
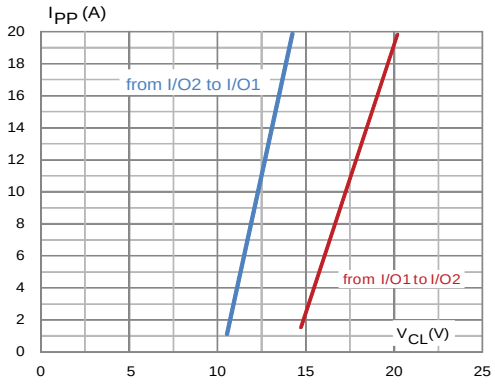


Figure 14: TLP measurement



2 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

2.1 SOD882 package information

Figure 15: SOD882 package outline

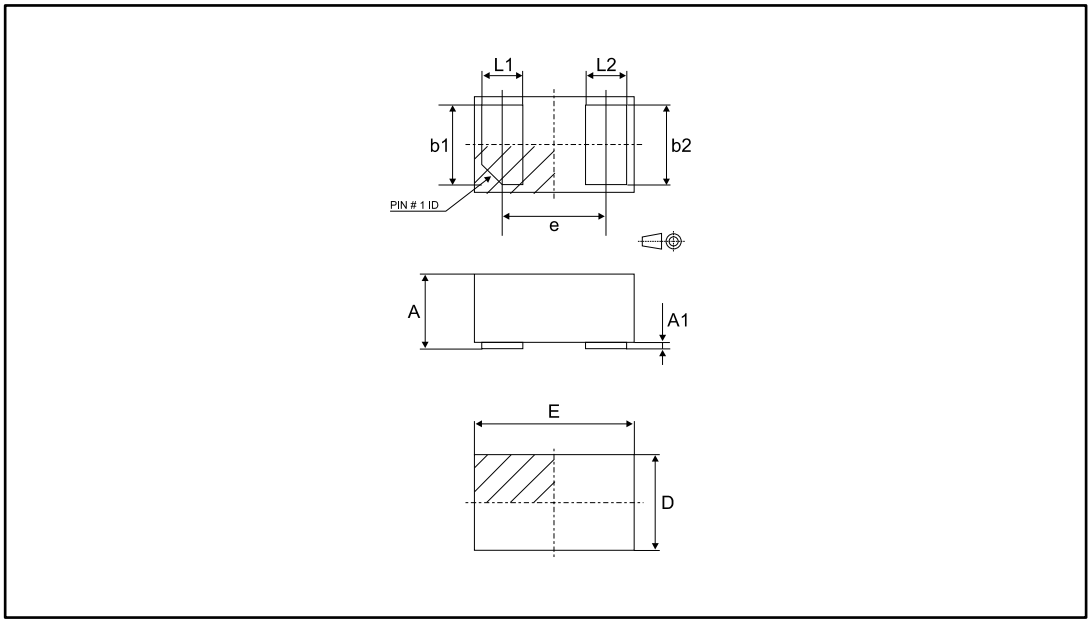


Table 3: SOD882 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.40	0.47	0.50	0.016	0.019	0.020
A1	0.00		0.05	0.000		0.002
b1	0.45	0.50	0.55	0.018	0.020	0.022
b2	0.45	0.50	0.55	0.018	0.020	0.022
D	0.55	0.60	0.65	0.022	0.024	0.026
E	0.95	1.00	1.05	0.037	0.039	0.041
e	0.60	0.65	0.70	0.024	0.026	0.028
L1	0.20	0.25	0.30	0.008	0.010	0.012
L2	0.20	0.25	0.30	0.008	0.010	0.012

Figure 16: Footprint recommendations, dimensions in mm (inches)

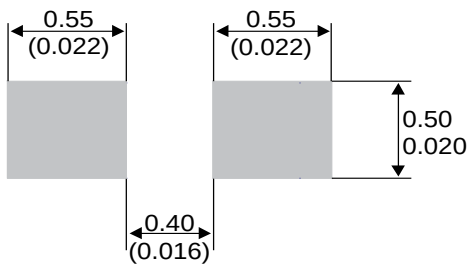
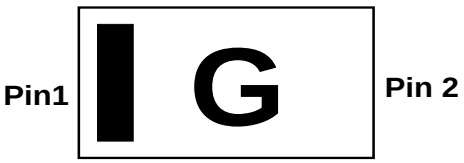
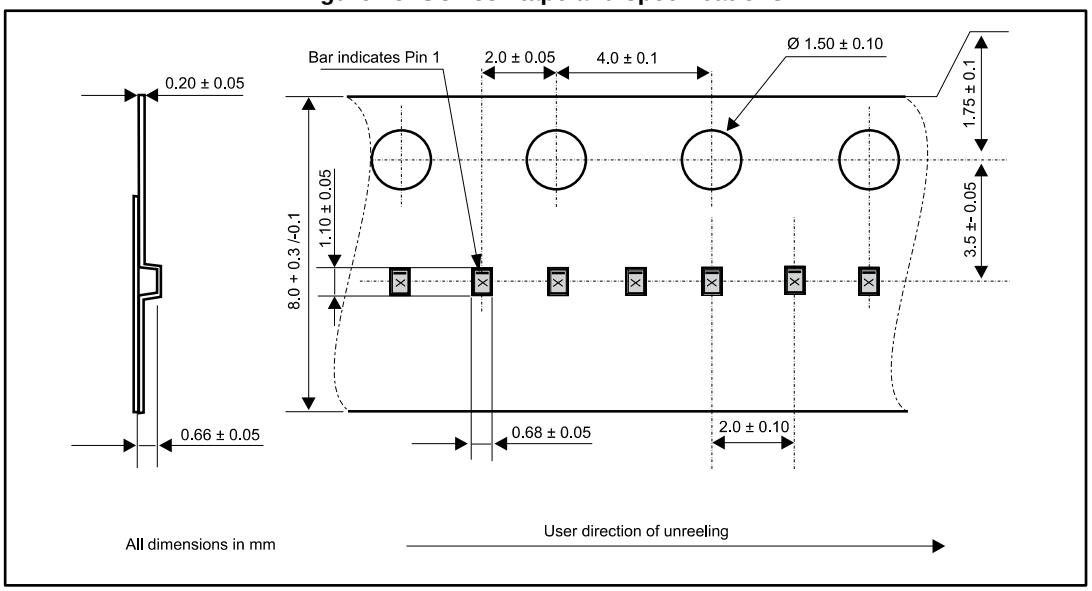


Figure 17: Marking



Product marking may be rotated by multiples of 90° for assembly plant differentiation. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

Figure 18: SOD882 tape and specifications



2.2 SOD882T package information

Figure 19: SOD882T package outline

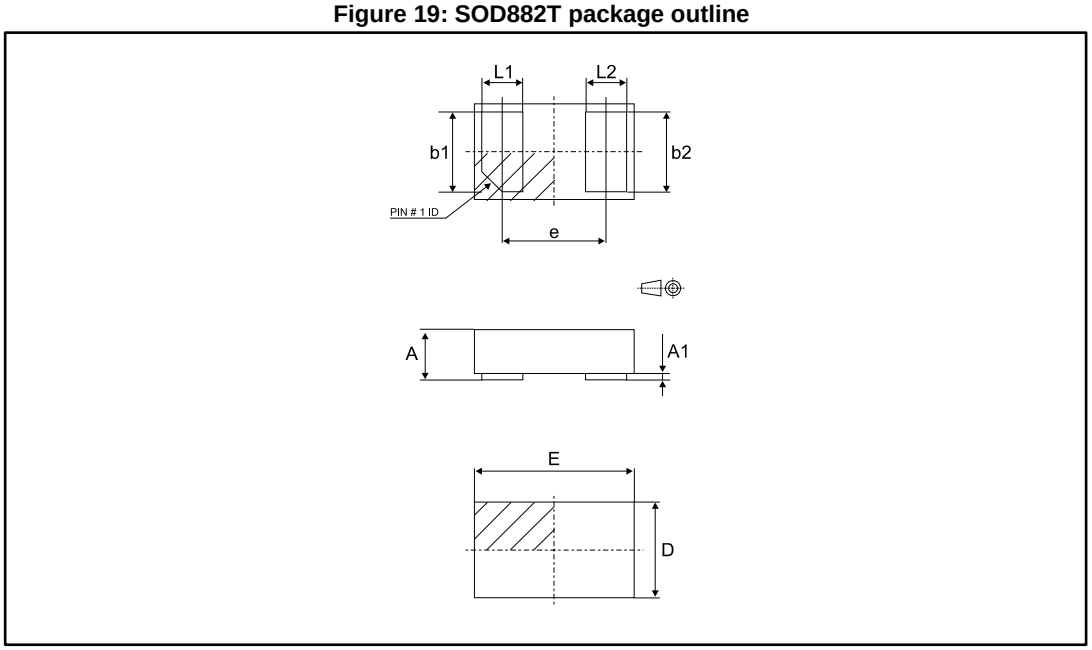


Table 4: SOD882T package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.30		0.40	0.012		0.016
A1	0.00		0.05	0.000		0.002
b1	0.45	0.50	0.55	0.018	0.020	0.022
b2	0.45	0.50	0.55	0.018	0.020	0.022
D	0.55	0.60	0.65	0.022	0.024	0.026
E	0.95	1.00	1.05	0.037	0.039	0.041
e	0.60	0.65	0.70	0.024	0.026	0.028
L1	0.20	0.25	0.30	0.008	0.010	0.012
L2	0.20	0.25	0.30	0.008	0.010	0.012

Figure 20: Footprint recommendations, dimensions in mm (inches)

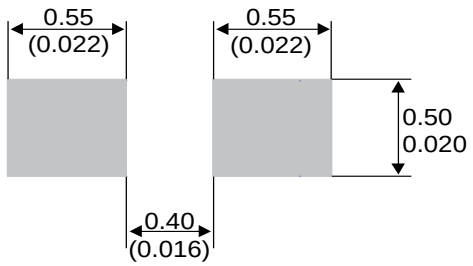
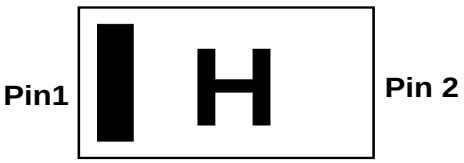
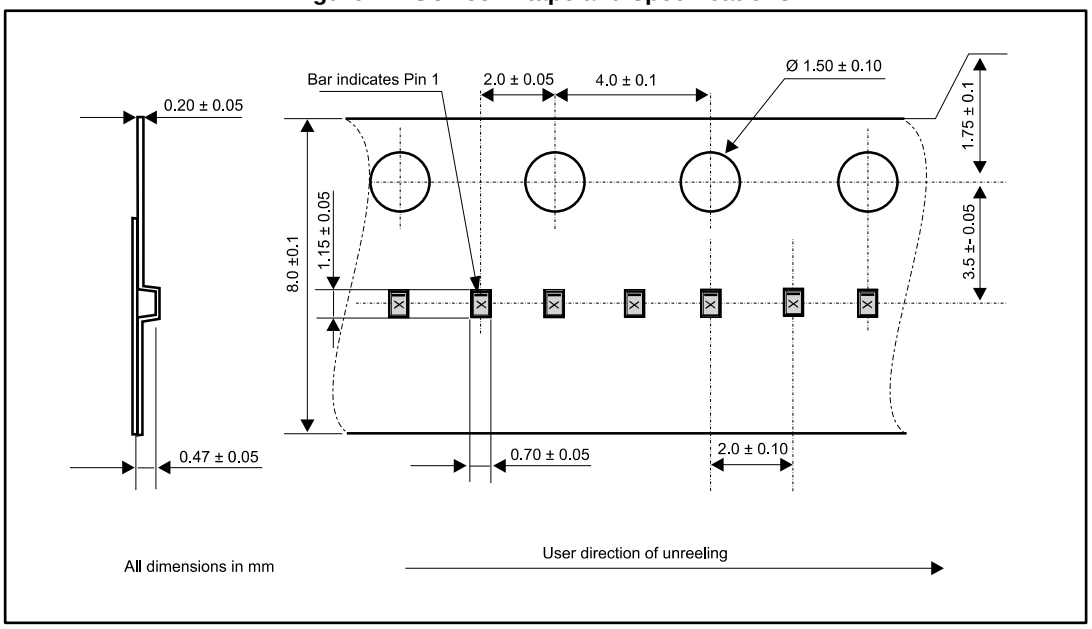


Figure 21: Marking



Product marking may be rotated by multiples of 90° for assembly plant differentiation. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

Figure 22: SOD882T tape and specifications



3 Recommendation on PCB assembly

3.1 Stencil opening design

1. General recommendation on stencil opening design
   a. Stencil opening dimensions: L (Length), W (Width), T (Thickness).
2. General design rule
   a. Stencil thickness (T) = 75 ~ 125 µm
   b. Aspect ratio = $\frac{W}{T} \geq 1.5$
   c. Aspect area = $\frac{L \times W}{2T(L+W)} \geq 0.66$
3. Reference design
   a. Stencil opening thickness: 100 µm
   b. Stencil opening for central exposed pad: Opening to footprint ratio is 50%.
   c. Stencil opening for leads: Opening to footprint ratio is 90%.

Figure 23: Stencil opening dimensions

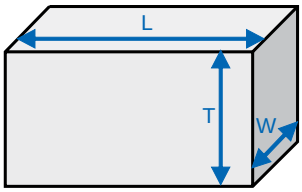
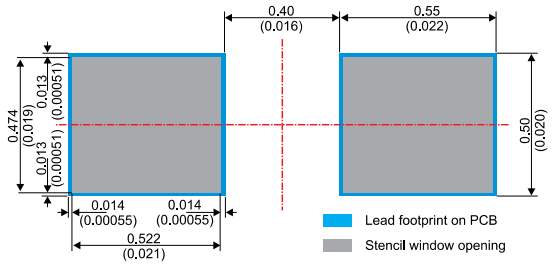


Figure 24: Recommended stencil window position in mm (inches)



3.2 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste is recommended.
3. Offers a high tack force to resist component movement during high speed.
4. Solder paste with fine particles: powder particle size is 20-38 µm.

3.3 Placement

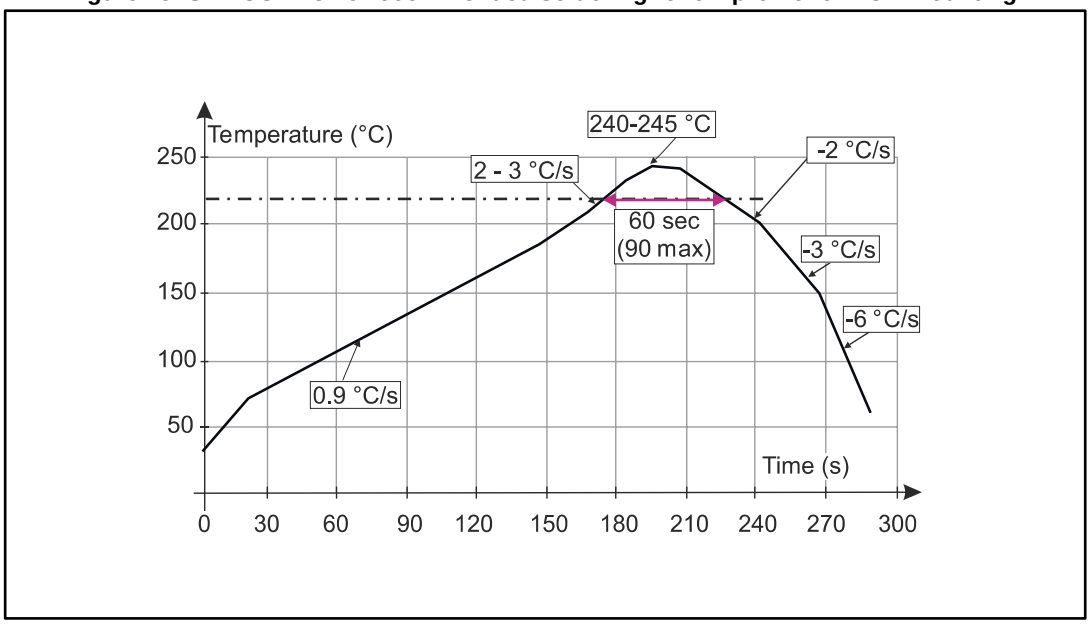
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering
3. Standard tolerance of ±0.05 mm is recommended.
4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

3.4 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. The symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away.

3.5 Reflow profile

Figure 25: ST ECOPACK® recommended soldering reflow profile for PCB mounting



Minimize air convection currents in the reflow oven to avoid component movement.

Maximum soldering profile corresponds to the latest IPC/JEDEC J-STD-020.

4 Ordering information

Figure 26: Ordering information scheme

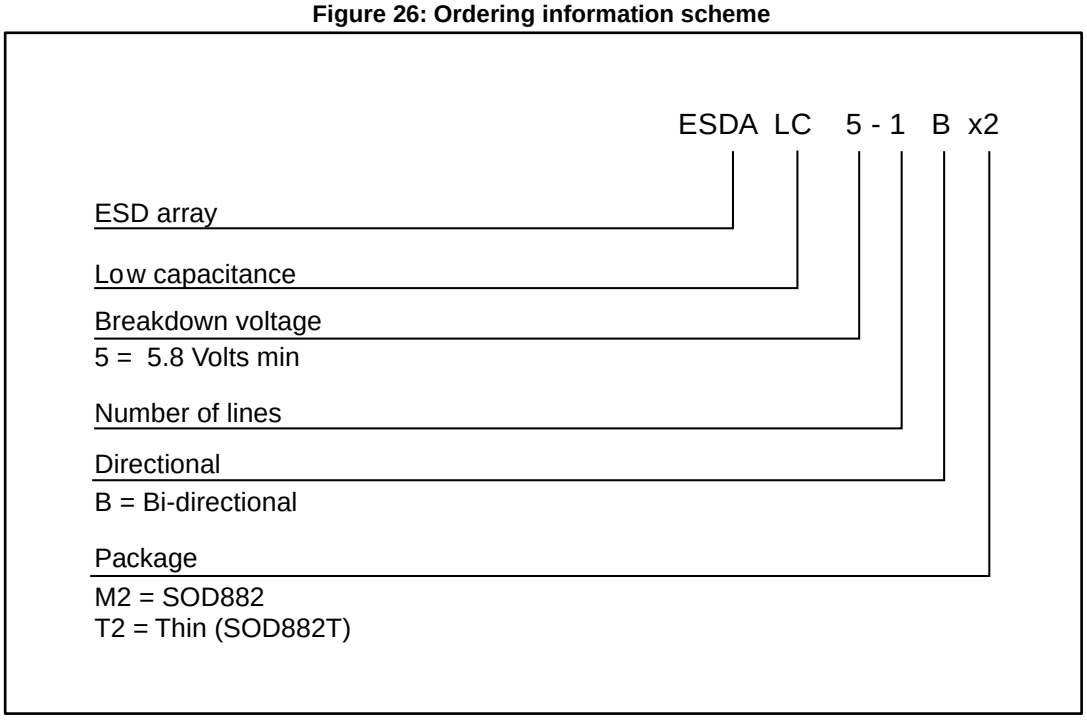


Table 5: Ordering information

Order code	Marking[(1)]	Package	Weight	Base qty.	Delivery mode
ESDALC5-1BM2	G	SOD882	0.93 mg	12000	Tape and reel
ESDALC5-1BT2	H	SOD882T	0.82 mg	12000	Tape and reel

Notes:

(1)The marking can be rotated by multiples of 90° to differentiate assembly location

5 Revision history

Table 6: Document revision history

Date	Revision	Changes
02-Feb-2010	1	Initial release.
06-Jun-2012	2	Updated *Figure 11, Figure 12, Figure 15, Figure 19, Table 3*, and *Table 4*. Updated note in page 7, 8 and 13. Updated I_{RM} in *Table 2*.
05-Mar-2013	3	Clamping voltage at 30 ns added in *Table 2*.
09-Jan-2014	4	Updated *Table 1, Table 2, Table 5, Figure 2, Figure 3, Figure 4, Figure 5, Figure 6, Figure 7, Figure 8, Figure 9, Figure 10, Figure 11, Figure 12, Figure 16, Figure 17, Figure 20, Figure 21* and *Figure 24*. Added *Figure 14*.
02-Apr-2014	5	Updated *Figure 4* and *Figure 5*.
28-Nov-2016	6	Updated cover image, *Table 2: "Electrical characteristics (Tamb = 25 °C)"* and *Figure 2: "Electrical characteristics (definitions)"*.

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