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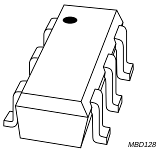
Team Nexperia



PMGD400UN

Dual N-channel µTrenchMOS™ ultra low level FET

Rev. 01 — 3 March 2004 **Product data**

1. Product profile

1.1 Description

Dual N-channel enhancement mode field-effect transistor in a plastic package using TrenchMOS™ technology.

1.2 Features

- Surface mounted package
- Dual device
- Low on-state resistance
- Footprint 40% smaller than SOT23
- Fast switching
- Low threshold voltage.

1.3 Applications

- Driver circuits
- Switching in portable appliances.

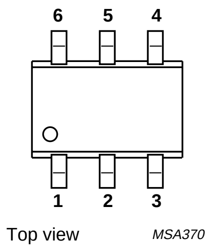
1.4 Quick reference data

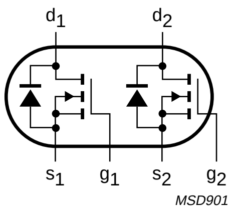
- $V_{DS} \leq 30$ V
- $P_{tot} \leq 0.41$ W
- $I_D \leq 0.71$ A
- $R_{DSon} \leq 480$ mΩ.

2. Pinning information

Table 1: Pinning - SOT363 (SC-88), simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	source (s1)		
2	gate (g1)		
3	drain (d2)		
4	source (s2)		
5	gate (g2)		
6	drain (d1)		





SOT363 (SC-88)

3. Ordering information

Table 2: Ordering information

Type number	Package		
	Name	Description	Version
PMGD400UN	SC-88	Plastic surface mounted package; 6 leads	SOT363

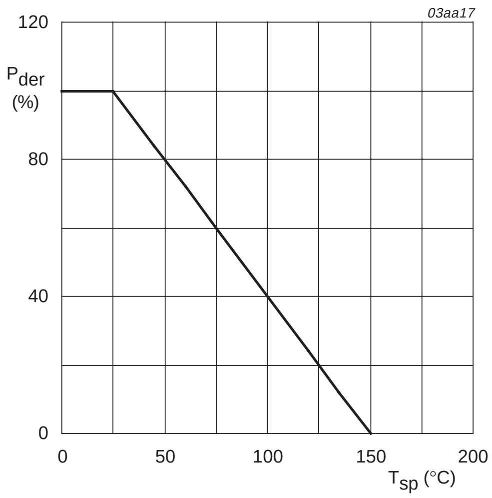
4. Limiting values

Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

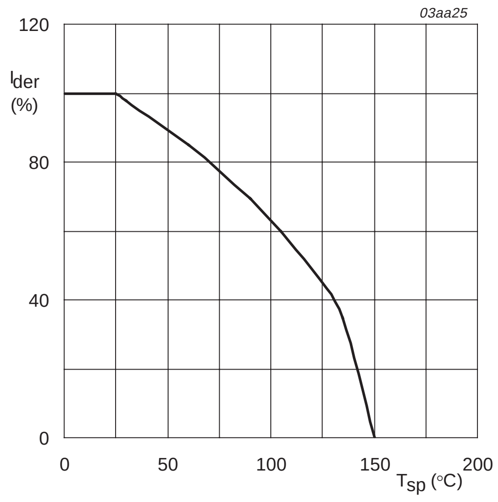
Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage (DC)	25 °C ≤ T_j ≤ 150 °C		-	30	V
V_{DGR}	drain-gate voltage (DC)	25 °C ≤ T_j ≤ 150 °C; R_{GS} = 20 kΩ		-	30	V
V_{GS}	gate-source voltage (DC)			-	±8	V
I_D	drain current (DC)	T_{sp} = 25 °C; V_{GS} = 4.5 V; Figure 2 and 3	[1]	-	0.71	A
		T_{sp} = 100 °C; V_{GS} = 4.5 V; Figure 2	[1]	-	0.45	A
I_{DM}	peak drain current	T_{sp} = 25 °C; pulsed; t_p ≤ 10 µs; Figure 3	[1]	-	1.42	A
P_{tot}	total power dissipation	T_{sp} = 25 °C; Figure 1		-	0.41	W
T_{stg}	storage temperature			–55	+150	°C
T_j	junction temperature			–55	+150	°C
Source-drain diode						
I_S	source (diode forward) current (DC)	T_{sp} = 25 °C	[1]	-	0.34	A
I_{SM}	peak source (diode forward) current	T_{sp} = 25 °C; pulsed; t_p ≤ 10 µs	[1]	-	0.69	A

[1] Single device conducting.



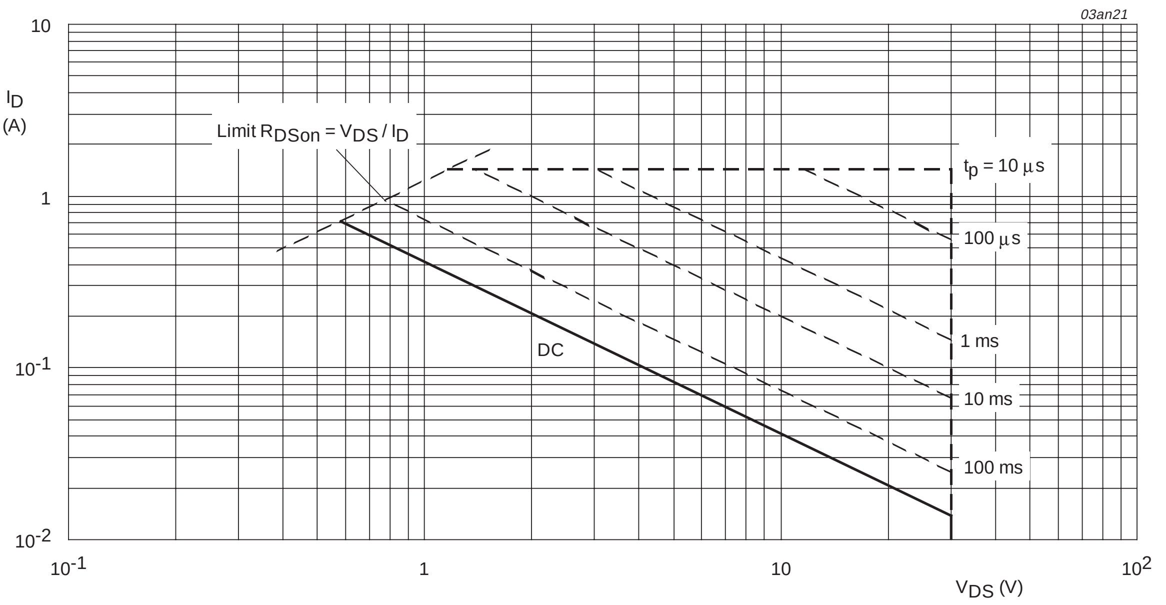
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of solder point temperature.



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of solder point temperature.



T_{sp} = 25 °C; I_{DM} is single pulse; V_{GS} = 4.5 V

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	Figure 4	-	-	300	K/W

5.1 Transient thermal impedance

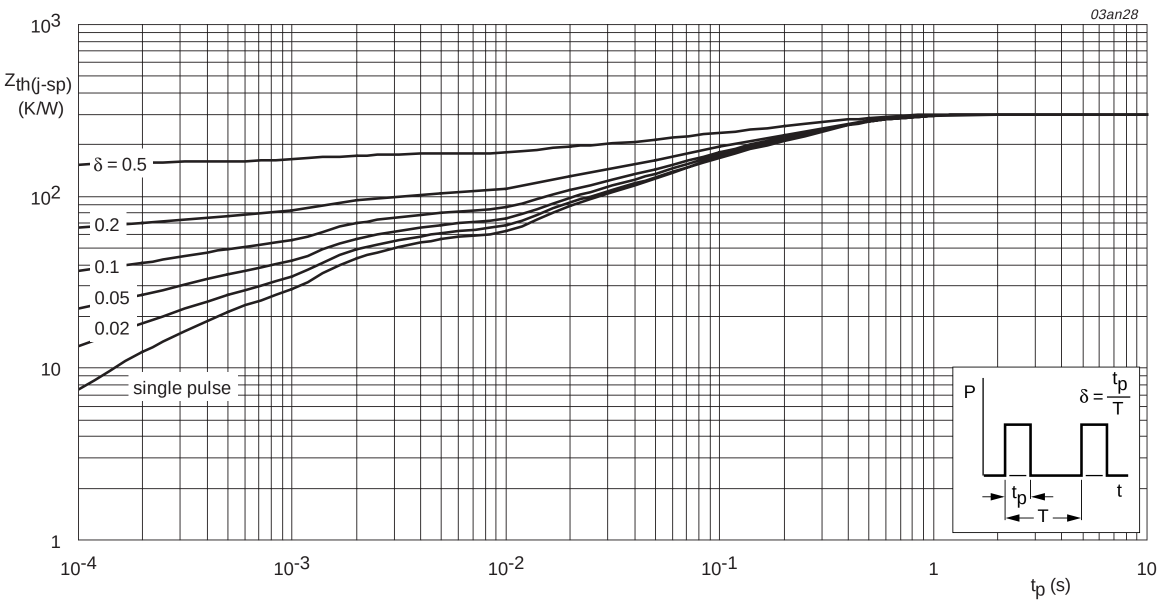


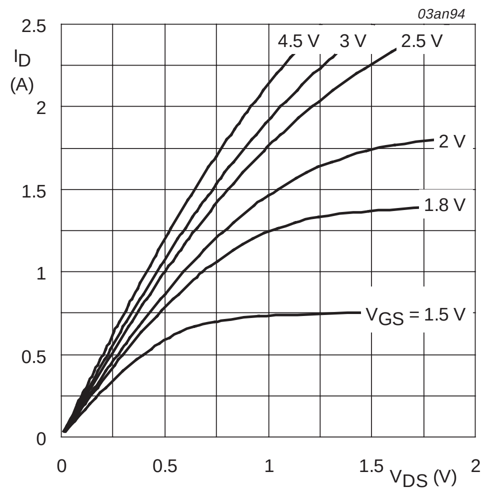
Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration.

6. Characteristics

Table 5: Characteristics

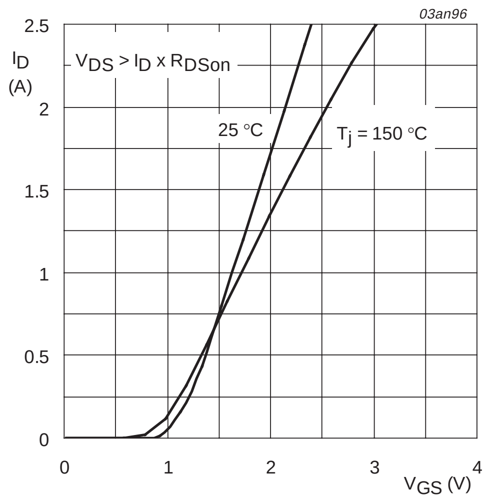
T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 1 µA; V_{GS} = 0 V				
		T_j = 25 °C	30	-	-	V
		T_j = –55 °C	27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 0.25 mA; V_{DS} = V_{GS}; Figure 9				
		T_j = 25 °C	0.45	0.7	1	V
		T_j = 150 °C	0.25	-	-	V
		T_j = –55 °C	-	-	1.2	V
I_{DSS}	drain-source leakage current	V_{DS} = 30 V; V_{GS} = 0 V				
		T_j = 25 °C	-	-	1	µA
		T_j = 150 °C	-	-	100	µA
I_{GSS}	gate-source leakage current	V_{GS} = ±8 V; V_{DS} = 0 V	-	10	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 0.2 A; Figure 7 and 8				
		T_j = 25 °C	-	400	480	mΩ
		T_j = 150 °C	-	660	816	mΩ
		V_{GS} = 2.5 V; I_D = 0.1 A; Figure 7 and 8	-	480	580	mΩ
		V_{GS} = 1.8 V; I_D = 0.075 A; Figure 7 and 8	-	580	830	mΩ
Dynamic characteristics						
$Q_{g(tot)}$	total gate charge	I_D = 1 A; V_{DD} = 15 V; V_{GS} = 4.5 V; Figure 13	-	0.89	-	nC
Q_{gs}	gate-source charge		-	0.1	-	nC
Q_{gd}	gate-drain (Miller) charge		-	0.2	-	nC
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz; Figure 11	-	43	-	pF
C_{oss}	output capacitance		-	7.7	-	pF
C_{rss}	reverse transfer capacitance		-	4.8	-	pF
$t_{d(on)}$	turn-on delay time	V_{DD} = 15 V; R_L = 15 Ω; V_{GS} = 4.5 V; R_G = 6 Ω	-	4	-	ns
t_r	rise time		-	7.5	-	ns
$t_{d(off)}$	turn-off delay time		-	18	-	ns
t_f	fall time		-	4.5	-	ns
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	I_S = 0.3 A; V_{GS} = 0 V; Figure 12	-	0.76	1.2	V



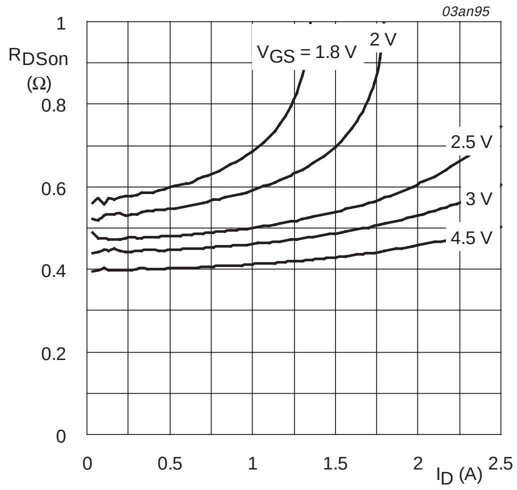
T_j = 25 °C

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



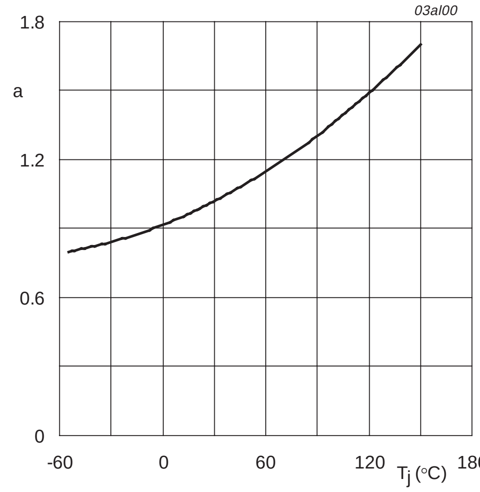
T_j = 25 °C and 150 °C; $V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



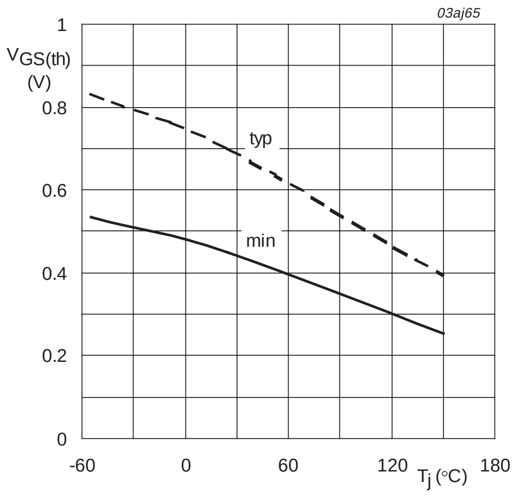
T_j = 25 °C

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



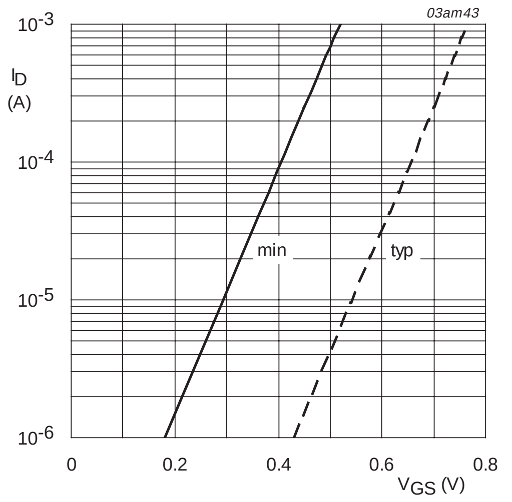
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ C)}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



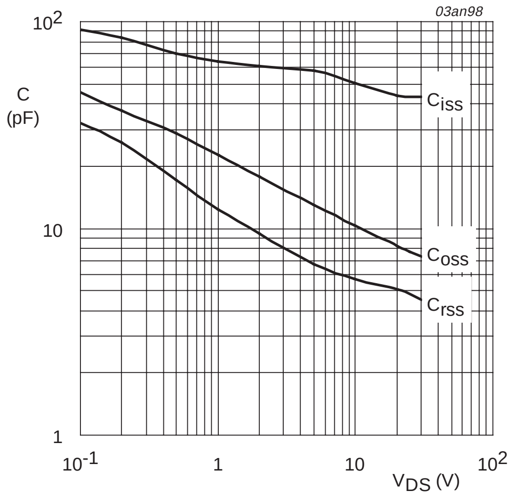
I_D = 0.25 mA; V_{DS} = V_{GS}

Fig 9. Gate-source threshold voltage as a function of junction temperature.



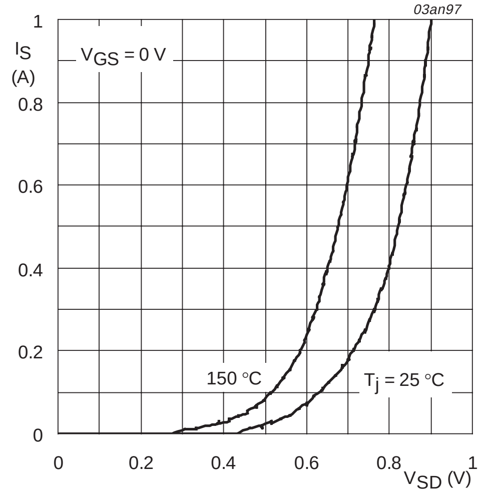
T_j = 25 °C; V_{DS} = 5 V

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



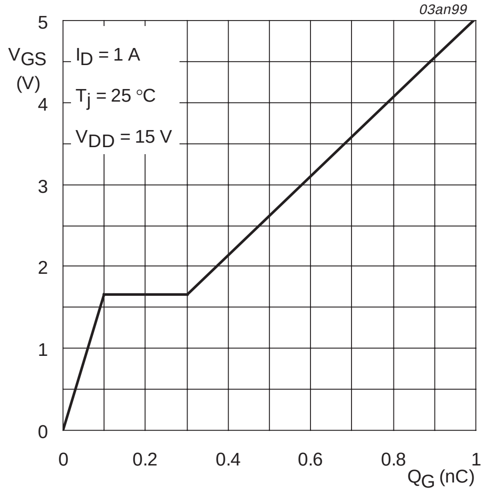
V_{GS} = 0 V; f = 1 MHz

Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



T_j = 25 °C and 150 °C; V_{GS} = 0 V

Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.

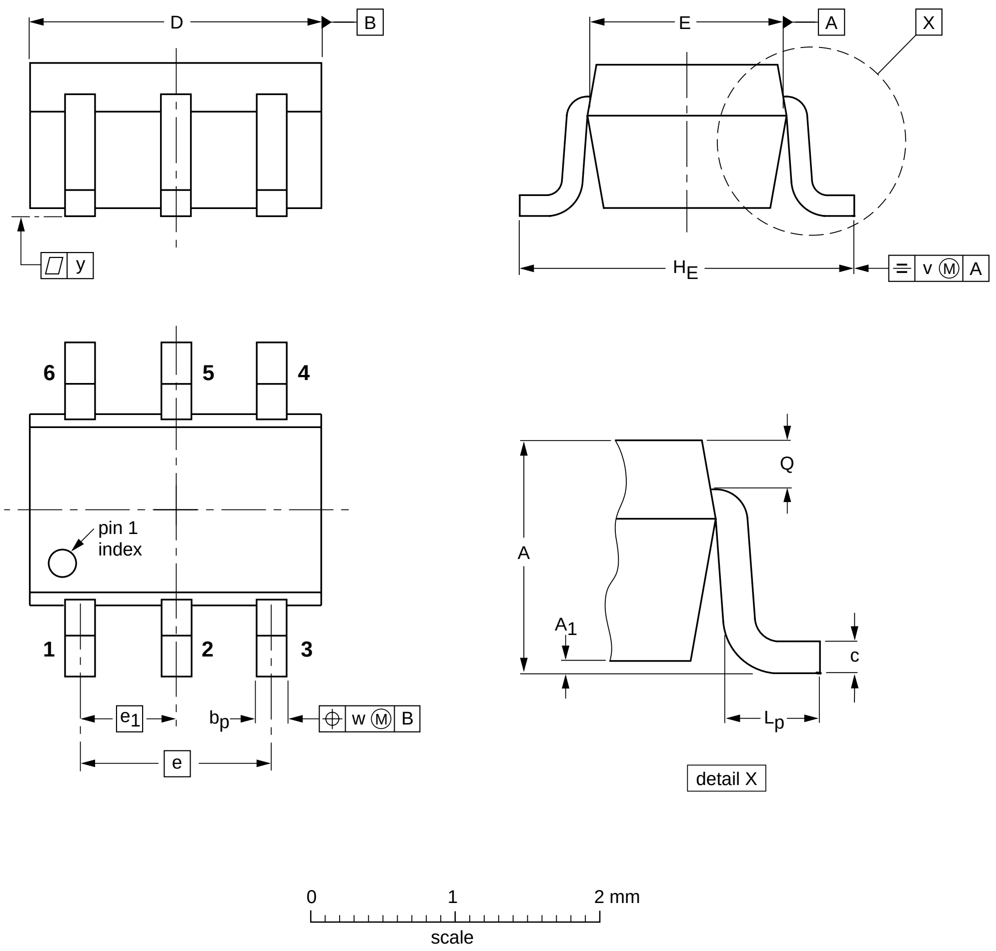


I_D = 1 A; V_{DD} = 15 V

Fig 13. Gate-source voltage as a function of gate charge; typical values.

7. Package outline

Plastic surface mounted package; 6 leads **SOT363**



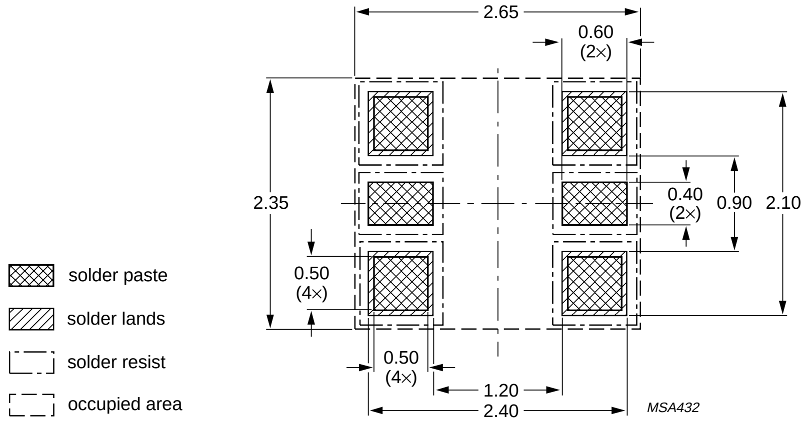
DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.1 0.8	0.1	0.30 0.20	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.25 0.15	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT363			SC-88			97-02-28

Fig 14. SOT363 (SC-88).

8. Soldering



Dimensions in mm.

Fig 15. Reflow soldering footprint for SOT363 (SC-88).

9. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
01	20040303	-	Product data (9397 750 12759)

10. Data sheet status

Level	Data sheet status[1]	Product status[2][3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

11. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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