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November 1988 Revised November 1999

74AC251 • 74ACT251 8-Input Multiplexer with 3-STATE Output

General Description

The AC/ACT251 is a high-speed 8-input digital multiplexer. It provides, in one package, the ability to select one bit of data from up to eight sources. It can be used as universal function generator to generate any logic function of four variables. Both true and complementary outputs are provided.

Features

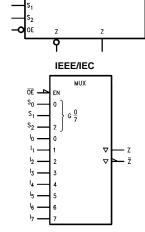
- I_{CC} reduced by 50%
- Multifunctional capability
- On-chip select logic decoding
- Inverting and noninverting 3-STATE outputs
- Outputs source/sink 24 mA
- ACT251 has TTL-compatible inputs

Ordering Code:

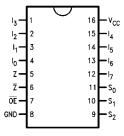
Order Number	Package Number	Package Description
74AC251SC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body
74AC251SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74AC251MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74AC251PC	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
74ACT251SC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body
74ACT251MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ACT251PC	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Logic Symbols



Connection Diagram



Pin Descriptions

Pin Names	Description				
S ₀ -S ₂	Select Inputs				
OE	3-STATE Output Enable Input				
I ₀ -I ₇	Multiplexer Inputs				
Z	3-STATE Multiplexer Output				
Z	Complementary 3-STATE Multiplexer Output				

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DS009945

Functional Description

This device is a logical implementation of a single-pole, 8-position switch with the switch position controlled by the state of three Select inputs, $S_0,\,S_1,\,S_2.$ Both true and complementary outputs are provided. The Output Enable input (\overline{OE}) is active LOW. When it is activated, the logic function provided at the output is:

$$\begin{split} Z = \overline{OE} \bullet & \quad (I_0 \bullet \overline{S}_0 \bullet \overline{S}_1 \bullet \overline{S}_2 + I_1 \bullet S_0 \bullet \overline{S}_1 \bullet \overline{S}_2 + \\ & \quad I_2 \bullet \overline{S}_0 \bullet S_1 \bullet \overline{S}_2 + I_3 \bullet S_0 \bullet S_1 \bullet \overline{S}_2 + \\ & \quad I_4 \bullet \overline{S}_0 \bullet \overline{S}_1 \bullet S_2 + I_5 \bullet S_0 \bullet \overline{S}_1 \bullet S_2 + \\ & \quad I_6 \bullet \overline{S}_0 \bullet S_1 \bullet S_2 + I_7 \bullet S_0 \bullet S_1 \bullet S_2) \end{split}$$

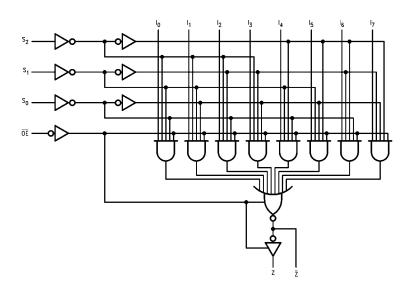
When the Output Enable is HIGH, both outputs are in the high impedance (High Z) state. This feature allows multiplexer expansion by tying the outputs of up to 128 devices together. When the outputs of the 3-STATE devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. The Output Enable signals should be designed to ensure there is no overlap in the active-LOW portion of the enable voltages.

Truth Table

	Inp	Out	puts		
OE	S ₂	S ₁	S ₀	Z	Z
Н	Х	Х	Х	Z	Z
L	L	L	L	Ī ₀	I_0
L	L	L	Н	Ī ₁	I ₁
L	L	Н	L	Ī ₂	l ₂
L	L	Н	Н	Ī ₃	I_3
L	Н	L	L	\overline{I}_4	I_4
L	Н	L	Н	Ī ₅	l ₅
L	Н	Н	L	Ī ₆	I ₆
L	Н	Н	Н	Ī ₇	l ₇

H = HIGH Voltage Level

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

L = LOW Voltage Level

X = Immaterial

Z = High Impedance

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC}) -0.5V to +7.0V

DC Input Diode Current (I_{IK})

 $\begin{array}{ccc} \text{V}_{\text{I}} = -0.5 \text{V} & -20 \text{ mA} \\ \text{V}_{\text{I}} = \text{V}_{\text{CC}} + 0.5 \text{V} & +20 \text{ mA} \\ \text{DC Input Voltage (V}_{\text{I}}) & -0.5 \text{V to V}_{\text{CC}} + 0.5 \text{V} \end{array}$

DC Output Diode Current (I_{OK})

 $\begin{aligned} \text{V}_{\text{O}} &= -0.5 \text{V} & -20 \text{ mA} \\ \text{V}_{\text{O}} &= \text{V}_{\text{CC}} + 0.5 \text{V} & +20 \text{ mA} \end{aligned}$

-0.5V to $V_{CC} + 0.5V$

DC Output Voltage (V_O)
DC Output Source

or Sink Current (I_O) $\pm 50 \text{ mA}$

DC V_{CC} or Ground Current

per Output Pin (I_{CC} or I_{GND}) ± 50 mA Storage Temperature (T_{STG}) -65° C to $+150^{\circ}$ C

Storage Temperature (T_{STG})

Junction Temperature (T_J)

PDIP 140°C

Recommended Operating Conditions

Supply Voltage (V_{CC})

Minimum Input Edge Rate (ΔV/Δt)

AC Devices

 $V_{\mbox{\footnotesize{IN}}}$ from 30% to 70% of $V_{\mbox{\footnotesize{CC}}}$

 $V_{CC} @ 3.3V, 4.5V, 5.5V$ 125 mV/ns

Minimum Input Edge Rate ($\Delta V/\Delta t$)

ACT Devices

 V_{IN} from 0.8V to 2.0V

V_{CC} @ 4.5V, 5.5V 125 mV/ns

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACTTM circuits outside databook specifications.

DC Electrical Characteristics for AC

Cumhal	Parameter	V _{CC}	T _A =	+25°C	$T_A = -40^{\circ}C$ to $+85^{\circ}C$	Units	Conditions
Symbol		(V)	(V) Typ		aranteed Limits	Units	Conditions
V _{IH}	Minimum HIGH Level	3.0	1.5	2.1	2.1		V _{OUT} = 0.1V
	Input Voltage	4.5	2.25	3.15	3.15	V	or V _{CC} - 0.1V
		5.5	2.75	3.85	3.85		
V _{IL}	Maximum LOW Level	3.0	1.5	0.9	0.9		$V_{OUT} = 0.1V$
	Input Voltage	4.5	2.25	1.35	1.35	V	or V _{CC} - 0.1V
		5.5	2.75	1.65	1.65		
V _{OH}	Minimum HIGH Level	3.0	2.99	2.9	2.9		
	Output Voltage	4.5	4.49	4.4	4.4	V	$I_{OUT} = -50 \mu A$
		5.5	5.49	5.4	5.4		
							$V_{IN} = V_{IL}$ or V_{IH}
		3.0		2.56	2.46		$I_{OH} = -12 \text{ mA}$
		4.5		3.86	3.76	V	$I_{OH} = -24 \text{ mA}$
		5.5		4.86	4.76		$I_{OH} = -24 \text{ mA (Note 2)}$
V _{OL}	Maximum LOW Level	3.0	0.002	0.1	0.1		
	Output Voltage	4.5	0.001	0.1	0.1	V	$I_{OUT} = 50 \ \mu A$
		5.5	0.001	0.1	0.1		
							$V_{IN} = V_{IL}$ or V_{IH}
		3.0		0.36	0.44		I _{OL} = 12 mA
		4.5		0.36	0.44	V	$I_{OL} = 24 \text{ mA}$
		5.5		0.36	0.44		I _{OL} = 24 mA (Note 2)
I _{IN} (Note 4)	Maximum Input Leakage Current	5.5		±0.1	±1.0	μΑ	$V_I = V_{CC}$, GND
I _{OZ}	Maximum 3-STATE						V_{I} (OE) = V_{IL} , V_{IH}
	Current	5.5		±0.25	±2.5	μΑ	$V_I = V_{CC}, V_{GND}$
							$V_O = V_{CC}$, GND
I _{OLD}	Minimum Dynamic	5.5			75	mA	V _{OLD} = 1.65V Max
I _{OHD}	Output Current (Note 3)	5.5			-75	mA	V _{OHD} = 3.85V Min
I _{CC} (Note 4)	Maximum Quiescent Supply Curent	5.5		4.0	40.0	μΑ	$V_{IN} = V_{CC}$ or GND

Note 2: All outputs loaded; thresholds on input associated with output under test.

 $\textbf{Note 3:} \ \text{Maximum test duration 2.0 ms, one output loaded at a time.}$

Note 4: $I_{\rm IN}$ and $I_{\rm CC}$ @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V $V_{\rm CC}$.

74AC251 • 74ACT251

DC Electrical Characteristics for ACT

Symbol	Parameter			$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$	Units	Conditions	
Cyllibol		(V)	Тур	Gu	aranteed Limits	Oilita	Conditions
V _{IH}	Minimum HIGH Level	4.5	1.5	2.0	2.0	V	V _{OUT} = 0.1V
	Input Voltage	5.5	1.5	2.0	2.0	V	or V _{CC} – 0.1V
V _{IL}	Maximum LOW Level	4.5	1.5	0.8	0.8	V	V _{OUT} = 0.1V
	Input Voltage	5.5	1.5	0.8	0.8	v	or V _{CC} – 0.1V
V _{OH}	Minimum HIGH Level	4.5	4.49	4.4	4.4	V	I _{OUT} = -50 μA
	Output Voltage	5.5	5.49	5.4	5.4	v	1 _{OUT} = -30 μA
							$V_{IN} = V_{IL}$ or V_{IH}
		4.5		3.86	3.76	V	$I_{OH} = -24 \text{ mA}$
		5.5		4.86	4.76		$I_{OH} = -24 \text{ mA (Note 5)}$
V _{OL}	Maximum LOW Level	4.5	0.001	0.1	0.1	V	I 50A
	Output Voltage	5.5	0.001	0.1	0.1	V	$I_{OUT} = 50 \mu A$
							$V_{IN} = V_{IL}$ or V_{IH}
		4.5		0.36	0.44	V	I _{OL} = 24 mA
		5.5		0.36	0.44		I _{OL} = 24 mA (Note 5)
I _{IN}	Maximum Input	5.5		±0.1	±1.0	μА	$V_{I} = V_{CC}$, GND
	Leakage Current	3.3		10.1	±1.0	μΛ	VI = VCC, GIAD
I _{OZ}	Maximum 3-STATE	5.5		±0.5	±5.0	μА	$V_I = V_{IL}, V_{IH}$
	Current	0.0			±3.0		$V_O = V_{CC}$, GND
I _{CCT}	Maximum	5.5	0.6		1.5	mA	V _I = V _{CC} - 2.1V
	I _{CC} /Input	3.3	0.0		1.5		VI = VCC = 2.1V
I _{OLD}	Minimum Dynamic	5.5			75	mA	V _{OLD} = 1.65V Max
I _{OHD}	Output Current (Note 6)	5.5			-75	mA	V _{OHD} = 3.85V Min
I _{CC}	Maximum Quiescent	5.5		4.0	40.0	μА	$V_{IN} = V_{CC}$
	Supply Current	5.5		7.0	- 0.0	μΛ	or GND

Note 5: All outputs loaded; thresholds on input associated with output under test.

Note 6: Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics for AC

	Parameter	V _{CC}		$T_A = +25^{\circ}C$		T _A = -40°	C to +85°C	
Symbol		(V)	C _L = 50 pF			$C_L = 50 \text{ pF}$		Units
		(Note 7)	Min	Тур	Max	Min	Max	
t _{PLH}	Propagation Delay	3.3	1.5	11.5	17.5	1.5	19.0	
	S_n to Z or \overline{Z}	5.0	1.5	8.5	12.5	1.5	13.5	ns
t _{PHL}	Propagation Delay	3.3	1.5	11.0	17.5	1.5	19.0	20
	S_n to Z or \overline{Z}	5.0	1.5	8.0	12.5	1.5	13.5	ns
t _{PLH}	Propagation Delay	3.3	1.5	10.0	14.0	1.5	15.5	ns
	I_n to Z or \overline{Z}	5.0	1.5	7.0	10.0	1.5	11.0	115
t _{PHL}	Propagation Delay	3.3	1.5	9.0	14.0	1.5	15.5	ns
	I_n to Z or \overline{Z}	5.0	1.5	6.5	10.0	1.5	11.0	
t _{PZH}	Output Enable Time	3.3	1.5	7.5	11.0	1.5	12.0	ns
	OE to Z or Z	5.0	1.5	5.5	8.0	1.5	9.0	115
t _{PZL}	Output Enable Time	3.3	1.5	7.5	11.0	1.5	12.0	ns
	OE to Z or Z	5.0	1.5	5.5	8.0	1.5	9.0	115
t _{PHZ}	Output Disable Time	3.3	1.5	8.5	11.5	1.5	13.0	20
	OE to Z or Z	5.0	1.5	7.0	9.5	1.5	10.0	ns
t _{PLZ}	Output Disable Time	3.3	1.5	7.0	11.0	1.5	12.0	ns
	OE to Z or Z	5.0	1.5	5.5	8.0	1.5	8.5	115

Note 7: Voltage Range 3.3 is 3.3V ± 0.3V. Voltage Range 5.0 is 5.0V ± 0.5V

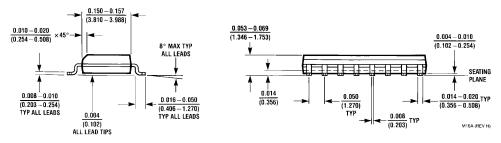
		V _{CC}		$T_A = +25^{\circ}C$		$T_A = -40^{\circ}$	C to +85°C	
Symbol	Parameter	(V)		$C_L = 50 pF$			$C_L = 50 \text{ pF}$	
		(Note 8)	Min	Тур	Max	Min	Max	
t _{PLH}	Propagation Delay S_n to Z or \overline{Z}	5.0	2.5	7.0	15.5	2.0	17.0	ns
t _{PHL}	Propagation Delay S_n to Z or \overline{Z}	5.0	2.5	7.5	16.5	2.5	18.5	ns
t _{PLH}	Propagation Delay I_n to Z or \overline{Z}	5.0	2.5	5.5	12.0	2.0	13.0	ns
t _{PHL}	Propagation Delay I_n to Z or \overline{Z}	5.0	2.5	6.5	12.5	2.5	14.0	ns
t _{PZH}	Output Enable Time OE to Z or Z	5.0	1.5	5.0	8.5	1.5	9.0	ns
t _{PZL}	Output Enable Time OE to Z or Z	5.0	1.5	4.5	8.5	1.5	9.5	ns
^t PHZ	Output Disable Time OE to Z or Z	5.0	2.0	6.0	12.0	2.0	13.0	ns
PLZ	Output Disable Time OE to Z or Z	5.0	1.5	4.5	8.5	1.5	9.0	ns

OE to Z or Z

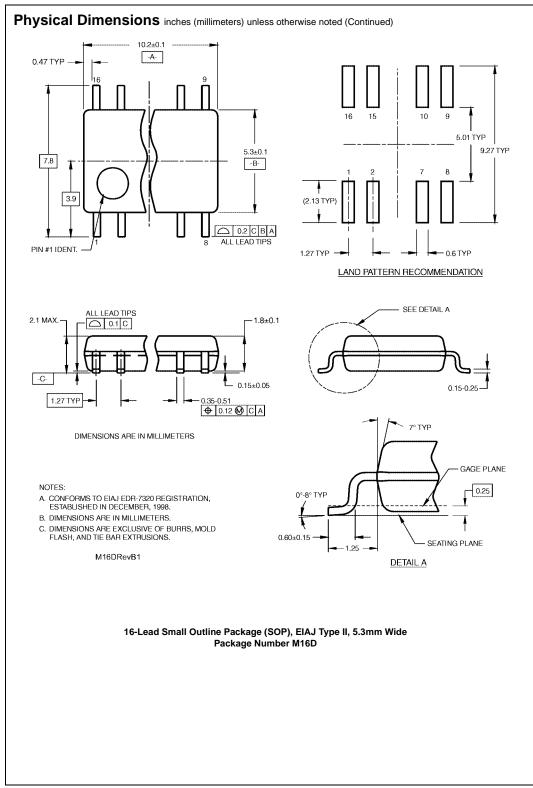
Note 8: Voltage Range 5.0 is 5.0V ±0.5V

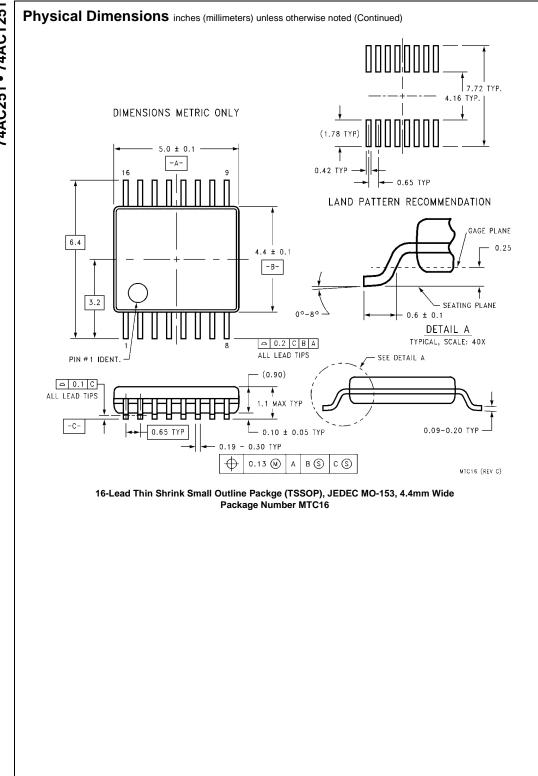
Capacitance

Symbol	Parameter	Тур	Units	Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = OPEN
Cpp	Power Dissipation Capacitance	70.0	pF	$V_{CC} = 5.0V$

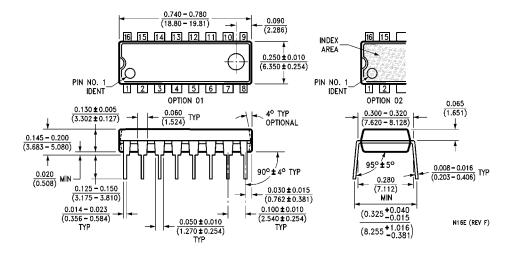


16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body Package Number M16A





Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N16E

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