NLSV8T244

8-Bit Dual-Supply Non-Inverting Level Translator

The NLSV8T244 is a 8−bit configurable dual−supply voltage level translator. The input A_n and output B_n ports are designed to track two different power supply rails, V_{CCA} and V_{CCB} respectively. Both supply rails are configurable from 0.9 V to 4.5 V allowing universal low−voltage translation from the input A_n to the output B_n port.

Features

- Wide V_{CCA} and V_{CCB} Operating Range: 0.9 V to 4.5 V
- High−Speed w/ Balanced Propagation Delay
- Inputs and Outputs have OVT Protection to 4.5 V
- Non−preferential V_{CCA} and V_{CCB} Sequencing
- Outputs at 3−State until Active V_{CC} is Reached
- Power−Off Protection
- Outputs Switch to 3−State with V_{CCB} at GND
- Ultra−Small Packaging: 4.0 mm x 2.0 mm UDFN20
- This is a Pb−Free Device

Typical Applications

- Mobile Phones, PDAs, Other Portable Devices

Important Information

- ESD Protection for All Pins:
  HBM (Human Body Model) > 6000 V

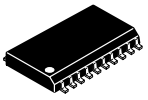
ON Semiconductor®

http://onsemi.com

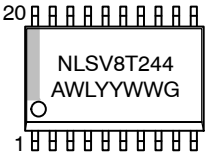
MARKING DIAGRAMS

UQFN20
MU SUFFIX
CASE 517AK

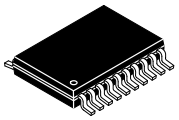
LC = Specific Device Code
M = Date Code
▪ = Pb−Free Package



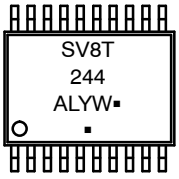
SOIC−20
DW SUFFIX
CASE 751D



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package



TSSOP−20
DT SUFFIX
CASE 948E



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

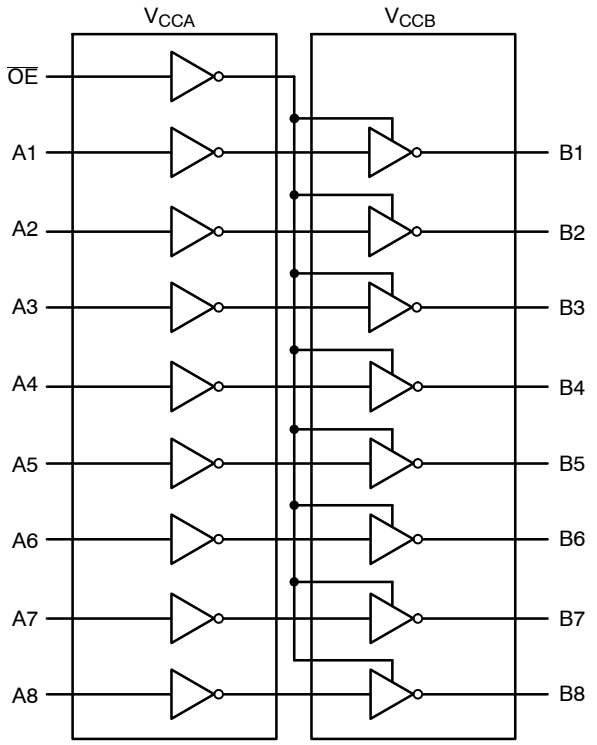


Figure 1. Logic Diagram

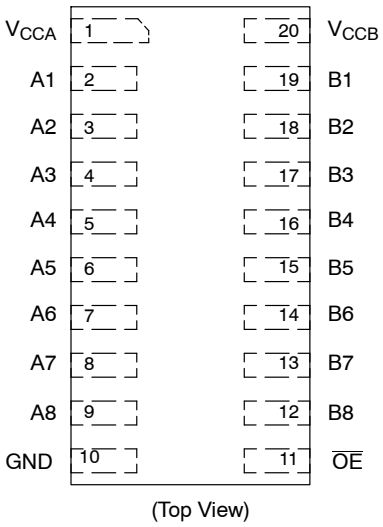


Figure 2. Pin Assignment

TRUTH TABLE

Inputs		Outputs
$\overline{OE}$	A_n	B_n
L	L	L
L	H	H
H	X	3−State

PIN ASSIGNMENT

PIN	FUNCTION
V_{CCA}	Input Port DC Power Supply
V_{CCB}	Output Port DC Power Supply
GND	Ground
A_n	Input Port
B_n	Output Port
$\overline{OE}$	Output Enable

MAXIMUM RATINGS

Symbol	Rating		Value	Condition	Unit
V_{CCA}, V_{CCB}	DC Supply Voltage		−0.5 to +5.5		V
V_I	DC Input Voltage	A_n	−0.5 to +5.5		V
V_C	Control Input	$\overline{OE}$	−0.5 to +5.5		V
V_O	DC Output Voltage (Power Down)	B_n	−0.5 to +5.5	$V_{CCA} = V_{CCB} = 0$	V
	(Active Mode)	B_n	−0.5 to +5.5		V
	(Tri−State Mode)	B_n	−0.5 to +5.5		V
I_{IK}	DC Input Diode Current		−20	V_I < GND	mA
I_{OK}	DC Output Diode Current		−50	V_O < GND	mA
I_O	DC Output Source/Sink Current		±50		mA
I_{CCA}, I_{CCB}	DC Supply Current Per Supply Pin		±100		mA
I_{GND}	DC Ground Current per Ground Pin		±100		mA
T_{STG}	Storage Temperature		−65 to +150		°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CCA}, V_{CCB}	Positive DC Supply Voltage		0.9	4.5	V
V_I	Bus Input Voltage		GND	4.5	V
V_C	Control Input	$\overline{OE}$	GND	4.5	V
V_{IO}	Bus Output Voltage (Power Down Mode)	B_n	GND	4.5	V
	(Active Mode)	B_n	GND	V_{CCB}	V
	(Tri−State Mode)	B_n	GND	4.5	V
T_A	Operating Temperature Range		−40	+85	°C
$\Delta t / \Delta V$	Input Transition Rise or Rate V_I, from 30% to 70% of V_{CC}; V_{CC} = 3.3 V ±0.3 V		0	10	nS

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CCA} (V)	V_{CCB} (V)	−40°C to +85°C		Unit
					Min	Max	
V_{IH}	Input HIGH Voltage (An, $\overline{OE}$)		3.6 – 4.5	0.9 – 4.5	2.2	–	V
			2.7 – 3.6		2.0	–	
			2.3 – 2.7		1.6	–	
			1.4 – 2.3		0.65 * V_{CCA}	–	
			0.9 – 1.4		0.9 * V_{CCA}	–	
V_{IL}	Input LOW Voltage (An, $\overline{OE}$)		3.6 – 4.5	0.9 – 4.5	–	0.8	V
			2.7 – 3.6		–	0.8	
			2.3 – 2.7		–	0.7	
			1.4 – 2.3		–	0.35 * V_{CCA}	
			0.9 – 1.4		–	0.1 * V_{CCA}	
V_{OH}	Output HIGH Voltage	I_{OH} = −100 μA; V_I = V_{IH}	0.9 – 4.5	0.9 – 4.5	V_{CCB} – 0.2	–	V
		I_{OH} = −0.5 mA; V_I = V_{IH}	0.9	0.9	0.75 * V_{CCB}	–	
		I_{OH} = −2 mA; V_I = V_{IH}	1.4	1.4	1.05	–	
		I_{OH} = −6 mA; V_I = V_{IH}	1.65	1.65	1.25	–	
			2.3	2.3	2.0	–	
		I_{OH} = −12 mA; V_I = V_{IH}	2.3	2.3	1.8	–	
			2.7	2.7	2.2	–	
		I_{OH} = −18 mA; V_I = V_{IH}	2.3	2.3	1.7	–	
			3.0	3.0	2.4	–	
		I_{OH} = −24 mA; V_I = V_{IH}	3.0	3.0	2.2	–	
V_{OL}	Output LOW Voltage	I_{OL} = 100 μA; V_I = V_{IL}	0.9 – 4.5	0.9 – 4.5	–	0.2	V
		I_{OL} = 0.5 mA; V_I = V_{IL}	1.1	1.1	–	0.3	
		I_{OL} = 2 mA; V_I = V_{IL}	1.4	1.4	–	0.35	
		I_{OL} = 6 mA; V_I = V_{IL}	1.65	1.65	–	0.3	
		I_{OL} = 12 mA; V_I = V_{IL}	2.3	2.3	–	0.4	
			2.7	2.7	–	0.4	
		I_{OL} = 18 mA; V_I = V_{IL}	2.3	2.3	–	0.6	
			3.0	3.0	–	0.45	
		I_{OL} = 24 mA; V_I = V_{IL}	3.0	3.0	–	0.6	
I_I	Input Leakage Current	V_I = V_{CCA} or GND	0.9 – 4.5	0.9 – 4.5	−1.0	1.0	μA
I_{OFF}	Power−Off Leakage Current	$\overline{OE}$ = 0 V	0 0.9 – 4.5	0.9 – 4.5 0	−1.0 −1.0	1.0 1.0	μA
I_{CCA}	Quiescent Supply Current	V_I = V_{CCA} or GND; I_O = 0, V_{CCA} = V_{CCB}	0.9 – 4.5	0.9 – 4.5	–	2.0	μA
I_{CCB}	Quiescent Supply Current	V_I = V_{CCA} or GND; I_O = 0, V_{CCA} = V_{CCB}	0.9 – 4.5	0.9 – 4.5	–	2.0	μA
I_{CCA} + I_{CCB}	Quiescent Supply Current	V_I = V_{CCA} or GND; I_O = 0, V_{CCA} = V_{CCB}	0.9 – 4.5	0.9 – 4.5	–	4.0	μA
ΔI_{CCA}	Increase in I_{CC} per Input Voltage, Other Inputs at V_{CCA} or GND	V_I = V_{CCA} – 0.6 V; V_I = V_{CCA} or GND	4.5 3.6	4.5 3.6	–	10 5.0	μA
ΔI_{CCB}	Increase in I_{CC} per Input Voltage, Other Inputs at V_{CCA} or GND	V_I = V_{CCA} – 0.6 V; V_I = V_{CCA} or GND	4.5 3.6	4.5 3.6	–	10 5.0	μA
I_{OZ}	I/O Tri−State Output Leakage Current	T_A = 25°C, $\overline{OE}$ = 0 V	0.9 – 4.5	0.9 – 4.5	−1.0	1.0	μA

TOTAL STATIC POWER CONSUMPTION (I_{CCA} + I_{CCB})

	−40°C to +85°C										
	V_{CCB} (V)										
	4.5		3.3		2.8		1.8		0.9		
V_{CCA} (V)	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit
4.5		2		2		2		2		< 1.5	μA
3.3		2		2		2		2		< 1.5	μA
2.8		< 2		< 1		< 1		< 0.5		< 0.5	μA
1.8		< 1		< 1		< 0.5		< 0.5		< 0.5	μA
0.9		< 0.5		< 0.5		< 0.5		< 0.5		< 0.5	μA

NOTE: Connect ground before applying supply voltage V_{CCA} or V_{CCB}. This device is designed with the feature that the power−up sequence of V_{CCA} and V_{CCB} will not damage the IC.

AC ELECTRICAL CHARACTERISTICS

			−40°C to +85°C										
			V_{CCB} (V)										
			4.5		3.3		2.8		1.8		1.2		
Symbol	Parameter	V_{CCA} (V)	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit
t_{PLH}, t_{PHL} (Note 1)	Propagation Delay, A_n to B_n	4.5		1.6		1.8		2.0		2.1		2.3	nS
		3.3		1.7		1.9		2.1		2.3		2.6	
		2.8		1.9		2.1		2.3		2.5		2.8	
		1.8		2.1		2.4		2.5		2.7		3.0	
		1.2		2.4		2.7		2.8		3.0		3.3	
t_{PZH}, t_{PZL} (Note 1)	Output Enable, $\overline{OE}$ to B_n	4.5		2.6		3.8		4.0		4.1		4.3	nS
		3.3		3.7		3.9		4.1		4.3		4.6	
		2.5		3.9		4.1		4.3		4.5		4.8	
		1.8		4.1		4.4		4.5		4.7		5.0	
		1.2		4.4		4.7		4.8		5.0		5.3	
t_{PHZ}, t_{PLZ} (Note 1)	Output Disable, $\overline{OE}$ to B_n	4.5		2.6		3.8		4.0		4.1		4.3	nS
		3.3		3.7		3.9		4.1		4.3		4.6	
		2.5		3.9		4.1		4.3		4.5		4.8	
		1.8		4.1		4.4		4.5		4.7		5.0	
		1.2		4.4		4.7		4.8		5.0		5.3	
t_{OSHL}, t_{OSLH} (Note 1)	Output to Output Skew, Time	4.5		0.15		0.15		0.15		0.15		0.15	nS
		3.3		0.15		0.15		0.15		0.15		0.15	
		2.5		0.15		0.15		0.15		0.15		0.15	
		1.8		0.15		0.15		0.15		0.15		0.15	
		1.2		0.15		0.15		0.15		0.15		0.15	

1. Propagation delays defined per Figure 3.

CAPACITANCE

Symbol	Parameter	Test Conditions	Typ (Note 2)	Unit
C_{IN}	Control Pin Input Capacitance	V_{CCA} = V_{CCB} = 3.3 V, V_I = 0 V or $V_{CCA/B}$	3.5	pF
$C_{I/O}$	I/O Pin Input Capacitance	V_{CCA} = V_{CCB} = 3.3 V, V_I = 0 V or $V_{CCA/B}$	5.0	pF
C_{PD}	Power Dissipation Capacitance	V_{CCA} = V_{CCB} = 3.3 V, V_I = 0 V or V_{CCA}, f = 10 MHz	20	pF

2. Typical values are at T_A = +25°C.
3. C_{PD} is defined as the value of the IC's equivalent capacitance from which the operating current can be calculated from: $I_{CC(operating)} \cong C_{PD} \times V_{CC} \times f_{IN} \times N_{SW}$ where $I_{CC} = I_{CCA} + I_{CCB}$ and N_{SW} = total number of outputs switching.

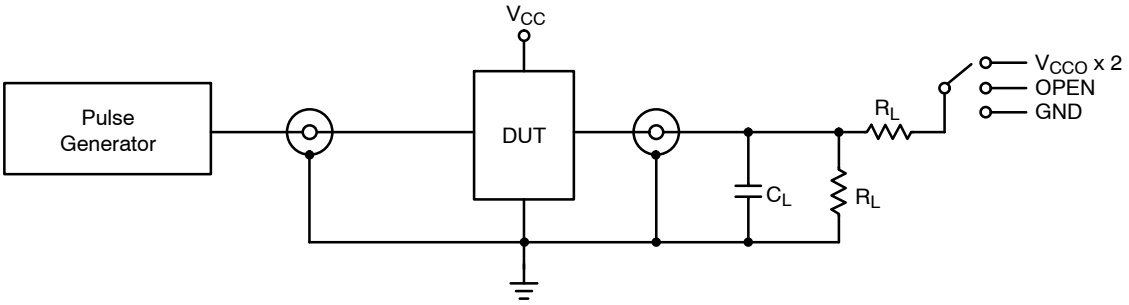
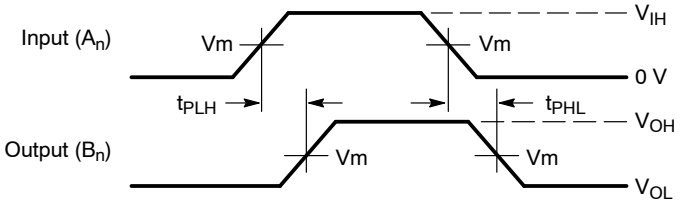
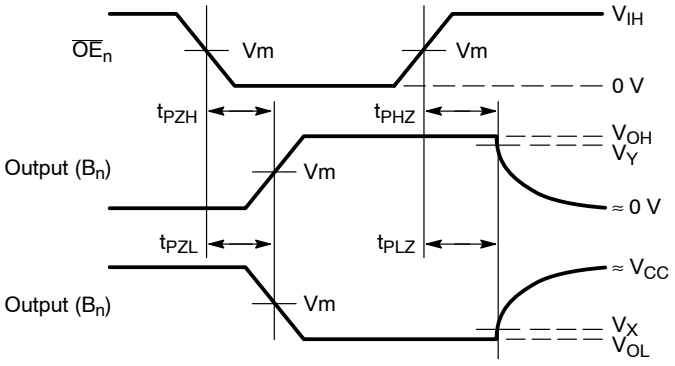


Figure 3. AC (Propagation Delay) Test Circuit

Test	Switch
t_{PLH}, t_{PHL}	OPEN
t_{PLZ}, t_{PZL}	V_{CCO} x 2
t_{PHZ}, t_{PZH}	GND
C_L = 15 pF or equivalent (includes probe and jig capacitance) R_L = 2 kΩ or equivalent Z_{OUT} of pulse generator = 50 Ω	



Waveform 1 – Propagation Delays
$t_R = t_F$ = 2.0 ns, 10% to 90%; f = 1 MHz; t_W = 500 ns



Waveform 2 – Output Enable and Disable Times
$t_R = t_F$ = 2.0 ns, 10% to 90%; f = 1 MHz; t_W = 500 ns

Figure 4. AC (Propagation Delay) Test Circuit Waveforms

Symbol	V_{CC}				
	3.0 V – 4.5 V	2.3 V – 2.7 V	1.65 V – 1.95 V	1.4 V – 1.6 V	0.9 V – 1.3 V
V_{mA}	$V_{CCA}/2$	$V_{CCA}/2$	$V_{CCA}/2$	$V_{CCA}/2$	$V_{CCA}/2$
V_{mB}	$V_{CCB}/2$	$V_{CCB}/2$	$V_{CCB}/2$	$V_{CCB}/2$	$V_{CCB}/2$
V_X	V_{OL} x 0.1	V_{OL} x 0.1	V_{OL} x 0.1	V_{OL} x 0.1	V_{OL} x 0.1
V_Y	V_{OH} x 0.9	V_{OH} x 0.9	V_{OH} x 0.9	V_{OH} x 0.9	V_{OH} x 0.9

ORDERING INFORMATION

Device	Package	Shipping†
NLSV8T244MUTAG	UQFN20 (Pb−Free)	3000 / Tape & Reel
NLSV8T244DTR2G	TSSOP−20 (Pb−Free)	2500 / Tape & Reel
NLSV8T244DWR2G	SOIC−20 (Pb−Free)	1000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

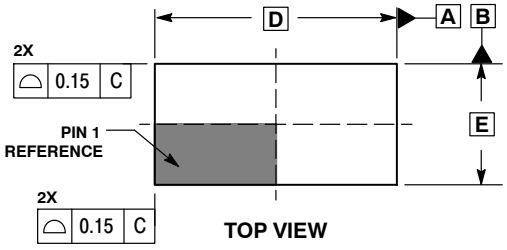
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

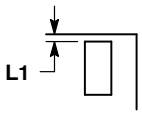
ON Semiconductor®

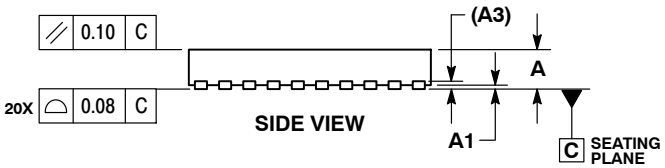
UDFN20 4x2, 0.4P
CASE 517AK−01
ISSUE O

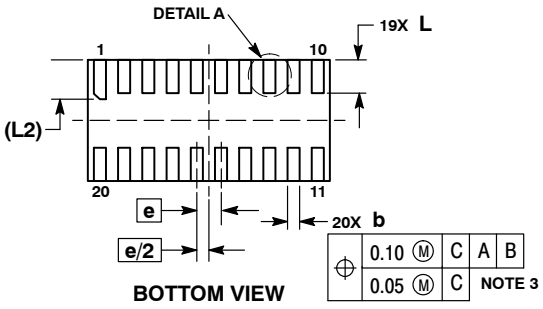
DATE 14 NOV 2006

SCALE 4:1









NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. MOLD FLASH ALLOWED ON TERMINALS ALONG EDGE OF PACKAGE. FLASH MAY NOT EXCEED 0.03 ONTO BOTTOM SURFACE OF TERMINALS.
5. DETAIL A SHOWS OPTIONAL CONSTRUCTION FOR TERMINALS.

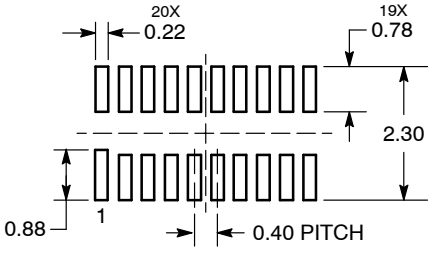
	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13 REF	
b	0.15	0.25
D	4.00 BSC	
E	2.00 BSC	
e	0.40 BSC	
L	0.50	0.60
L1	0.00	0.03
L2	0.60	0.70

GENERIC MARKING DIAGRAM*

XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

MOUNTING FOOTPRINT SOLDERMASK DEFINED

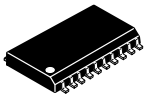


DIMENSIONS: MILLIMETERS

DOCUMENT NUMBER:	98AON23419D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	UDFN20 4 X 2, 0.4P	PAGE 1 OF 1

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

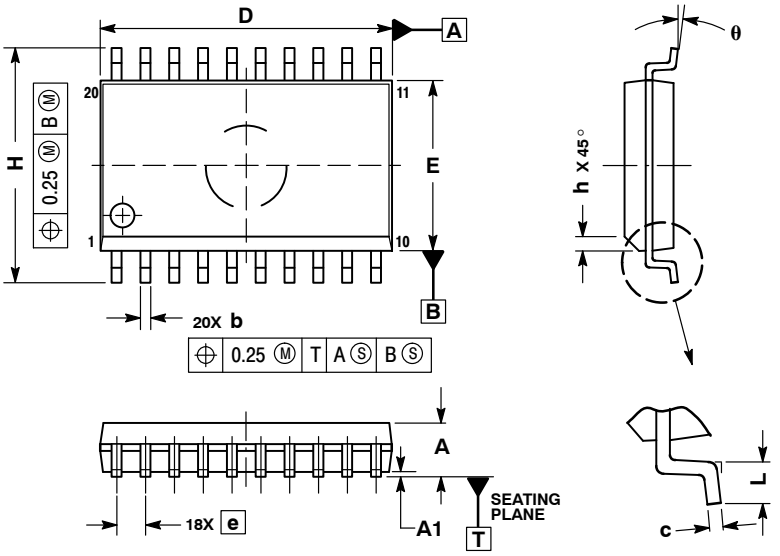
ON Semiconductor®



SOIC−20 WB
CASE 751D−05
ISSUE H

DATE 22 APR 2015

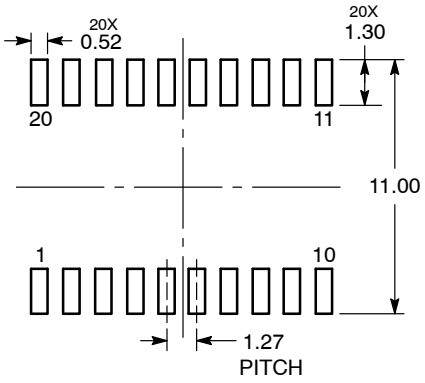
SCALE 1:1



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
b	0.35	0.49
c	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

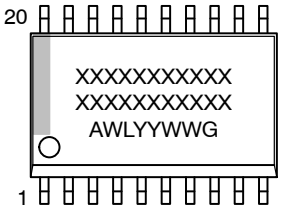
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

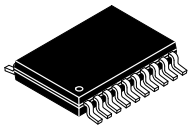
DOCUMENT NUMBER:	**98ASB42343B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**SOIC−20 WB**	**PAGE 1 OF 1**

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

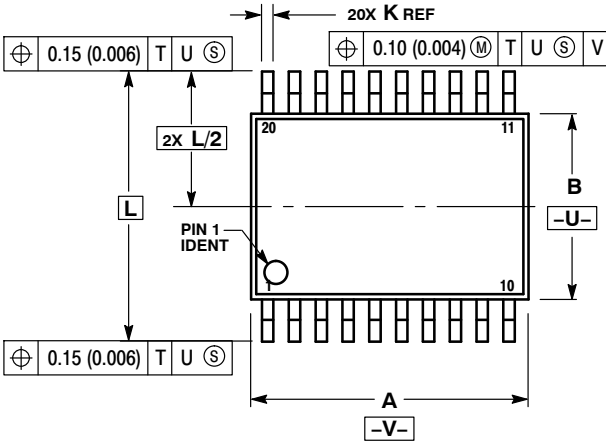
ON Semiconductor®

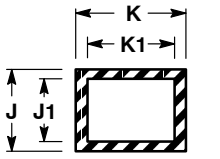
TSSOP−20 WB
CASE 948E
ISSUE D

DATE 17 FEB 2016

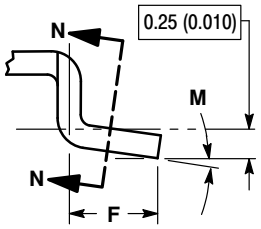


SCALE 2:1

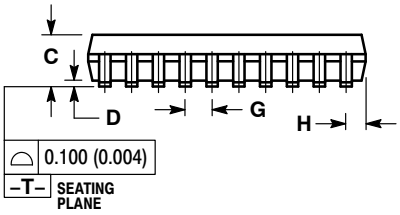


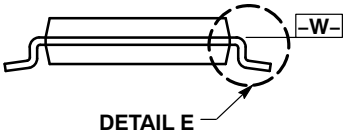


SECTION N−N



DETAIL E

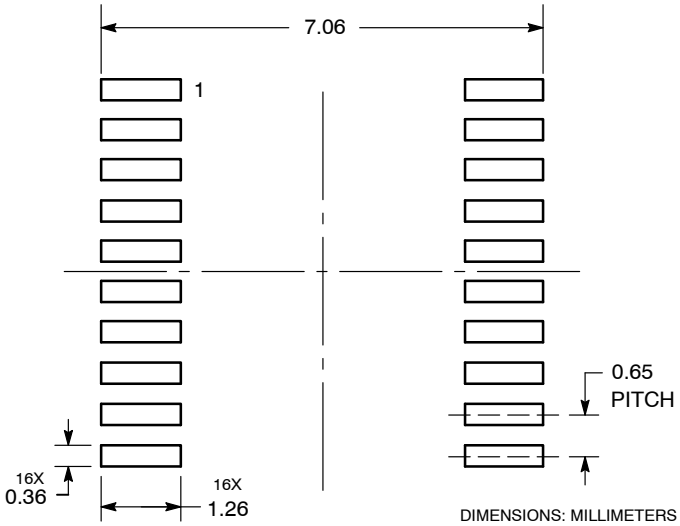




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

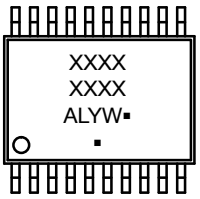
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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DESCRIPTION:	**TSSOP−20 WB**	**PAGE 1 OF 1**

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