

74HC244

Octal 3-State Noninverting Buffer/Line Driver/ Line Receiver

High-Performance Silicon-Gate CMOS

The 74HC244 is identical in pinout to the LS244. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This octal noninverting buffer/line driver/line receiver is designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. The device has noninverting outputs and two active-low output enables.

The HC244 is similar in function to the HC240A.

Features

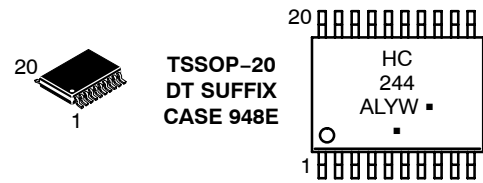
- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- ESD Performance: HBM > 2000 V; Machine Model > 200 V
- Chip Complexity: 136 FETs or 34 Equivalent Gates
- This is a Pb-Free Device



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MARKING DIAGRAM



HC244 = Specific Device Code

A = Assembly Location

L = Wafer Lot

Y = Year

W = Work Week

▪ = Pb-Free Package

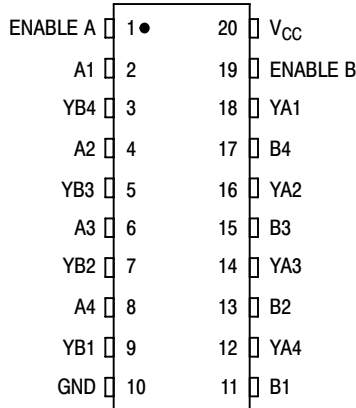
(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

74HC244

PIN ASSIGNMENT

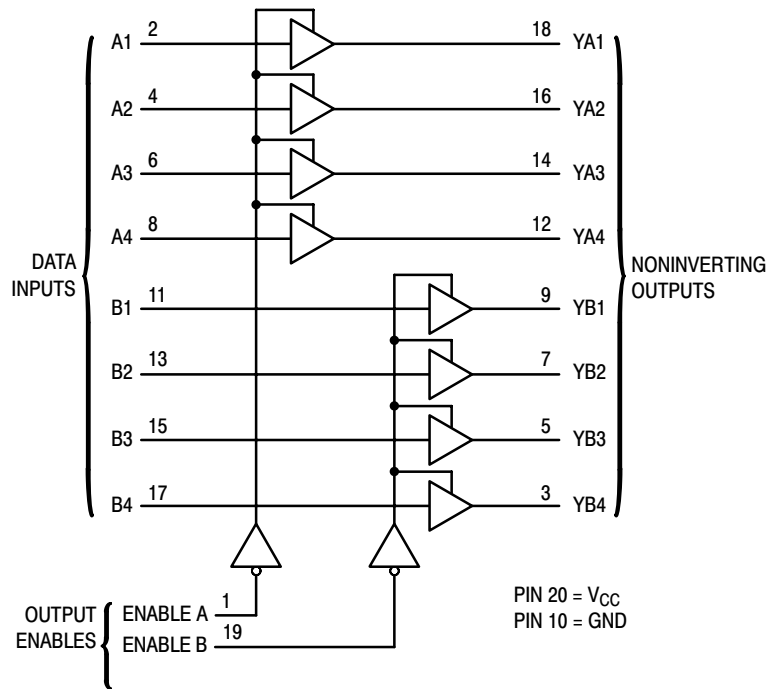


FUNCTION TABLE

Inputs		Outputs
Enable A, Enable B	A, B	YA, YB
L	L	L
L	H	H
H	X	Z

Z = high impedance

LOGIC DIAGRAM



ORDERING INFORMATION

Device	Package	Shipping†
74HC244DTR2G	TSSOP-20*	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*This package is inherently Pb-Free.

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	- 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	- 0.5 to $V_{CC} + 0.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	- 0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, TSSOP Package†	450	mW
T_{stg}	Storage Temperature	- 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (TSSOP Package)	260	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

†Derating — TSSOP Package: - 6.1 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

74HC244

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	0	1000 500 400	ns
	$V_{CC} = 2.0\text{ V}$	0	1000	ns
	$V_{CC} = 4.5\text{ V}$	0	500	ns
	$V_{CC} = 6.0\text{ V}$	0	400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} (V)	Guaranteed Limit			Unit
				-55 to 25°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = V_{CC} - 0.1\text{ V}$ $ I_{out} \leq 20\ \mu\text{A}$	2.0	1.5	1.5	1.5	V
			3.0	2.1	2.1	2.1	
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1\text{ V}$ $ I_{out} \leq 20\ \mu\text{A}$	2.0	0.5	0.5	0.5	V
			3.0	0.9	0.9	0.9	
			4.5	1.35	1.35	1.35	
			6.0	1.8	1.8	1.8	
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH}$ $ I_{out} \leq 20\ \mu\text{A}$	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
			$V_{in} = V_{IH}$ $ I_{out} \leq 2.4\text{ mA}$ $ I_{out} \leq 6.0\text{ mA}$ $ I_{out} \leq 7.8\text{ mA}$	3.0	2.48	2.34	
			4.5	3.98	3.84	3.7	
			6.0	5.48	5.34	5.2	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IL}$ $ I_{out} \leq 20\ \mu\text{A}$	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
			$V_{in} = V_{IL}$ $ I_{out} \leq 2.4\text{ mA}$ $ I_{out} \leq 6.0\text{ mA}$ $ I_{out} \leq 7.8\text{ mA}$	3.0	0.26	0.33	
			4.5	0.26	0.33	0.4	
			6.0	0.26	0.33	0.4	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State $V_{in} = V_{IL}$ or V_{IH} $V_{out} = V_{CC}$ or GND	6.0	±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0\ \mu\text{A}$	6.0	4.0	40	40	μA

NOTE: Information on typical parametric values and high frequency or heavy load considerations can be found in Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

74HC244

AC ELECTRICAL CHARACTERISTICS ($C_L = 50 \text{ pF}$, Input $t_r = t_f = 6 \text{ ns}$)

Symbol	Parameter	V_{CC} (V)	Guaranteed Limit			Unit
			- 55 to 25°C	$\leq 85^\circ\text{C}$	$\leq 125^\circ\text{C}$	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, A to YA or B to YB (Figures 1 and 3)	2.0	96	115	135	ns
		3.0	50	60	70	
		4.5	18	23	27	
		6.0	15	20	23	
t_{PLZ} , t_{PHZ}	Maximum Propagation Delay, Output Enable to YA or YB (Figures 2 and 4)	2.0	110	140	165	ns
		3.0	60	70	80	
		4.5	22	28	33	
		6.0	19	24	28	
t_{PZL} , t_{PZH}	Maximum Propagation Delay, Output Enable to YA or YB (Figures 2 and 4)	2.0	110	140	165	ns
		3.0	60	70	80	
		4.5	22	28	33	
		6.0	19	24	28	
t_{TLH} , t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0	60	75	90	ns
		3.0	23	27	32	
		4.5	12	15	18	
		6.0	10	13	15	
C_{in}	Maximum Input Capacitance	-	10	10	10	pF
C_{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State)	-	15	15	15	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

C_{PD}	Power Dissipation Capacitance (Per Buffer)*	Typical @ 25°C, $V_{CC} = 5.0 \text{ V}$	
		34	pF

* Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

SWITCHING WAVEFORMS

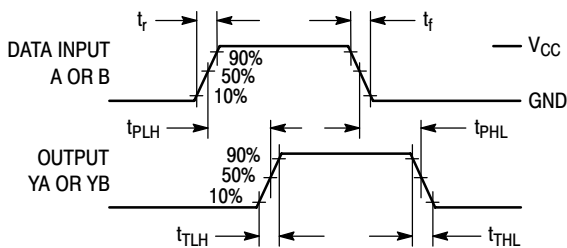


Figure 1.

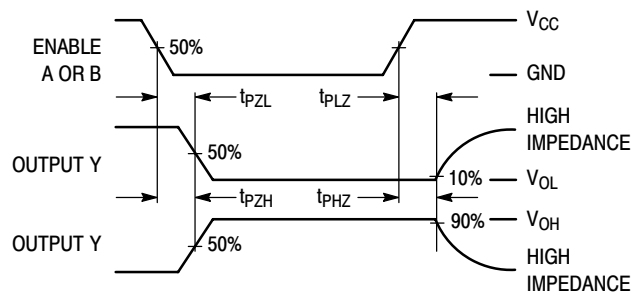
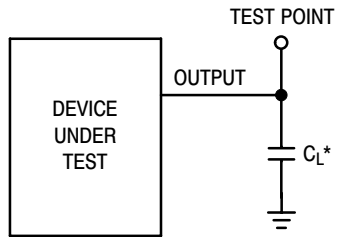


Figure 2.

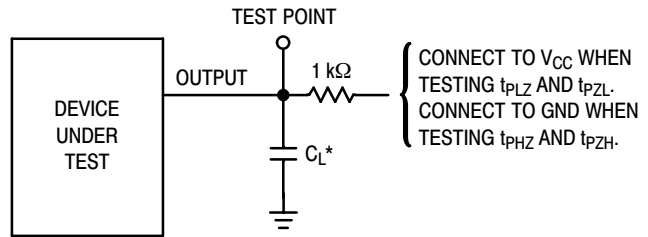
74HC244

TEST CIRCUITS



*Includes all probe and jig capacitance

Figure 3. Test Circuit



*Includes all probe and jig capacitance

Figure 4. Test Circuit

PIN DESCRIPTIONS

INPUTS

A1, A2, A3, A4, B1, B2, B3, B4
(Pins 2, 4, 6, 8, 11, 13, 15, 17)

Data input pins. Data on these pins appear in noninverted form on the corresponding Y outputs, when the outputs are enabled.

CONTROLS

Enable A, Enable B (Pins 1, 19)

Output enables (active-low). When a low level is applied to these pins, the outputs are enabled and the devices

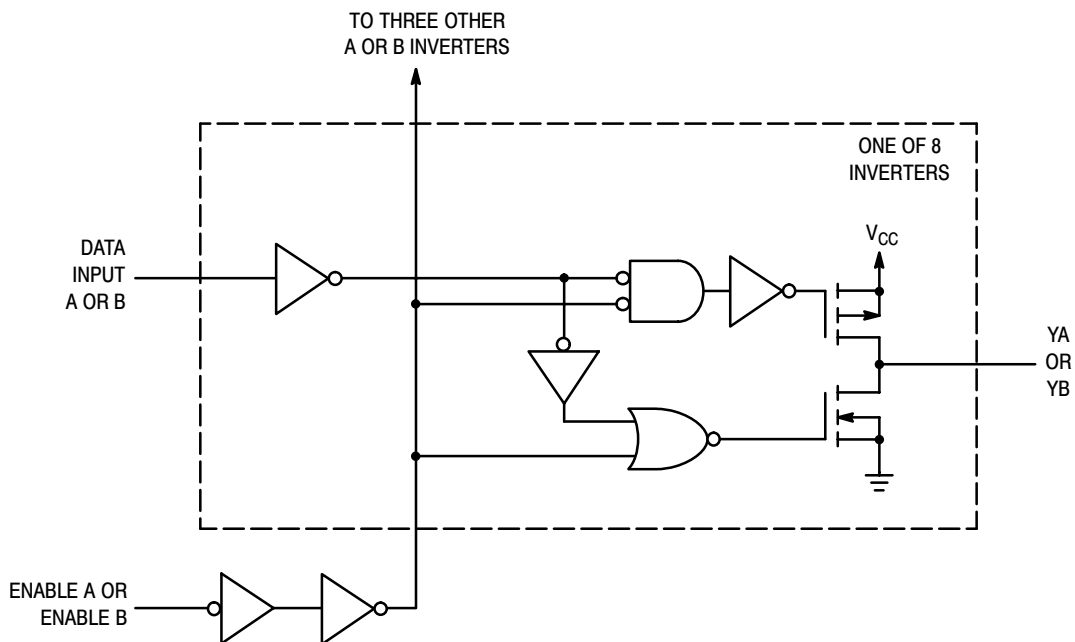
function as noninverting buffers. When a high level is applied, the outputs assume the high impedance state.

OUTPUTS

YA1, YA2, YA3, YA4, YB1, YB2, YB3, YB4
(Pins 18, 16, 14, 12, 9, 7, 5, 3)

Device outputs. Depending upon the state of the output-enable pins, these outputs are either noninverting outputs or high-impedance outputs.

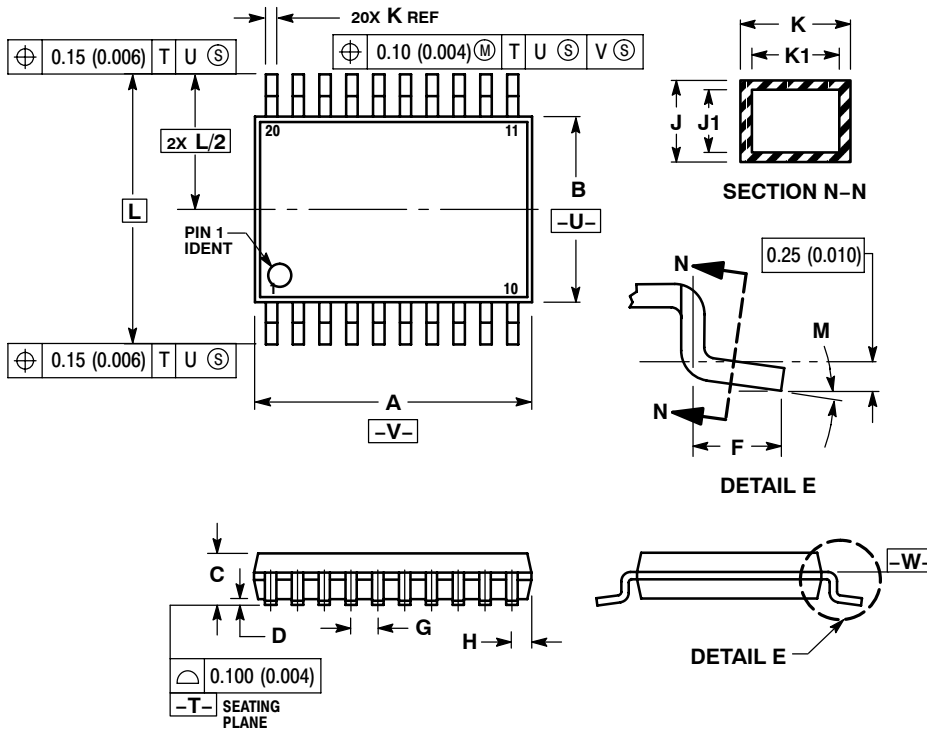
LOGIC DETAIL



74HC244

PACKAGE DIMENSIONS

TSSOP-20
CASE 948E-02
ISSUE C

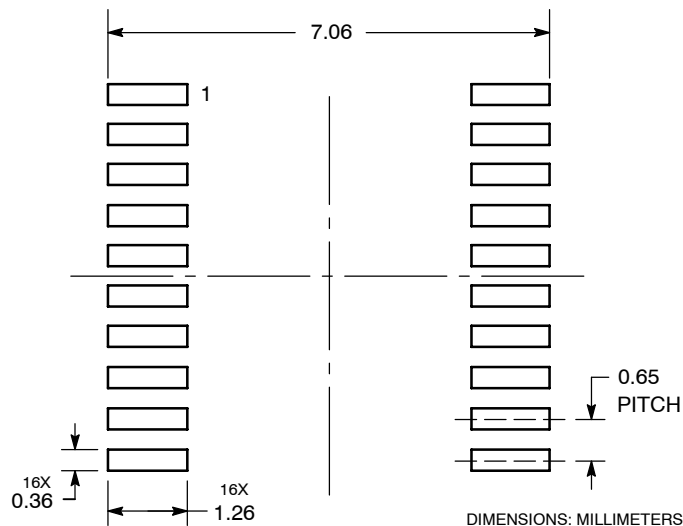


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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