

# ON Semiconductor

## Is Now

# onsemi™

To learn more about onsemi™, please visit our website at  
[www.onsemi.com](http://www.onsemi.com)

---

**onsemi** and **onsemi** and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi** product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner. Other names and brands may be claimed as the property of others.

# KAF-1603

## 1536 (H) x 1024 (V) Full Frame CCD Image Sensor

### Description

The KAF-1603 Image Sensor is a high performance monochrome area CCD (charge-coupled device) image sensor with 1536 (H) x 1024 (V) photoactive pixels designed for a wide range of image sensing applications.

The sensor incorporates true two-phase CCD technology, simplifying the support circuits required to drive the sensor as well as reducing dark current without compromising charge capacity. The sensor also utilizes the TRUESENSE Transparent Gate Electrode to improve sensitivity compared to the use of a standard front side illuminated polysilicon electrode.

Optional microlenses focus the majority of the light through the transparent gate, increasing the optical response further.

Table 1. GENERAL SPECIFICATIONS

Parameter	Typical Value
Architecture	Full Frame CCD
Total Number of Pixels	1552 (H) x 1032 (V)
Number of Active Pixels	1536 (H) x 1024 (V) = approx. 1.6 Mp
Pixel Size	9.0 $\mu\text{m}$ (H) x 9.0 $\mu\text{m}$ (V)
Active Image Size	13.8 mm (H) x 9.2 mm (V) 16.6 mm (Diagonal) 1" Optical Format
Die Size	15.5 mm (H) x 10.0 mm (V)
Aspect Ratio	3:2
Saturation Signal	100,000 electrons
Output Sensitivity	10 $\mu\text{V}/\text{e}^-$
Quantum Efficiency (with Microlens)	Peak: 77% 400 nm: 45%
Quantum Efficiency (no Microlens)	Peak: 65% 400 nm: 30%
Read Noise	15 electrons
Dark Current	< 10 pA/cm <sup>2</sup>
Dark Current Doubling Temperature	6.3°C
Dynamic Range	74 dB
Charge Transfer Efficiency	> 0.99999
Blooming Suppression	None
Maximum Data Rate	10 MHz
Package	CERDIP Package (Sidebrazed)
Cover Glass	Clear or AR Coated, 2 Sides

NOTE: Parameters above are specified at T = 25°C unless otherwise noted.



ON Semiconductor®

[www.onsemi.com](http://www.onsemi.com)

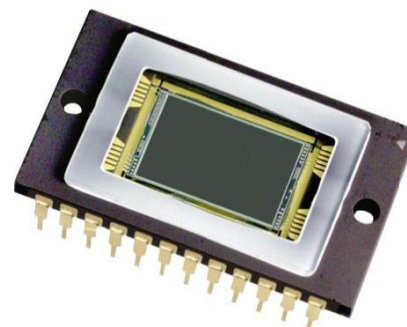


Figure 1. KAF-1603 CCD Image Sensor

### Features

- True Two Phase Full Frame Architecture
- TRUESENSE Transparent Gate Electrode for High Sensitivity

### Applications

- Scientific Imaging

### ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

# KAF-1603

## ORDERING INFORMATION

**Table 2. ORDERING INFORMATION – KAF-1603 IMAGE SENSOR**

Part Number	Description	Marking Code
KAF-1603-ABA-CD-B2	Monochrome, Telecentric Microlens, CERDIP Package (Sidebrazed), Clear Cover Glass with AR Coating (Both Sides), Grade 2	KAF-1603-ABA Serial Number
KAF-1603-ABA-CD-AE	Monochrome, Telecentric Microlens, CERDIP Package (Sidebrazed), Clear Cover Glass with AR Coating (Both Sides), Engineering Sample	
KAF-1603-ABA-CP-B2	Monochrome, Telecentric Microlens, CERDIP Package (Sidebrazed), Taped Clear Cover Glass (No Coatings), Grade 2	
KAF-1603-ABA-CP-AE	Monochrome, Telecentric Microlens, CERDIP Package (Sidebrazed), Taped Clear Cover Glass (No Coatings), Engineering Sample	
KAF-1603-AAA-CP-B2	Monochrome, No Microlens, CERDIP Package (Sidebrazed), Taped Clear Cover Glass (No Coatings), Grade 2	KAF-1603-AAA Serial Number
KAF-1603-AAA-CP-AE	Monochrome, No Microlens, CERDIP Package (Sidebrazed), Taped Clear Cover Glass (No Coatings), Engineering Sample	

**Table 3. ORDERING INFORMATION – EVALUATION SUPPORT**

Part Number	Description
KAF-1603-12-5-A-EVK	Evaluation Board (Complete Kit)

See the ON Semiconductor *Device Nomenclature* document (TND310/D) for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at [www.onsemi.com](http://www.onsemi.com).

DEVICE DESCRIPTION

Architecture

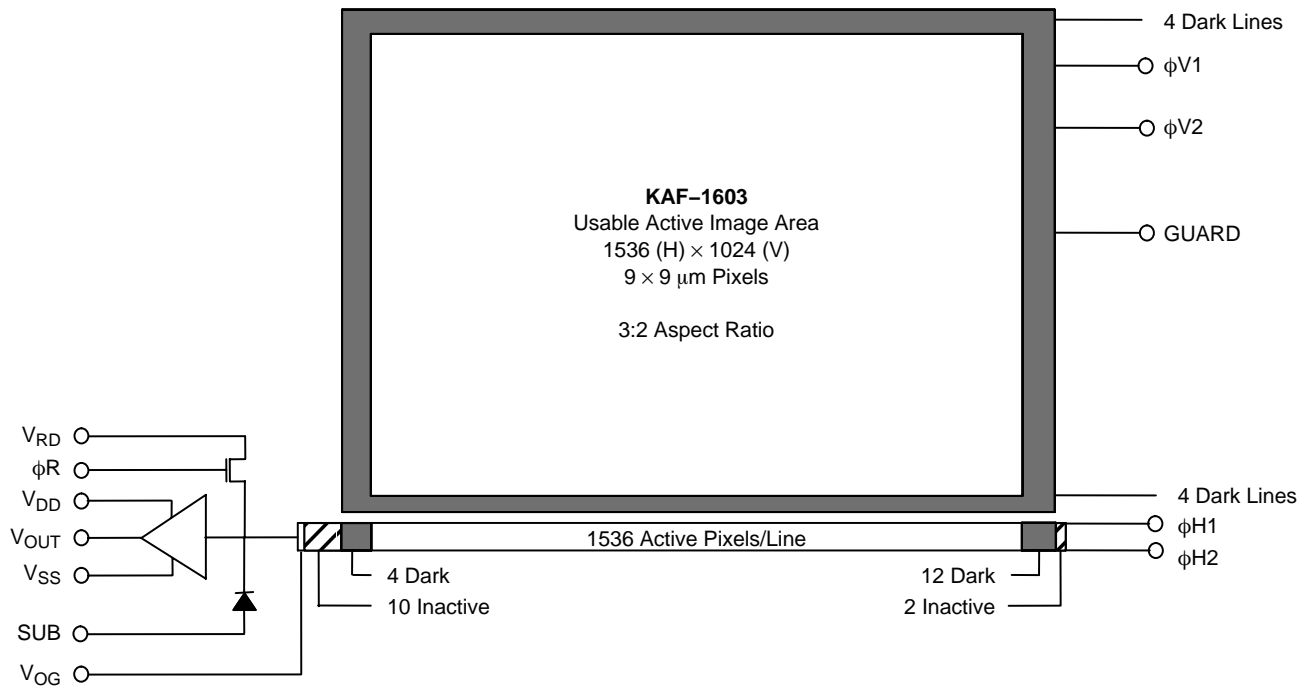


Figure 2. Block Diagram

The sensor consists of 1,552 parallel (vertical) CCD shift registers each 1,032 elements long. These registers act as both the photosensitive elements and as the transport circuits that allow the image to be sequentially read out of the sensor. The parallel (vertical) CCD registers transfer the image one line at a time into a single 1,564 element (horizontal) CCD shift register. The horizontal register transfers the charge to a single output amplifier. The output amplifier is a two-stage source follower that converts the photo-generated charge to a voltage for each pixel.

Microlenses

Micro lenses are formed along each row. They are effectively half of a cylinder centered on the transparent gates, extending continuously in the row direction. They act to direct the photons away from the polysilicon gate and through the transparent gate. This increases the response, especially at the shorter wavelengths (< 600 nm).

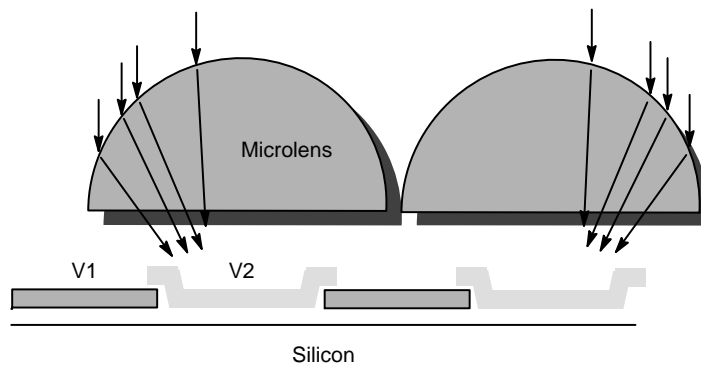


Figure 3. Microlens Cross-Section

## *Output Structure*

Charge presented to the floating diffusion is converted into a voltage and current amplified in order to drive off-chip loads. The resulting voltage change seen at the output is linearly related to the amount of charge placed on the floating diffusion. Once the signal has been sampled by the system electronics, the reset gate ( $\phi_R$ ) is clocked to remove the signal, and the floating diffusion is reset to the potential applied by  $V_{rd}$  (see Figure 4). More signal at the floating diffusion reduces the voltage seen at the output pin. In order to activate the output structure, an off-chip load must be added to the  $V_{out}$  pin of the device such as shown in Figure 5.

## *Dark Reference Pixels*

There are 4 light shielded pixels at the beginning of each line, and 12 at the end. There are 4 dark lines at the start of every frame and 4 dark lines at the end of each frame. Under normal circumstances, these pixels do not respond to light. However, dark reference pixels in close proximity to an active pixel can scavenge signal depending on light intensity and wavelength and therefore will not represent the true dark signal.

## *Dummy Pixels*

Within the horizontal shift register are 10 leading additional pixels that are not associated with a column of pixels within the vertical register. These pixels contain only horizontal shift register dark current signal and do not respond to light. A few leading dummy pixels may scavenge false signal depending on operating conditions. There are two more dummy pixels at the end of each line.

## **Image Acquisition**

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron-hole pairs within the sensor. These photon-induced electrons are collected locally by the formation of potential wells at each photogate or pixel site. The number of electrons collected is linearly dependent on light level and exposure time and non-linearly dependent on wavelength. When the pixel's capacity is reached, excess electrons will leak into the adjacent pixels within the same column. This is termed blooming. During the integration period, the  $\phi_{V1}$  and  $\phi_{V2}$  register clocks are held at a constant (low) level, and the sensor is illuminated. See Figure 9. The sensor must be illuminated only during the integration period. Light must not reach the sensor during the time the image is read out. This is usually accomplished with the use of a mechanical shutter or a pulsed light source.

## **Charge Transport**

Referring to Figure 10, the integrated charge from each photogate is transported to the output using a two-step process. During this readout time, the sensor needs to be protected from all light through the use of a shutter or pulsed light source. Each line (row) of charge is first moved from the vertical CCD to the horizontal CCD register using the  $\phi_{V1}$  and  $\phi_{V2}$  register clocks. The horizontal CCD is presented a new line on the falling edge of  $\phi_{V2}$  while  $\phi_{H1}$  is held high. The horizontal CCD then transports each line, pixel by pixel, to the output structure by alternately clocking the  $\phi_{H1}$  and  $\phi_{H2}$  pins in a complementary fashion. On each falling edge of  $\phi_{H2}$  a new charge packet is transferred onto a floating diffusion and sensed by the output amplifier.

Horizontal Register

Output Structure

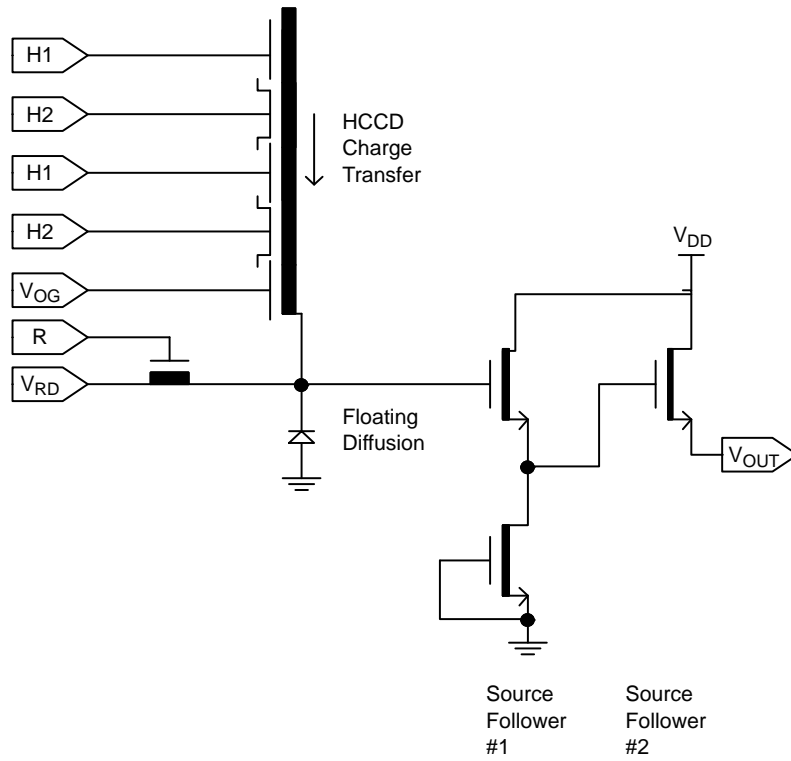


Figure 4. Output Schematic

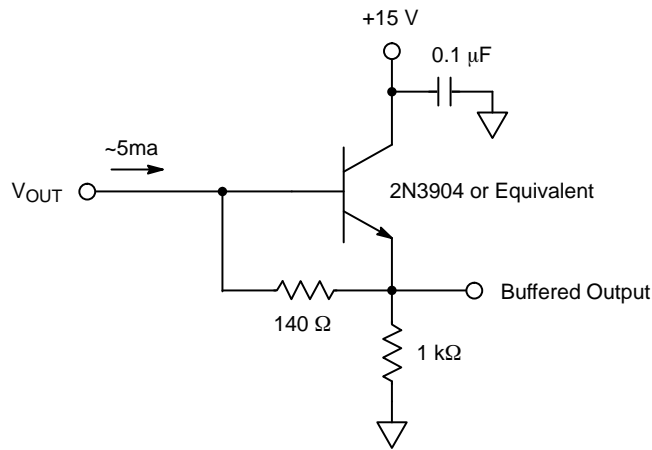
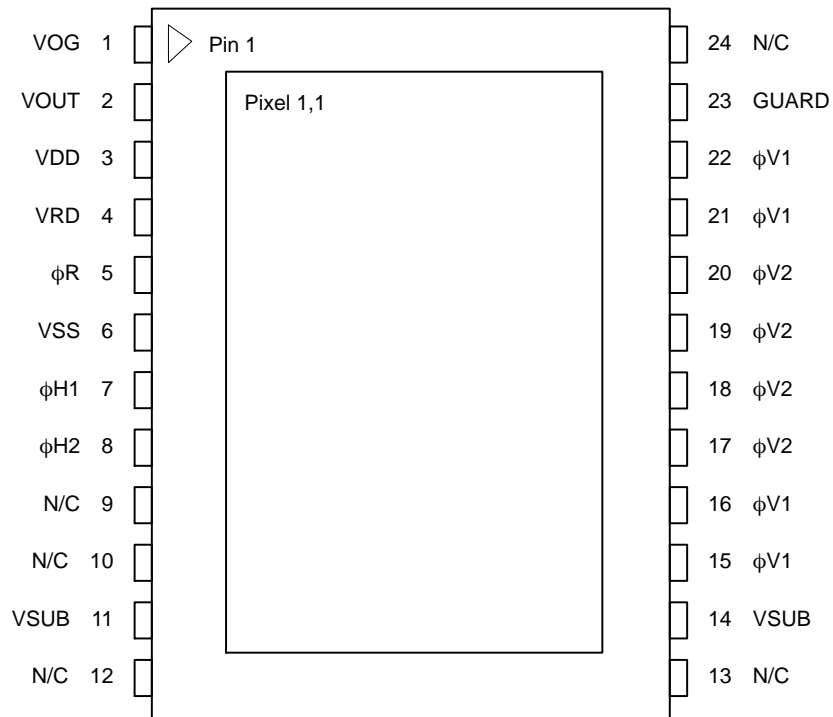


Figure 5. Output Structure Load Diagram

# KAF-1603

## Physical Description

### Pin Description and Device Orientation



**Figure 6. Pinout Diagram**

NOTE: The KAF-1603 is mechanically the same and electrically identical to the KAF-0402 sensor. It is also mechanically the same as the KAF-0261 and KAF-3200 sensors. There are some electrical differences since the KAF-0261 has two outputs and two additional clock inputs. The KAF-3200 requires that pin 11 be a “No connect” and be electrically floating. Refer to their specifications for details.

**Table 4. PIN DESCRIPTION**

Pin	Name	Description
1	VOG	Output Gate
2	VOUT	Video Output
3	VDD	Amplifier Supply
4	VRD	Reset Drain
5	φR	Reset Clock
6	VSS	Amplifier Supply Return
7	φH1	Horizontal CCD Clock – Phase 1
8	φH2	Horizontal CCD Clock – Phase 2
9	N/C	No Connection (Open Pin)
10	N/C	No Connection (Open Pin)
11	VSUB	Substrate (Ground)
12	N/C	No Connection (Open Pin)

Pin	Name	Description
13	N/C	No Connection (Open Pin)
14	VSUB	Substrate (Ground)
15	φV1	Vertical CCD Clock – Phase 1
16	φV1	Vertical CCD Clock – Phase 1
17	φV2	Vertical CCD Clock – Phase 2
18	φV2	Vertical CCD Clock – Phase 2
19	φV2	Vertical CCD Clock – Phase 2
20	φV2	Vertical CCD Clock – Phase 2
21	φV1	Vertical CCD Clock – Phase 1
22	φV1	Vertical CCD Clock – Phase 1
23	GUARD	Guard Ring
24	N/C	No Connection (Open Pin)

## IMAGING PERFORMANCE

**Table 5. TYPICAL OPERATIONAL CONDITIONS**

(All values measured at 25°C, and nominal operating conditions. These parameters exclude defective pixels.)

Description	Symbol	Min.	Nom.	Max.	Units	Notes	Verification Plan
Saturation Signal Vertical CCD Capacity Horizontal CCD Capacity Output Node Capacity	$N_{SAT}$	85,000 170,000 190,000	100,000 200,000 220,000	– – 240,000	e <sup>-</sup> /pix	1	Design <sup>9</sup>
Quantum Efficiency Microlens No Microlens		– –	– –	77% 65%	% QE		Design <sup>9</sup>
Photoresponse Non-Linearity	PRNL	–	1.0	2.0	%	2	Design <sup>9</sup>
Photoresponse Non-Uniformity	PRNU	–	0.8	–	%	3	Die <sup>8</sup>
Dark Signal	$J_{DARK}$	– –	10 2	50 10	e <sup>-</sup> /pix/sec pA/cm <sup>2</sup>	4	Die <sup>8</sup>
Dark Signal Doubling Temperature		–	6.3	7	°C		Design <sup>9</sup>
Dark Signal Non-Uniformity	DSNU	–	10	50	e <sup>-</sup> /pix/sec	5	Die <sup>8</sup>
Dynamic Range	DR	72	74	–	dB	6	Design <sup>9</sup>
Charge Transfer Efficiency	CTE	0.99997	0.99999	–			Die <sup>8</sup>
Output Amplifier DC Offset	$V_{ODC}$	$V_{RD}$	$V_{RD} + 0.5$	$V_{RD} + 1.0$	V		Die <sup>8</sup>
Output Amplifier Sensitivity	$V_{OUT}/N_{e^-}$	9	10	–	μV/e <sup>-</sup>		Design <sup>9</sup>
Output Amplifier Output Impedance	$Z_{OUT}$	180	200	220	Ω		Design <sup>9</sup>
Noise Floor	$n_{e^-}$	–	15	20	electrons	7	Die <sup>8</sup>

1. For pixel binning applications, electron capacity up to 330,000 can be achieved with modified CCD inputs.
2. Worst case deviation from straight line fit, between 2% and 90% of  $V_{SAT}$ .
3. One Sigma deviation of a  $128 \times 128$  sample when CCD illuminated uniformly at half of saturation.
4. Average of all pixels with no illumination at 25°C.
5. Average dark signal of any of  $11 \times 8$  blocks within the sensor (each block is  $128 \times 128$  pixels).
6.  $20\log(N_{SAT} / n_{e^-})$  at nominal operating frequency and 25°C.
7. Noise floor is specified at the nominal pixel frequency and excludes any dark or pattern noises. It is dominated by the output amplifier power spectrum with a bandwidth =  $5 \times$  pixel rate.
8. A parameter that is measured on every sensor during production testing.
9. A parameter that is quantified during the design verification activity.



# KAF-1603

## TYPICAL PERFORMANCE CURVES

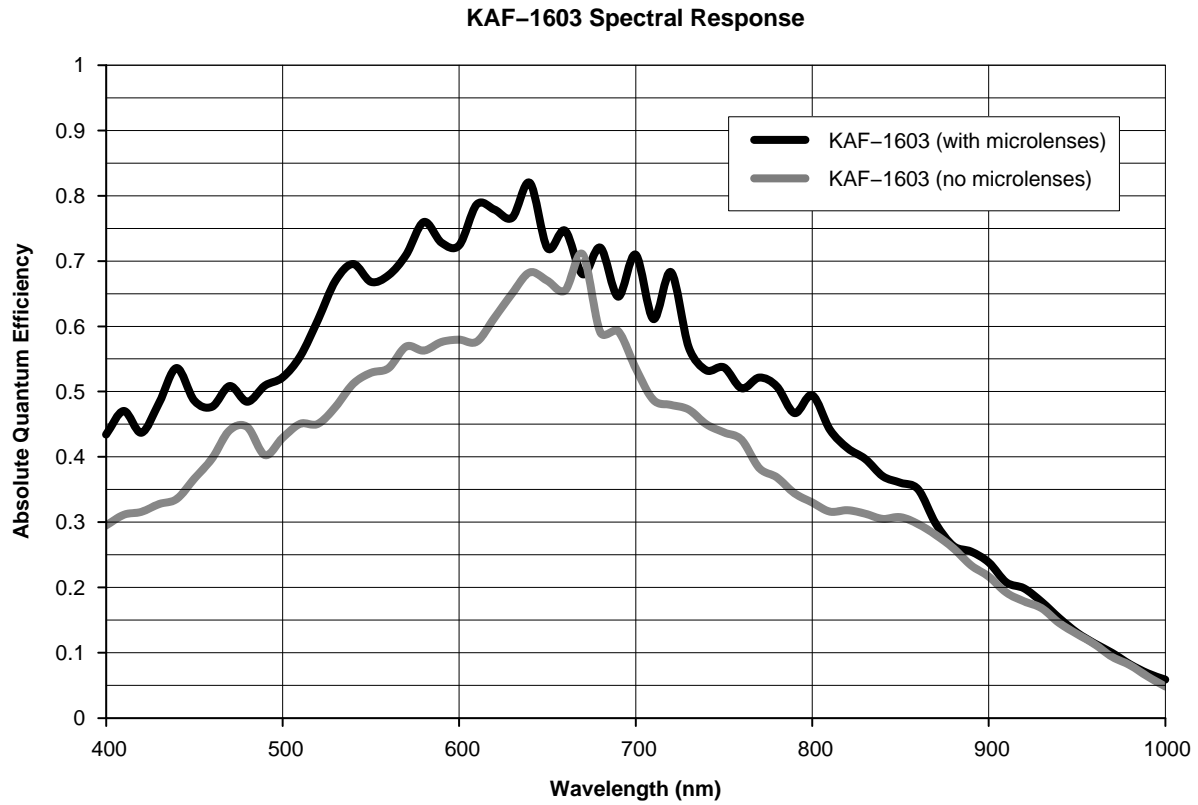


Figure 7. Typical Spectral Response

**DEFECT DEFINITIONS**

**Table 6. SPECIFICATIONS** (All tests performed at T = 25°C)

Classification	Point Defect		Cluster Defect		Column Defect	
	Total	Zone A	Total	Zone A	Total	Zone A
C2	≤ 10	≤ 5	≤ 4	≤ 2	0	0

*Point Defects*

**Dark:** A pixel which deviates by more than 6% from neighboring pixels when illuminated to 70% of saturation.

**Bright:** A pixel with a dark current greater than 5,000 e<sup>-</sup>/pixel/sec at 25°C.

*Cluster Defect*

A grouping of not more than 5 adjacent point defects.

*Column Defect*

A grouping of > 5 contiguous point defects along a single column.

A column containing a pixel with dark current > 12,000 e<sup>-</sup>/pix/sec at 25°C (Bright column).

A column that does not meet the minimum vertical CCD charge capacity (Low charge capacity column).

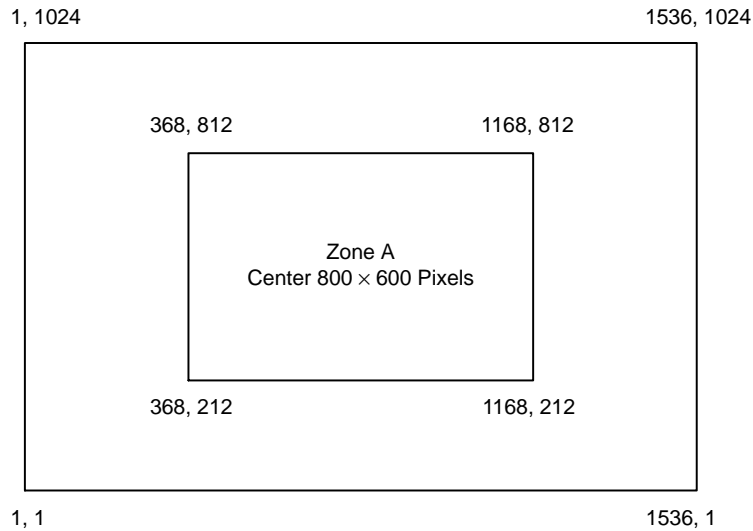
A column that loses > 250 e<sup>-</sup> under 2 ke<sup>-</sup> illumination (Trap defect).

*Neighboring Pixels*

The surrounding 128 × 128 pixels or ±64 columns/rows.

*Defect Separation*

Column and cluster defects are separated by no less than 2 pixels in any direction (excluding single pixel defects).



**Figure 8. Active Pixel Region**

**OPERATION**

**Table 7. ABSOLUTE MAXIMUM RATINGS**

Description	Symbol	Minimum	Maximum	Units
Diode Pin Voltages (Notes 10, 11)	V <sub>DIODE</sub>	0	20	V
Gate Pin Voltages (Notes 10, 12, 15)	V <sub>GATE1</sub>	-16	16	V
Output Bias Current (Note 13)	I <sub>OUT</sub>	-	-10	mA
Output Load Capacitance (Note 13)	C <sub>LOAD</sub>	-	15	pF
Storage Temperature	T	-20	80	°C
Humidity (Note 14)	RH	5	90	%

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

10. Referenced to pin V<sub>SUB</sub> or between each pin in this group.

11. Includes pins: V<sub>RD</sub>, V<sub>DD</sub>, V<sub>SS</sub>, V<sub>OUT</sub>.

12. Includes pins: φV1, φV2, φH1, φH2, V<sub>OG</sub>, V<sub>LG</sub>, φR.

13. Avoid shorting output pins to ground or any low impedance source during operation.

14. T = 25°C. Excessive humidity will degrade MTTF.

15. This sensor contains gate protection circuits to provide some protection against ESD events. The circuits will turn on when greater than 16 V appears between any two gate pins. Permanent damage can result if excessive current is allowed to flow under these conditions.

**Table 8. DC BIAS OPERATING CONDITIONS**

Description	Symbol	Minimum	Nominal	Maximum	Units	Maximum DC Current (mA)
Reset Drain	V <sub>RD</sub>	10.5	11.0	11.5	V	0.01
Output Amplifier Return	V <sub>SS</sub>	1.5	2.0	2.5	V	-0.5
Output Amplifier Supply	V <sub>DD</sub>	14.5	15	15.5	V	I <sub>OUT</sub>
Substrate	V <sub>SUB</sub>	0	0	0	V	0.01
Output Gate	V <sub>OG</sub>	3.75	4	5	V	0.01
Guard Ring	V <sub>LG</sub>	8.0	9.0	12.0	V	0.01
Video Output Current (Note 16)	I <sub>OUT</sub>	-	-5	-10	mA	-

16. An output load sink must be applied to V<sub>OUT</sub> to activate output amplifier – see Figure 5.

**AC Operating Conditions**

**Table 9. CLOCK LEVELS**

Description	Symbol	Level	Minimum	Nominal	Maximum	Units	Effective Capacitance
Vertical CCD Clock – Phase 1	φV1	Low	-10.5	-10	-9.5	V	6 nF (All φV1 Pins)
Vertical CCD Clock – Phase 1	φV1	High	0	0.5	1.0	V	6 nF (All φV1 Pins)
Vertical CCD Clock – Phase 2	φV2	Low	-10.5	-10.0	-9.5	V	6 nF (All φV2 Pins)
Vertical CCD Clock – Phase 2	φV2	High	0	0.5	1.0	V	6 nF (All φV2 Pins)
Horizontal CCD Clock – Phase 1	φH1	Low	-4.5	-4.0	-3.5	V	50 pF
Horizontal CCD Clock – Phase 1	φH1	Amplitude	9.5	10.0	10.5	V	50 pF
Horizontal CCD Clock – Phase 2	φH2	Low	-4.5	-4.0	-3.5	V	50 pF
Horizontal CCD Clock – Phase 2	φH2	Amplitude	9.5	10.0	10.5	V	50 pF
Reset Clock	φR	Low	-3.0	-2.0	-1.75	V	50 pF
Reset Clock	φR	Amplitude	5.0	6.0	7.0	V	50 pF

17. All pins draw less than 10 μA DC current.

18. Capacitance values relative to V<sub>SUB</sub>.

**TIMING**

**Table 10. REQUIREMENTS AND CHARACTERISTICS**

Description	Symbol	Minimum	Nominal	Maximum	Units
$\phi H1, \phi H2$ Clock Frequency (Notes 19, 20, 21)	$f_H$	–	4	10	MHz
Pixel Period (1 Count)	$t_{PIX}$	100	250	–	ns
$\phi H1, \phi H2$ Set-up Time	$t_{\phi HS}$	0.5	1	–	$\mu s$
$\phi V1, \phi V2$ Clock Pulse Width (Note 20)	$t_{\phi V}$	4	5	–	$\mu s$
Reset Clock Width (Note 22)	$t_{\phi R}$	10	20	–	ns
Readout Time (Note 23)	$t_{READOUT}$	178	420	–	ms
Integration Time (Note 24)	$t_{INT}$	–	–	–	
Line Time (Note 25)	$t_{LINE}$	172.4	407	–	$\mu s$

19. 50% duty cycle values.

20. CTE may degrade above the nominal frequency.

21. Rise and fall times (10/90% levels) should be limited to 5–10% of clock period. Crossover of register clocks should be between 40–60% of amplitude.

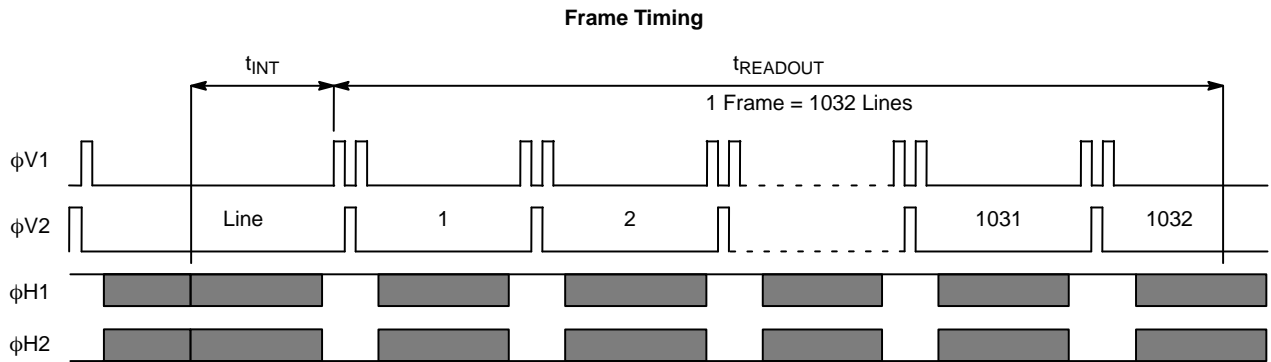
22.  $\phi R$  should be clocked continuously.

23.  $t_{READOUT} = (1032 \times t_{LINE})$

24. Integration time ( $t_{INT}$ ) is user specified. Longer integration times will degrade noise performance due to dark signal fixed pattern and shot noise.

25.  $t_{LINE} = (3 \times t_{\phi V}) + t_{\phi HS} + (1564 \times t_{PIX}) + t_{PIX}$

**Frame Timing**



**Figure 9. Frame Timing Diagram**

Line Timing and Pixel Timing

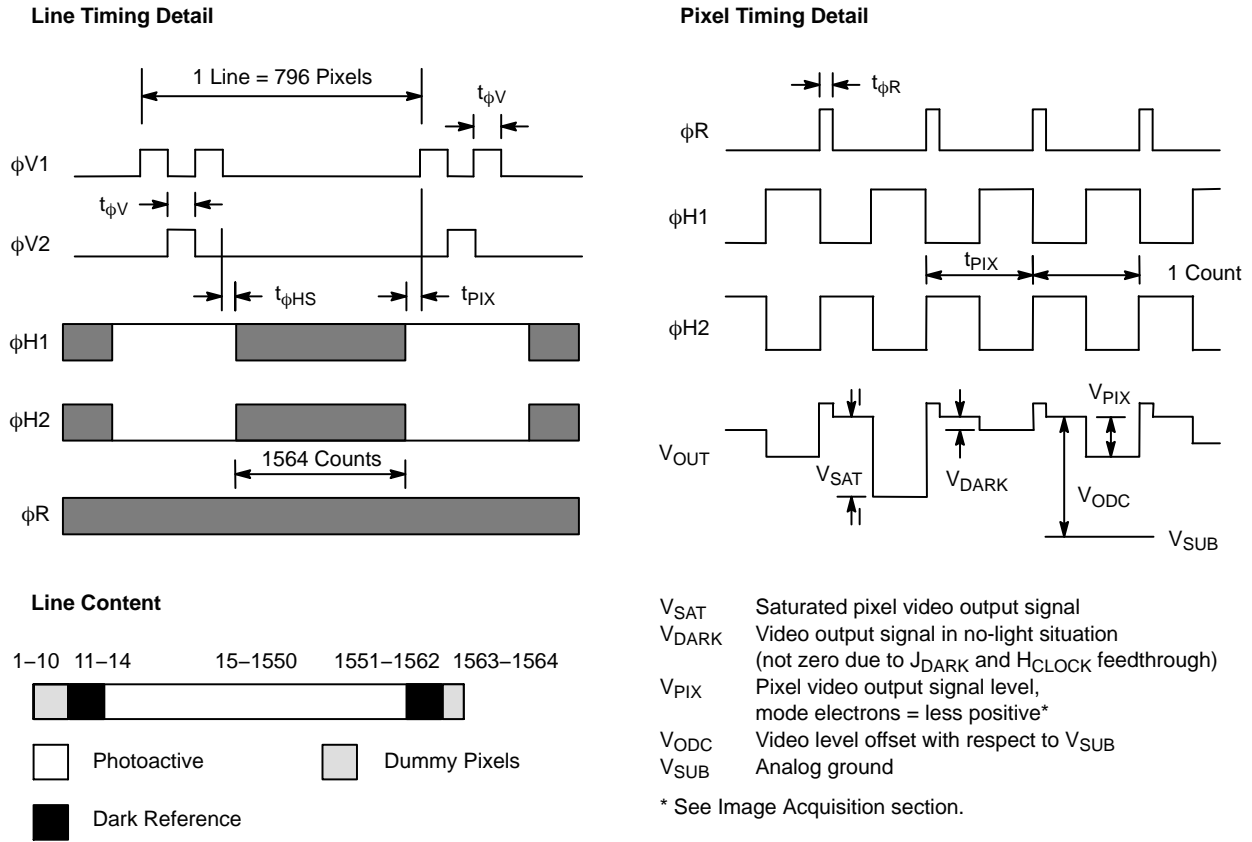


Figure 10. Timing Diagrams

## STORAGE AND HANDLING

Table 11. STORAGE CONDITIONS

Description	Symbol	Minimum	Maximum	Units
Storage Temperature (Note 26)	T <sub>ST</sub>	-20	80	°C
Operating Temperature	T <sub>OP</sub>	-60	60	°C

26. Storage toward the maximum temperature will accelerate color filter degradation.

For information on ESD and cover glass care and cleanliness, please download the *Image Sensor Handling and Best Practices* Application Note (AN52561/D) from [www.onsemi.com](http://www.onsemi.com).

For information on soldering recommendations, please download the *Soldering and Mounting Techniques Reference Manual* (SOLDERRM/D) from [www.onsemi.com](http://www.onsemi.com).

For quality and reliability information, please download the *Quality & Reliability Handbook* (HBD851/D) from [www.onsemi.com](http://www.onsemi.com).

For information on device numbering and ordering codes, please download the *Device Nomenclature* technical note (TND310/D) from [www.onsemi.com](http://www.onsemi.com).

For information on Standard terms and Conditions of Sale, please download [Terms and Conditions](http://www.onsemi.com) from [www.onsemi.com](http://www.onsemi.com).

MECHANICAL INFORMATION

Completed Assembly

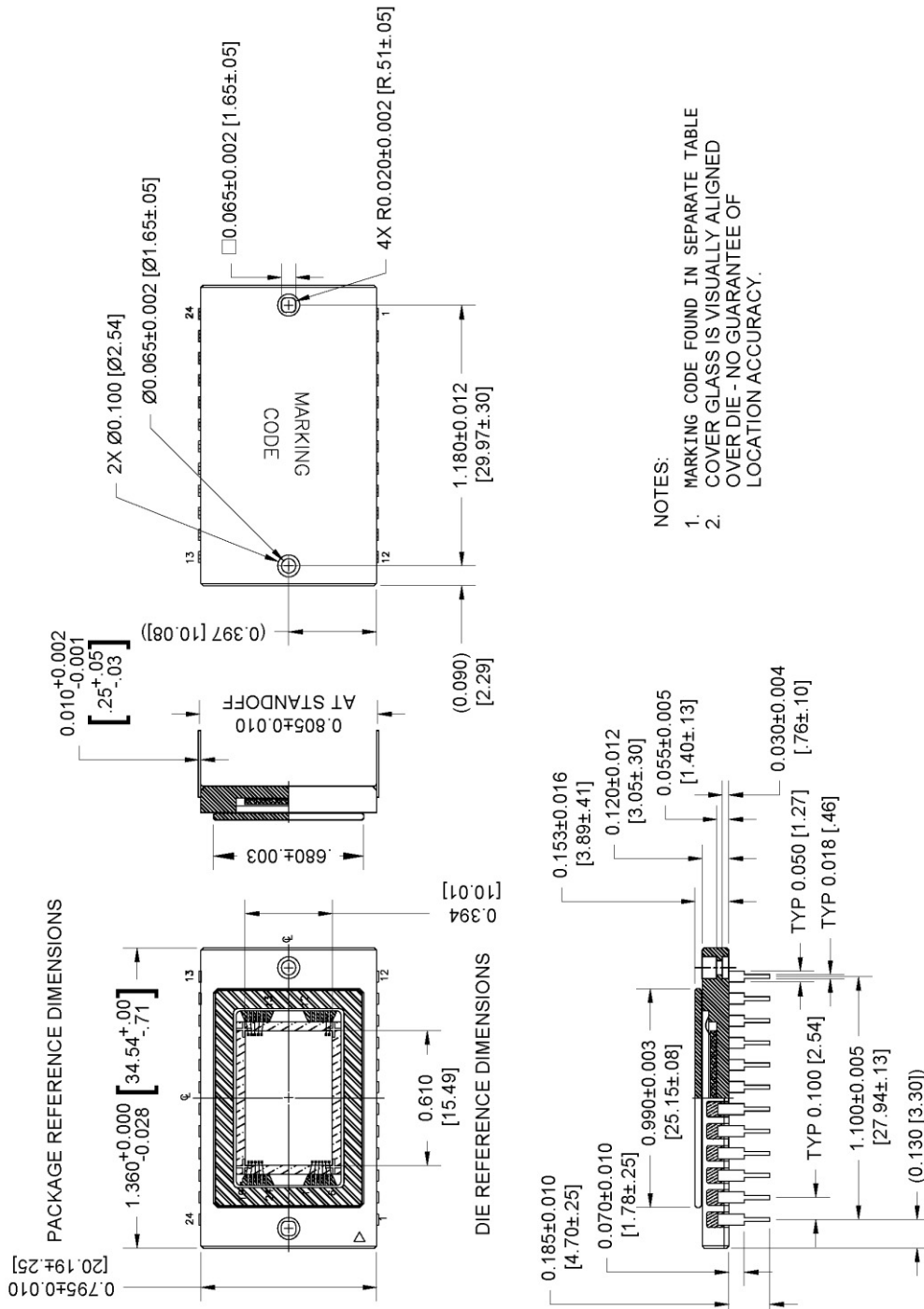


Figure 11. Completed Assembly (1 of 2)

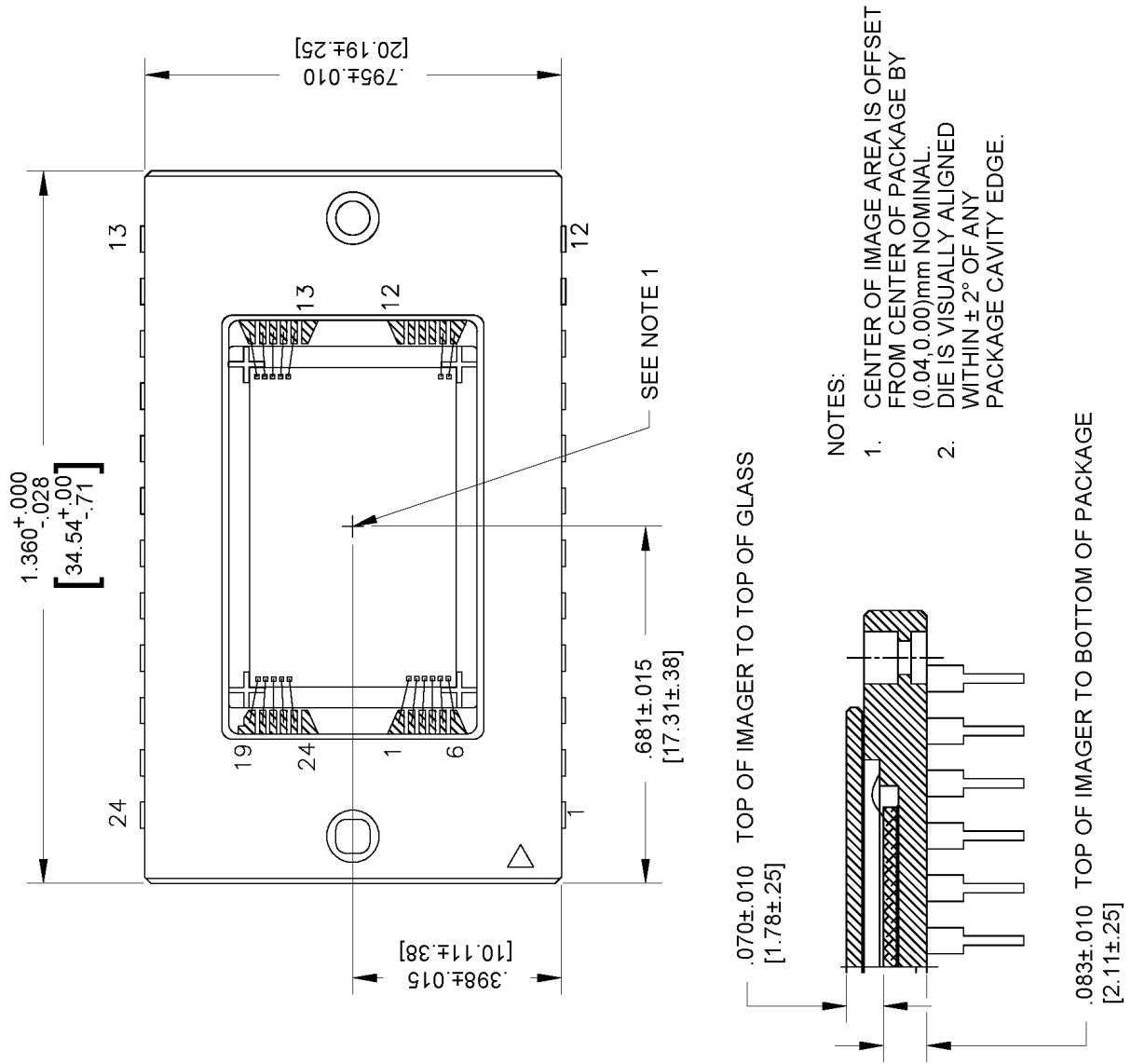


Figure 12. Completed Assembly (2 of 2)

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

**PUBLICATION ORDERING INFORMATION**

**LITERATURE FULFILLMENT:**  
Literature Distribution Center for ON Semiconductor  
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**N. American Technical Support:** 800-282-9855 Toll Free USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5817-1050

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)  
**Order Literature:** <http://www.onsemi.com/orderlit>  
For additional information, please contact your local Sales Representative