

N25Q512A83G1241E

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Orderable Part Information

Status	Production	Alternative Part	N/A
FBGA Code	N/A	SPD Data	N/A
MBQual Data	N/A	Shipping Media	N/A
PLP	No	Start Date	N/A

Specs

Density	512Mb	Width	x1/x2/x4
Voltage	2.7V-3.6V	Package	T-PBGA
Pin Count	24-ball	Speed	108 MHz
RoHS	Yes	Type	Multi I/O
Op Temp	-40C to +85C	Applications	Embedded
Part Family	N25Q	Media	Tray

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Date	What was added
10/2014	N25Q (16Mb, 32Mb, 64Mb, 128Mb, 256Mb, 512Mb, 1Gb) General Low-Level Driver v1.8
08/2014	IBIS_N25Q512A83G124 v1.4

FAQs

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Sim Models & Software

Title & Description	Secure	ID	Updated
Verilog model, N25Q, 512A13E, 3.0V, v1.3: 512Mb 3.0V Micron XIP Hold pin			07/2014
IBIS_N25Q512A83G124 v1.4: A= 65nm . 8= HOLD# + RESET#. 3= 2.7-3.6V. G= Uniform, easy transparent stack. 12= 6x8x1.2 BGA24/5x5. 4= -40C to +85C.		N25Q-QGJS	08/2014

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[+ My design was based on a specification stating the JTAG was relative to VDD \(1.8V\), but now we've discovered that JTAG is actually relative to VDDQ \(1.5V\). It's a fairly significant board spin to change this: what do I risk by leaving the design as-is? I assume that the specification is still for VDDQ + 0.3V = 1.8V, but with CMOS parts there's no way I can guarantee that it won't swing past that on transitions.](#)
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