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KAI-0340

640 (H) x 480 (V) Interline CCD Image Sensor

Description

The KAI−0340 image sensor is a 640 (H) × 480 (V) resolution, 1/3″ optical format, progressive scan interline CCD. This image sensor is offered in 2 versions: the KAI−0340−Dual supports 210 full resolution frame-per-second readout while the KAI−0340−Single supports 110 frame-per-second readout. Frame rates as high as 2,000 Hz (KAI−0340−Single) and 3,400 Hz (KAI−0340−Dual) can be achieved by combining the Fast Horizontal Line Dump with custom clocking modes. Designed for demanding imaging applications, the KAI−0340 provides electronic shuttering, peak QE (quantum efficiency) of 55%, extremely low noise and low dark current. These features give this sensor exceptional sensitivity and make it ideal for machine vision, scientific, surveillance, and other computer input applications.

Table 1. GENERAL SPECIFICATIONS

Parameter	Typical Value
Architecture	Interline CDD; Progressive Scan
Total Number of Pixels	696 (H) × 492 (V)
Number of Effective Pixels	648 (H) × 484 (V)
Number of Active Pixels	640 (H) × 480 (V)
Pixel Size	7.4 μm(H) × 7.4 μm (V)
Active Image Size	4.736 mm (H) × 3.552 mm (V), 5.920 mm (Diagonal), 1/3″ Optical Format
Aspect Ratio	4:3
Number of Outputs	1 or 2
Charge Capacity	40 MHz − 20,000 e^- 20 MHz − 40,000 e^-
Output Sensitivity	30 μV/e^-
Photometric Sensitivity KAI−0340−ABB KAI−0340−CBA (RGB) KAI−0340−FBA (RGB)	 3.61 V/lux−sec 0.66 (R), 1.51 (G), 1.14 (B) V/lux−sec 0.92 (R), 1.80 (G), 1.22 (B) V/lux−sec
Readout Noise	40 MHz − 16 e^- 20 MHz − 14 e^-
Dynamic Range	40 MHz − 62 dB 20 MHz − 69 dB
Dark Current Photodiode VCCD	 < 200 eps < 1,000 eps
Maximum Pixel Clock Speed	40 MHz
Maximum Frame Rate KAI−0340−Dual KAI−0340−Single	 210 fps 110 fps
Package Type	22-Pin CERDIP (0.050″ Pin Spacing)
Cover Glass	Clear/Quartz Glass

NOTE: All Parameters are specified at T = 40°C unless otherwise noted.

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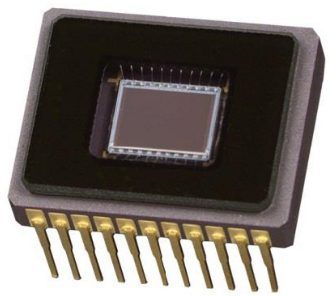


Figure 1. KAI−0340 Interline CCD Image Sensor

Features

- High Sensitivity
- High Dynamic Range
- Low Noise Architecture
- High Frame Rate
- Electronic Shutter

Applications

- Intelligent Transportation Systems
- Machine Vision
- Scientific

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

ORDERING INFORMATION

Table 2. ORDERING INFORMATION − KAI−0340 IMAGE SENSOR

Part Number	Description	Marking Code
KAI−0340−AAA−CP−AA−Single	Monochrome, No Microlens, CERDIP Package (Sidebrazed), Taped Clear Cover Glass, No Coatings, Standard Grade, Single Output	KAI−0340S
KAI−0340−AAA−CP−AE−Single	Monochrome, No Microlens, CERDIP Package (Sidebrazed), Taped Clear Cover Glass, No Coatings, Engineering Grade, Single Output	
KAI−0340−AAA−CP−AA−Dual	Monochrome, No Microlens, CERDIP Package (Sidebrazed), Taped Clear Cover Glass, No Coatings, Standard Grade, Dual Output	KAI−0340D
KAI−0340−AAA−CP−AE−Dual	Monochrome, No Microlens, CERDIP Package (Sidebrazed), Taped Clear Cover Glass, No Coatings, Engineering Grade, Dual Output	
KAI−0340−AAA−CF−AA−Single	Monochrome, No Microlens, CERDIP Package (Sidebrazed), Quartz Cover Glass, No Coatings, Standard Grade, Single Output	KAI−0340S
KAI−0340−AAA−CF−AE−Single	Monochrome, No Microlens, CERDIP Package (Sidebrazed), Quartz Cover Glass, No Coatings, Engineering Grade, Single Output	
KAI−0340−AAA−CF−AA−Dual	Monochrome, No Microlens, CERDIP Package (Sidebrazed), Quartz Cover Glass, No Coatings, Standard Grade, Dual Output	KAI−0340D
KAI−0340−AAA−CF−AE−Dual	Monochrome, No Microlens, CERDIP Package (Sidebrazed), Quartz Cover Glass, No Coatings, Engineering Grade, Dual Output	
KAI−0340−ABB−CP−AA−Single	Monochrome, Telecentric Microlens, CERDIP Package (Sidebrazed), Taped Clear Cover Glass, No Coatings, Standard Grade, Single Output	KAI−0340ABBS
KAI−0340−ABB−CP−AE−Single	Monochrome, Telecentric Microlens, CERDIP Package (Sidebrazed), Taped Clear Cover Glass, No Coatings, Engineering Grade, Single Output	
KAI−0340−ABB−CP−AA−Dual	Monochrome, Telecentric Microlens, CERDIP Package (Sidebrazed), Taped Clear Cover Glass, No Coatings, Standard Grade, Dual Output	KAI−0340ABBD
KAI−0340−ABB−CP−AE−Dual	Monochrome, Telecentric Microlens, CERDIP Package (Sidebrazed), Taped Clear Cover Glass, No Coatings, Engineering Grade, Dual Output	
KAI−0340−ABB−CB−AA−Single	Monochrome, Telecentric Microlens, CERDIP Package (Sidebrazed), Clear Cover Glass, No Coatings, Standard Grade, Single Output	KAI−0340ABBS
KAI−0340−ABB−CB−A2−Single	Monochrome, Telecentric Microlens, CERDIP Package (Sidebrazed), Clear Cover Glass, No Coatings, Grade 2, Single Output	
KAI−0340−ABB−CB−AE−Single	Monochrome, Telecentric Microlens, CERDIP Package (Sidebrazed), Clear Cover Glass, No Coatings, Engineering Grade, Single Output	
KAI−0340−ABB−CB−AA−Dual	Monochrome, Telecentric Microlens, CERDIP Package (Sidebrazed), Clear Cover Glass, No Coatings, Standard Grade, Dual Output	KAI−0340ABBD
KAI−0340−ABB−CB−AE−Dual	Monochrome, Telecentric Microlens, CERDIP Package (Sidebrazed), Clear Cover Glass, No Coatings, Engineering Grade, Dual Output	
KAI−0340−FBA−CB−AA−Single	Color Gen2 (Bayer RGB), Telecentric Microlens, CERDIP Package (Sidebrazed), Clear Cover Glass, No Coatings, Standard Grade, Single Output	KAI0340FBAS
KAI−0340−FBA−CB−AE−Single	Color Gen2 (Bayer RGB), Telecentric Microlens, CERDIP Package (Sidebrazed), Clear Cover Glass, No Coatings, Engineering Grade, Single Output	
KAI−0340−FBA−CB−AA−Dual	Color Gen2 (Bayer RGB), Telecentric Microlens, CERDIP Package (Sidebrazed), Clear Cover Glass, No Coatings, Standard Grade, Dual Output	KAI0340FBAD
KAI−0340−FBA−CB−AE−Dual	Color Gen2 (Bayer RGB), Telecentric Microlens, CERDIP Package (Sidebrazed), Clear Cover Glass, No Coatings, Engineering Grade, Dual Output	
KAI−0340−CBA−CB−AA−Single*	Color Gen1 (Bayer RGB), Telecentric Microlens, CERDIP Package (Sidebrazed), Clear Cover Glass, No Coatings, Standard Grade, Single Output	KAI−0340SCM
KAI−0340−CBA−CB−AE−Single*	Color Gen1 (Bayer RGB), Telecentric Microlens, CERDIP Package (Sidebrazed), Clear Cover Glass, No Coatings, Engineering Grade, Single Output	
KAI−0340−CBA−CB−AA−Dual*	Color Gen1 (Bayer RGB), Telecentric Microlens, CERDIP Package (Sidebrazed), Clear Cover Glass, No Coatings, Standard Grade, Dual Output	KAI−0340DCM
KAI−0340−CBA−CB−AE−Dual*	Color Gen1 (Bayer RGB), Telecentric Microlens, CERDIP Package (Sidebrazed), Clear Cover Glass, No Coatings, Engineering Grade, Dual Output	

*Not recommended for new designs.

Table 3. ORDERING INFORMATION − EVALUATION SUPPORT

Part Number	Description
KAI−0340−10−40−A−EVK	Evaluation Board (Complete Kit)

See the ON Semiconductor *Device Nomenclature* document (TND310/D) for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.onsemi.com.

DEVICE DESCRIPTION

Architecture

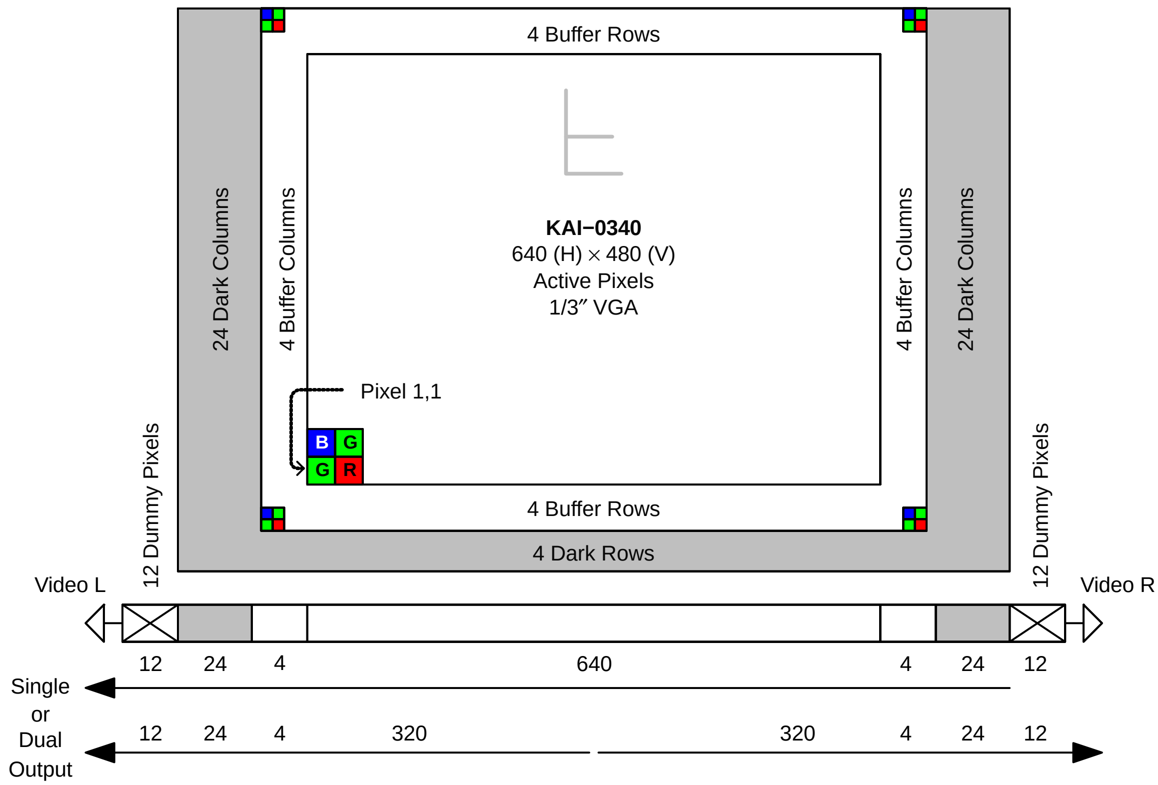


Figure 2. Sensor Architecture

There are 4 light-shielded rows followed by 488 photoactive rows. The first 4 and the last 4 photoactive rows are buffer rows giving a total of 480 lines of image data.

In the single output mode all pixels are clocked out of the Video L output in the lower left corner of the sensor. The first 12 empty pixels of each line do not receive charge from the vertical shift register. The next 24 pixels receive charge from the left light-shielded edge followed by 648 photosensitive pixels and finally 24 more light-shielded pixels from the right edge of the sensor. The first and last 4 photosensitive pixels are buffer pixels giving a total of 640 pixels of image data.

In the dual output mode the clocking of the right half of the horizontal CCD is reversed. The left half of the image is clocked out Video L and the right half of the image is clocked out Video R. Each row consists of 12 empty pixels followed by 24 light-shielded pixels followed by 324 photosensitive pixels. When reconstructing the image, data from Video R will have to be reversed in a line buffer and appended to the Video L data.

There are no dark reference rows at the top and 4 dark rows at the bottom of the image sensor. The 4 dark rows are not entirely dark and so should not be used for a dark reference level. Use the 24 dark columns on the left or right side of the image sensor as a dark reference.

Of the 24 dark columns, the first and last dark columns should not be used for determining the zero signal level. Some light does leak into the first and last dark columns. Only use the center 22 columns of the 24 column dark reference.

ESD Protection

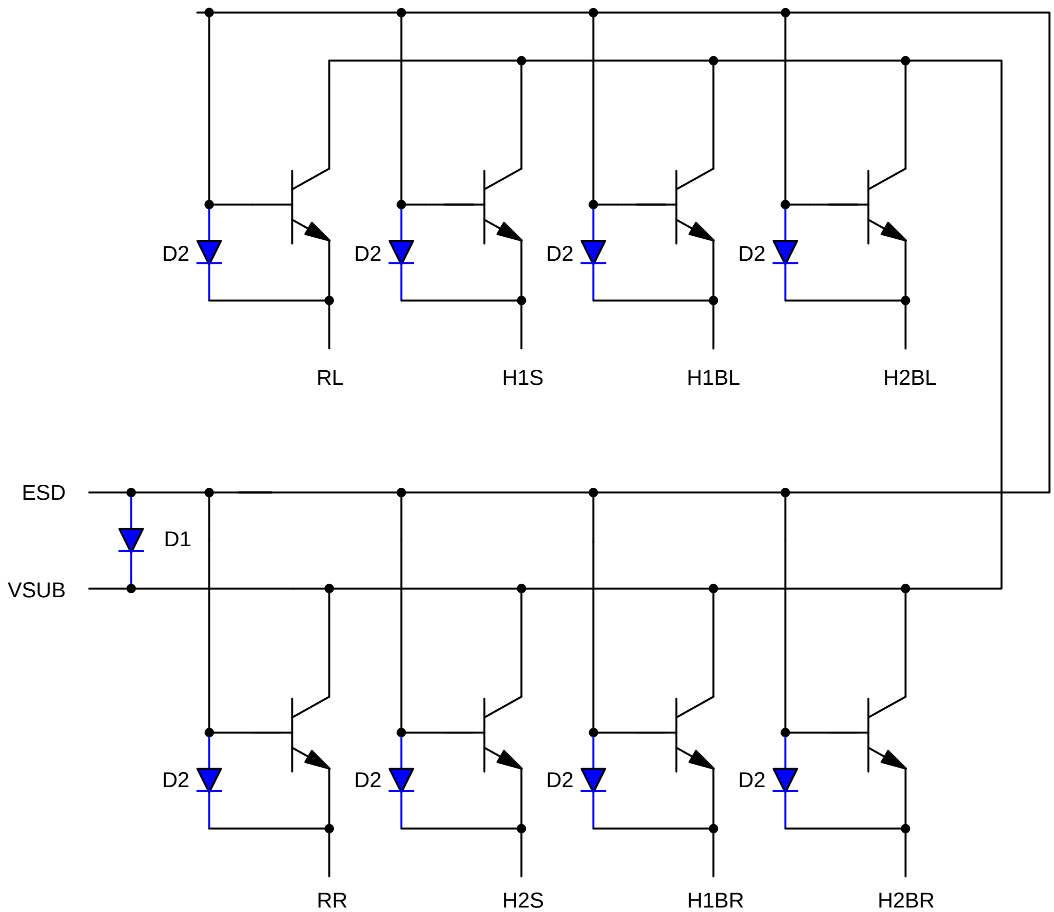


Figure 3. ESD Protection

The ESD protection on the KAI−0340 is implemented using bipolar transistors. The substrate (SUB) forms the common collector of all the ESD protection transistors. The ESD pin is the common base of all the ESD protection transistors. Each protected pin is connected to a separate emitter as shown in Figure 3.

The ESD circuit turns on if the base-emitter junction voltage exceeds 17 V. Care must be taken while operating the image sensor, especially during the power on sequence, to not forward bias the base-emitter or base-collector junctions. If it is possible for the camera power up sequence to forward bias these junctions then diodes D1 and D2 should be added to protect the image sensor. Put one diode D1 between the ESD and VSUB pins. Put one diode D2 on each pin that may forward bias the base-emitter junction. The diodes will prevent large currents from flowing through the image sensor. Note that external diodes D1 and D2 are optional and are only needed if it is possible to forward bias any of the junctions.

Note that diodes D1 and D2 are added external to the KAI−0340.

Pin Description and Device Orientation

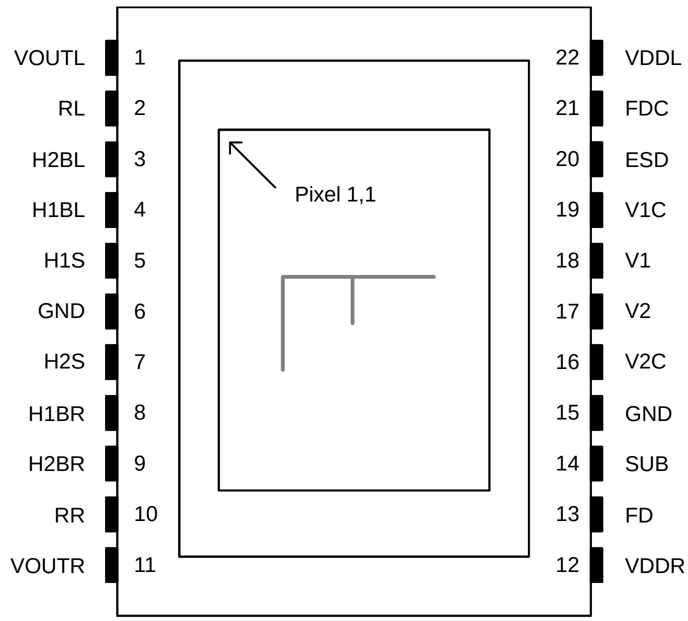


Figure 4. Pin Description (Top View)

Table 4. PIN DESCRIPTION

Pin No.	Symbol	Description
1	VOUTL	Video Output, Left
2	RL	Reset Gate, Left
3	H2BL	Horizontal Clock, Phase 2, Barrier, Left
4	H1BL	Horizontal Clock, Phase 1, Barrier, Right
5	H1S	Horizontal Clock, Phase 1, Storage
6	GND	Ground
7	H2S	Horizontal Clock, Phase 2, Storage
8	H1BR	Horizontal Clock, Phase 1, Barrier, Right
9	H2BR	Horizontal Clock, Phase 2, Barrier, Right
10	RR	Reset Gate, Right
11	VOUTR	Video Output, Right
12	VDDR	V_{DD}, Right
13	FD	Fast Line Dump Gate, Left and Right Columns
14	SUB	Substrate
15	GND	Ground
16	V2C	Vertical Clock, Phase 2, Center Rows
17	V2	Vertical Clock, Phase 2, Top and Bottom Rows
18	V1	Vertical Clock, Phase 1, Top and Bottom Rows
19	V1C	Vertical Clock, Phase 1, Center Rows
20	ESD	ESD
21	FDC	Fast Line Dump Gate, Center Columns
22	VDDL	V_{DD}, Left

1. The pins are on a 0.050″ spacing
2. If the vertical windowing option is not to be used, then the V1 and V1C pins should be driven from one clock driver. The V2 and V2C pins should also be driven from one clock driver.
3. If the fast dump windowing option is not to be used, then the FD and FDC pins should be driven from the same clock driver.
4. The VOUTR pin is not enabled in the KAI−0340−Single version.

IMAGING PERFORMANCE

Table 5. IMAGING PERFORMANCE OPERATIONAL CONDITIONS

(Unless otherwise noted, Imaging Performance Specifications are measured using the following conditions.)

Description	Condition
Frame Time (Note 5)	53 ms
Horizontal Clock Frequency	10 MHz
Light Source (Notes 6, 7)	Continuous Red, Green and Blue Illumination Centered at 450, 530 and 650 nm
Operation	Nominal Operating Voltages and Timing

5. Electronic shutter is not used. Integration time equals frame time.
6. LEDs used: Blue: Nichia NLPB500, Green: Nichia NSPG500S and Red: HP HLMP−8115.
7. For monochrome sensor, only green LED used.

Table 6. IMAGING PERFORMANCE SPECIFICATIONS

Description	Symbol	Min.	Nom.	Max.	Unit	Sampling Plan	Temperature Tested at (°C)
ALL CONFIGURATIONS							
Photodiode CCD Dark Current	I_{PD}	0	40	200	e/p/s	Die	27, 40
Vertical CCD Dark Current	I_{VD}	0	400	1,000	e/p/s	Die	27, 40
Dark Current Doubling Temperature		N/A	7	N/A	°C	Design	
Horizontal CCD Charge Capacity	H_{Ne}	80	N/A	N/A	ke−	Design	
Vertical CCD Charge Capacity	V_{Ne}	50	N/A	N/A	ke−	Design	
Horizontal CCD Charge Transfer Efficiency	HCTE	0.99999	N/A	N/A		Design	
Vertical CCD Charge Transfer Efficiency	VCTE	0.99999	N/A	N/A		Design	
Image Lag	Lag	0	< 10	50	e−	Design	
Anti-Blooming Factor	X_{AB}	100	300	N/A		Design	
Vertical Smear	Smr	N/A	80	75	dB	Design	
Output Amplifier DC Offset (Note 8)	V_{ODC}	6	N/A	12	V	Die	
Output Amplifier Impedance (Note 9)	R_{OUT}	100	150	200	Ω	Die	
Output Amplifier Bandwidth	f_{-3dB}	N/A	140	N/A	MHz	Design	
Output Amplifier Sensitivity	ΔV/ΔN	N/A	30	N/A	μV/e	Design	
MONOCHROME CONFIGURATIONS							
Global Uniformity		0.0	1.5	3.0	% rms	Die	27, 40
Global Peak to Peak Uniformity	PRNU	0.0	5.0	10.0	% pp	Die	27, 40
Center Uniformity		0.0	0.6	1.0	% rms	Die	27, 40
Photometric Sensitivity KAI−0340M (Note 11)		N/A	3.61	N/A	V/lux-sec	Design	
COLOR CONFIGURATIONS							
Global Uniformity (Note 10)		0.0	2.0	5.0	% rms	Die	27, 40
Global Peak to Peak Uniformity (Note 10)	PRNU	0.0	5.0	10.0	% pp	Die	27, 40
Center Uniformity (Note 10)		0.0	1.0	2.0	% rms	Die	27, 40
Photometric Sensitivity Gen2 Blue (B) Pixels (Note 11)		N/A	1.22	N/A	V/lux-sec	Design	
Photometric Sensitivity Gen2 Green (G) Pixels (Note 11)		N/A	1.80	N/A	V/lux-sec	Design	

Table 6. IMAGING PERFORMANCE SPECIFICATIONS (continued)

Description	Symbol	Min.	Nom.	Max.	Unit	Sampling Plan	Temperature Tested at (°C)
COLOR CONFIGURATIONS							
Photometric Sensitivity Gen2 Red (R) Pixels (Note 11)		N/A	0.92	N/A	V/lux-sec	Design	
Photometric Sensitivity Gen1 Blue (B) Pixels (Notes 11, 12)		N/A	1.14	N/A	V/lux-sec	Design	
Photometric Sensitivity Gen1 Green (G) Pixels (Notes 11, 12)		N/A	1.51	N/A	V/lux-sec	Design	
Photometric Sensitivity Gen1 Red (R) Pixels (Notes 11, 12)		N/A	0.66	N/A	V/lux-sec	Design	

8. Measured at sensor output with constant current load of I_{OUT} = −5 mA and during the floating diffusion reset interval (R high).
9. Last stage only. C_{LOAD} = 10 pF. Then f_{-3dB} = (1 / (2n · R_{OUT} · C_{LOAD})).
10. Per color.
11. Calculated using quantum efficiency, output amplifier sensitivity, 3200K Plankian source and a CM500S IR-cut filter.
12. This color filter set configuration (Gen1) is not recommended for new designs.

TYPICAL PERFORMANCE CURVES

Quantum Efficiency

Monochrome with Microlens

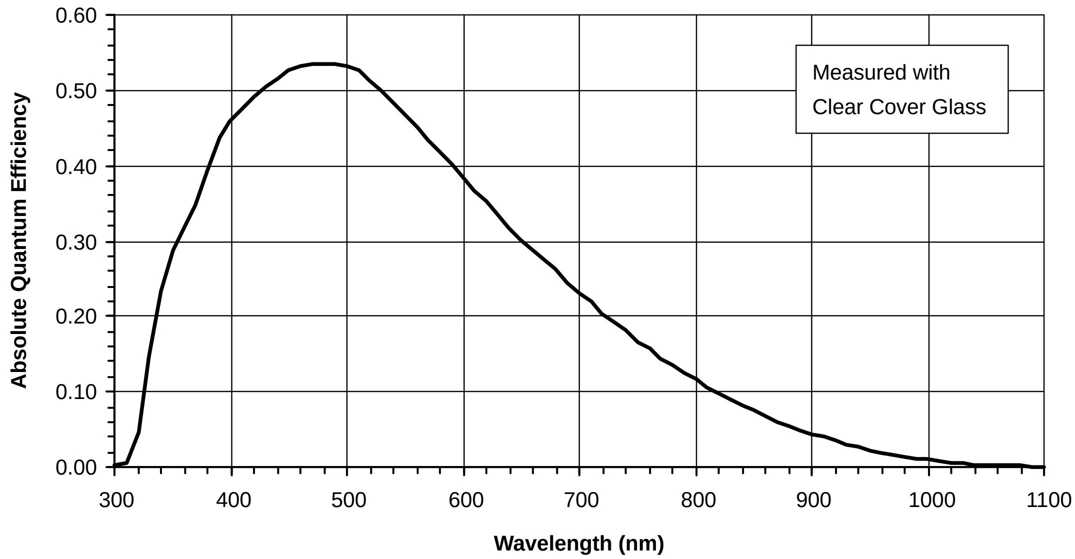


Figure 5. Monochrome with Microlens Quantum Efficiency

Monochrome without Microlens

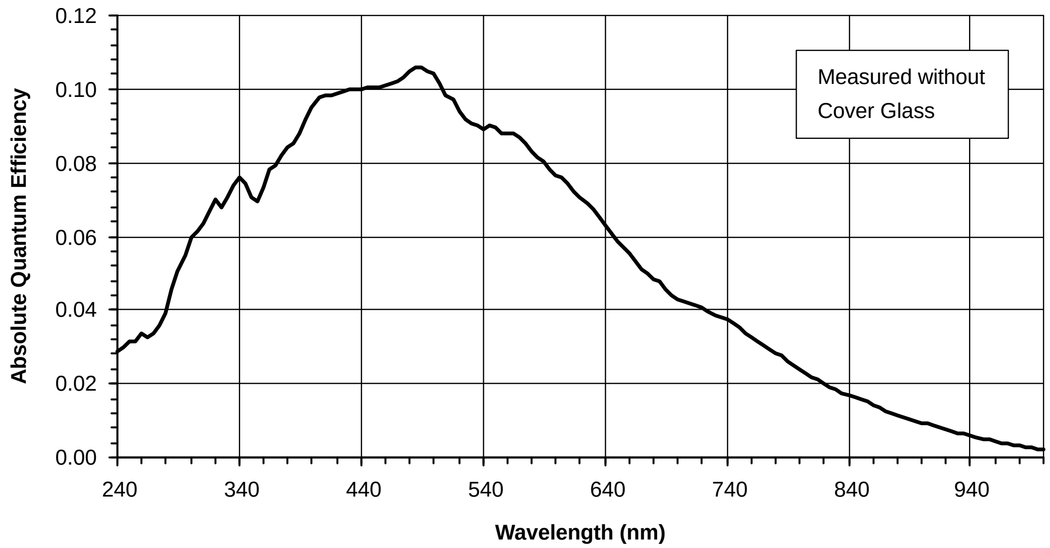


Figure 6. Monochrome without Microlens Quantum Efficiency

Color (Bayer RGB) with Microlens

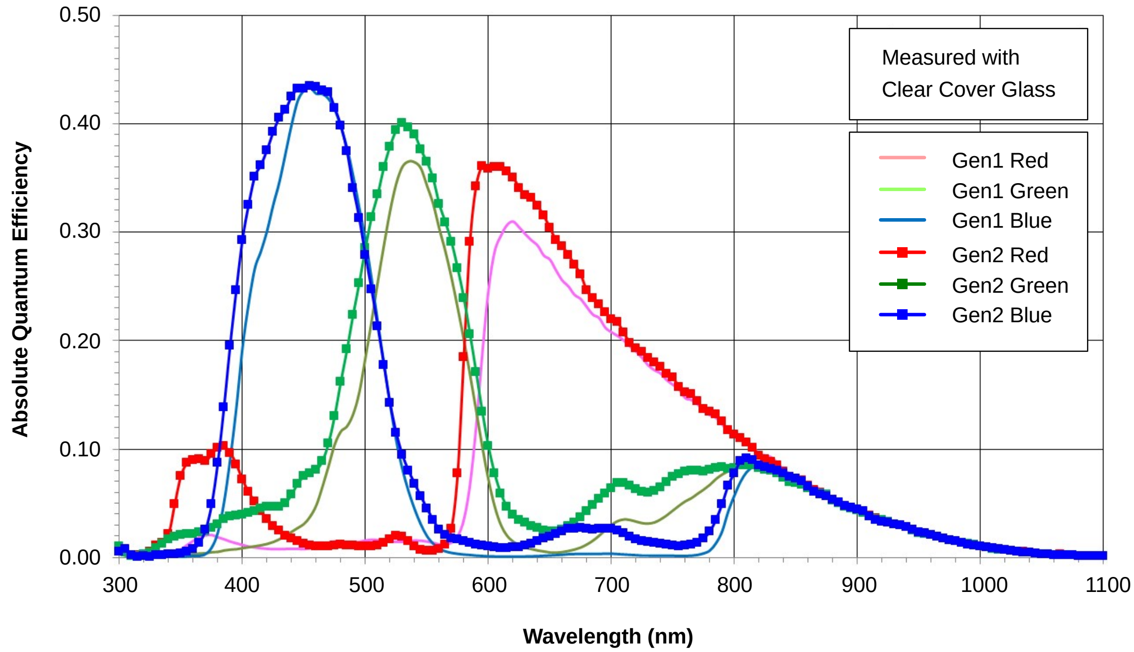


Figure 7. Color (Bayer RGB) with Microlens Quantum Efficiency

Angular Quantum Efficiency

Monochrome with Microlens

For the curves marked "Horizontal", the incident light angle is varied in a plane parallel to the HCCD.
For the curves marked "Vertical", the incident light angle is varied in a plane parallel to the VCCD.

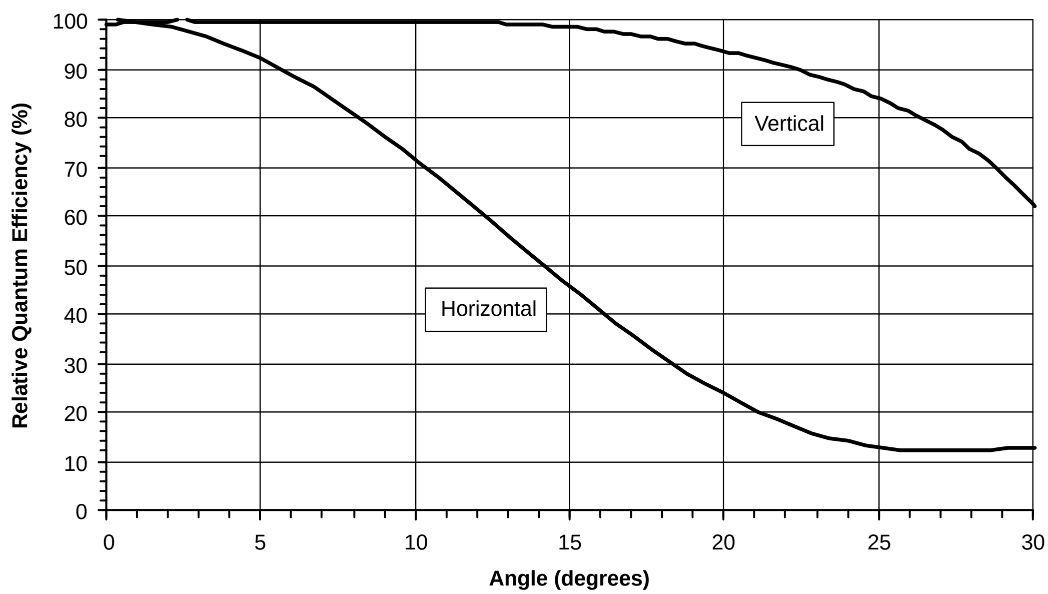


Figure 8. Angular Quantum Efficiency

Power Estimated

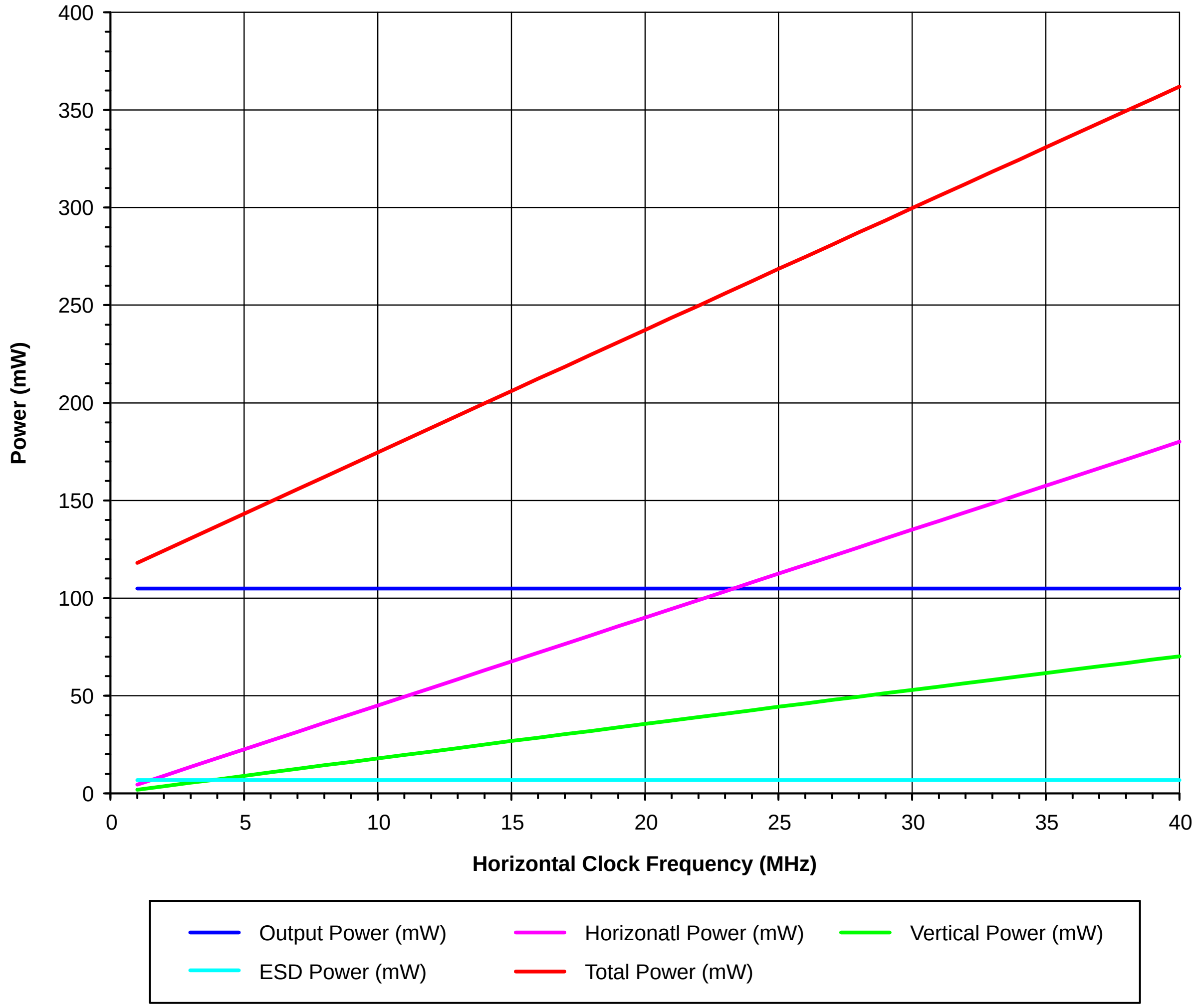


Figure 9. Power

Frame Rates

Frames rates are for continuous mode operation.

Table 7. FRAME RATES

Description	KAI−0340−Single and KAI−0340−Dual Single Output (fps)	KAI−0340−Dual Only Dual Output (fps)
640 × 480	112	214
228 × 480	306	581
640 × 164	325	618
228 × 164	877	1,637
228 × 55	2,000	3,400

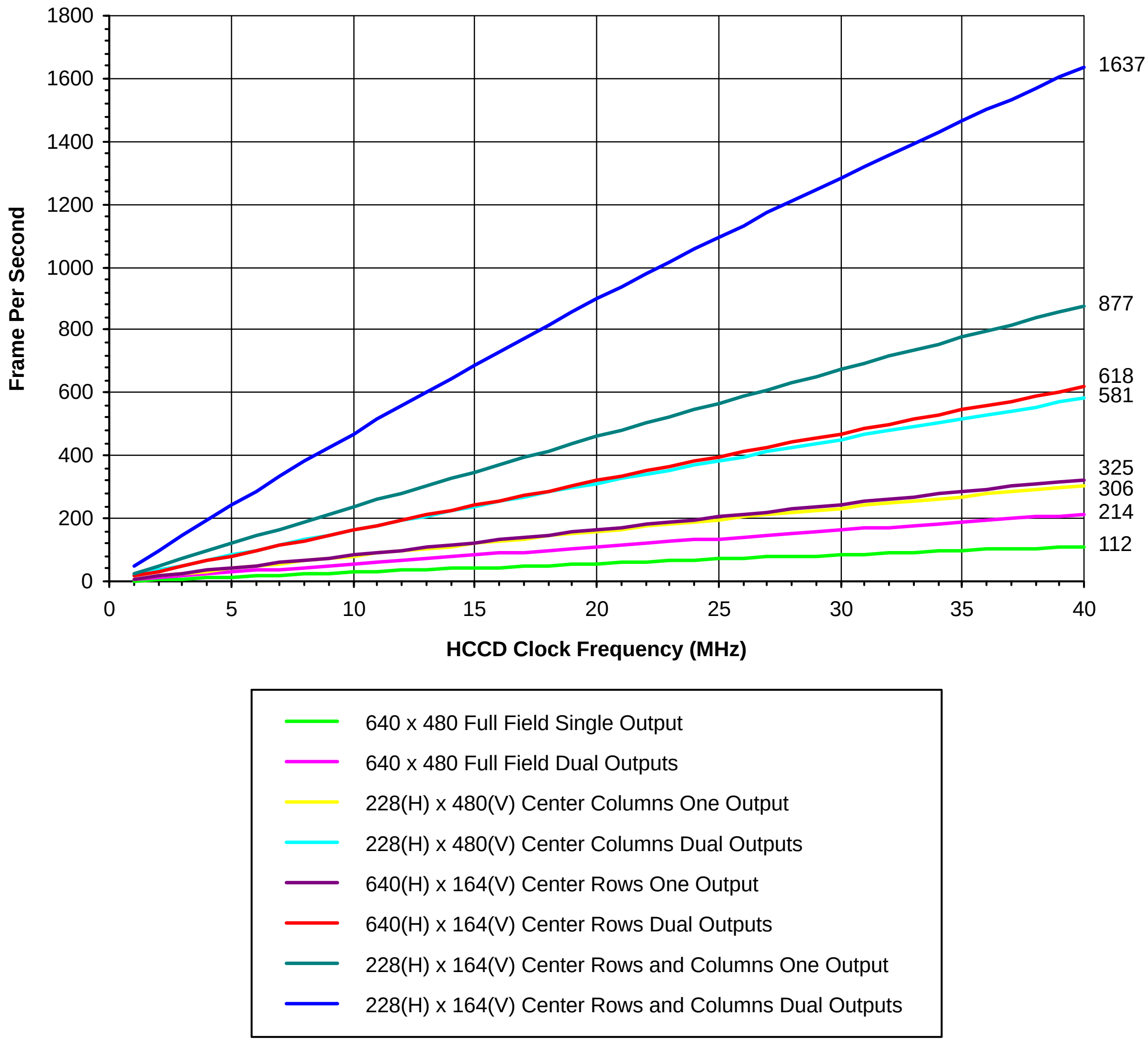


Figure 10. Frame Rates

DEFECT DEFINITIONS

Table 8. DEFECT DEFINITIONS

Description	Definition	Maximum	Temperature(s) Tested at (°C)
MONOCHROME (EXCLUDING KAI−0340−ABB−CB−A2−SINGLE)			
Major Dark Field Defective Pixel	Defect ≥ 16 mV	2	27, 40
Major Bright Field Defective Pixel	Defect ≥ 11%	0	27, 40
Minor Dark Field Defective Pixel	Defect ≥ 4 mV	100	27, 40
Dead Pixel	Defect ≥ 80%	0	27, 40
Saturated Pixel	Defect ≥ 30 mV	0	27, 40
Cluster Defect	A Group of 2 to 10 Contiguous Major Defective Pixels	0	27, 40
Column Defect	A Group of more than 10 Contiguous Major Defective Pixels along a Single Column	0	27, 40
MONOCHROME (KAI−0340−ABB−CB−A2−SINGLE ONLY)			
Major Dark Field Defective Pixel	Defect ≥ 16 mV	2	27, 40
Major Bright Field Defective Pixel	Defect ≥ 11%	10	27, 40
Minor Dark Field Defective Pixel	Defect ≥ 4 mV	100	27, 40
Dead Pixel	Defect ≥ 80%	0	27, 40
Saturated Pixel	Defect ≥ 30 mV	0	27, 40
Cluster Defect	A Group of 2 to 10 Contiguous Major Defective Pixels	0	27, 40
Column Defect	A Group of more than 10 Contiguous Major Defective Pixels along a Single Column	0	27, 40
COLOR VERSIONS			
Major Dark Field Defective Pixel	Defect ≥ 16 mV	2	27, 40
Major Bright Field Defective Pixel	Defect ≥ 11%	2	27, 40
Minor Dark Field Defective Pixel	Defect ≥ 4 mV	100	27, 40
Dead Pixel	Defect ≥ 80%	0	27, 40
Saturated Pixel	Defect ≥ 30 mV	0	27, 40
Cluster Defect	A Group of 2 to 10 Contiguous Major Defective Pixels	0	27, 40
Column Defect	A Group of more than 10 Contiguous Major Defective Pixels along a Single Column	0	27, 40

Defect Map

No defect maps are available for the KAI−0340 image sensor.

TEST DEFINITIONS

Test Regions of Interest

Active Area ROI:	Pixel (1, 1) to Pixel (640, 480)
Center 100 by 100 ROI:	Pixel (270, 190) to Pixel (369, 289)

Only the active pixels are used for performance and defect tests.

Test Sub-Regions of Interest

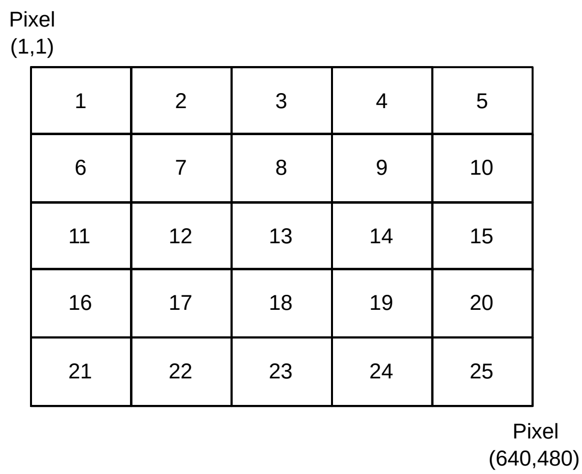


Figure 11. Test Sub-Regions of Interest

Over-Clocking

The test system timing is configured such that the sensor is overclocked in both the vertical and horizontal directions. See Figure 12 for a pictorial representation of the regions.

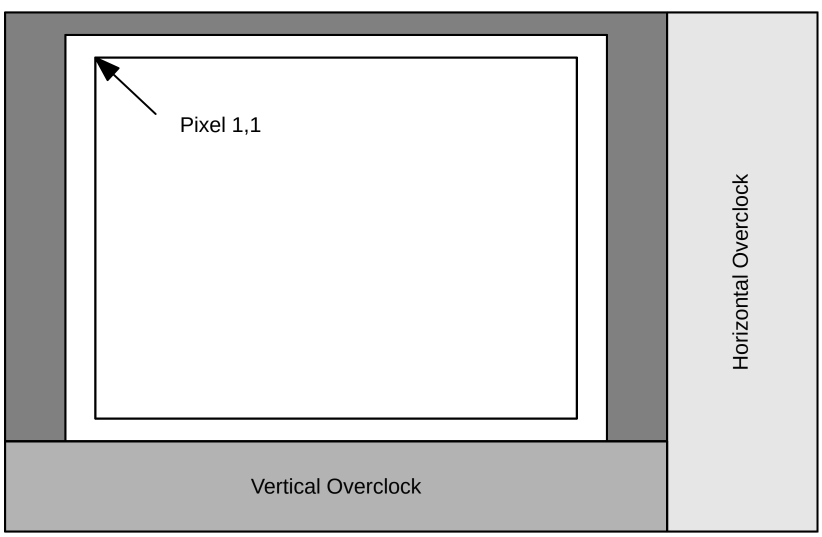


Figure 12. Overclock Regions of Interest

Tests

Global Non-Uniformity

This test is performed with the imager illuminated to a level such that the output is at 70% of saturation (approximately 420 mV). Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 600 mV. Global non-uniformity is defined as

$$\text{Global Non−Uniformity} = 100 \cdot \left(\frac{\text{Active Area Standard Deviation}}{\text{Active Area Signal}}\right)$$

Units : % rms

Active Area Signal = Active Area Average − H. Overclock Average

Global Peak-to-Peak Non-Uniformity

This test is performed with the imager illuminated to a level such that the output is at 70% of saturation (approximately 420 mV). Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 600 mV. The sensor is partitioned into 25 sub-regions of interest, each of which is 128 by 96 pixels in size. The average signal level of each of the 25 sub-regions of interest (ROI) is calculated. The signal level of each of the sub regions of interest is calculated using the following formula:

$$A[i] = (\text{ROI Average} - \text{Horizontal Overclock Average})$$

Where i = 1 to 25. During this calculation on the 25 sub-regions of interest, the maximum and minimum average signal levels are found. The global peak-to-peak non-uniformity is then calculated as:

$$\text{Global Non−Uniformity} = 100 \cdot \left(\frac{\text{A[i] Max. Signal} - \text{A[i] Min. Signal}}{\text{Active Area Signal}}\right)$$

Units : % pp

Active Area Signal = Active Area Average − H. Overclock Average

Center Non-Uniformity

This test is performed with the imager illuminated to a level such that the output is at 70% of saturation (approximately 420 mV). Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 600 mV. Defects are excluded for the calculation of this test. This test is performed on the center 100 by 100 pixels (See Test Regions of Interest) of the sensor. Center non-uniformity is defined as:

$$\text{Center ROI Non−Uniformity} = 100 \cdot \left(\frac{\text{Center ROI Standard Deviation}}{\text{Center ROI Signal}}\right)$$

Units : % rms

Center ROI Signal = Center ROI Average − H. Overclock Average

Dark Field Defect Test

This test is performed under dark field conditions. The sensor is partitioned into 25 sub-regions of interest, each of which is 128 by 96 pixels in size. In each region of interest, the median value of all pixels is found. For each region of interest, a pixel is marked defective if it is greater than or equal to the median value of that region of interest plus the defect threshold specified in “Defect Definitions” section.

Bright Field Defect Test

This test is performed with the imager illuminated to a level such that the output is at 70% of saturation (approximately 420 mV). Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 600 mV. The average signal level of all active pixels is found. The bright and dark thresholds are set as:

$$\text{Dark Defect Threshold} = \text{Active Area Signal} \cdot \text{Threshold}$$

$$\text{Bright Defect Threshold} = \text{Active Area Signal} \cdot \text{Threshold}$$

The sensor is then partitioned into 25 sub-regions of interest, each of which is 128 by 96 pixels in size. In each region of interest, the average value of all pixels is found. For each region of interest, a pixel is marked defective if it is greater than or equal to the median value of that region of interest plus the bright threshold specified or if it is less than or equal to the median value of that region of interest minus the dark threshold specified.

Example for major bright field defective pixels:

- Average value of all active pixels is found to be 420 mV.
- Dark defect threshold: 420 mV · 11% = 46 mV
- Bright defect threshold: 420 mV · 11% = 46 mV
- Region of interest #1 selected. This region of interest is pixels 1,1 to pixels 128,96.
  - Median of this region of interest is found to be 420 mV.
  - Any pixel in this region of interest that is ≥ (420 + 46 mV) 466 mV in intensity will be marked defective.
  - Any pixel in this region of interest that is ≤ (420 − 46 mV) 374 mV in intensity will be marked defective.
- All remaining 24 sub-regions of interest are analyzed for defective pixels in the same manner.

For the color sensor, the threshold for each color channel is determined independently.

OPERATION

Absolute maximum rating is defined as a level or condition that should not be exceeded at any time per the description. If the level or the condition is exceeded, the device will be degraded and may be damaged.

Table 9. ABSOLUTE MAXIMUM RATINGS

Description	Symbol	Min.	Max.	Unit
Operating Temperature (Note 13)	T	−50	70	°C
Humidity (Note 14)	RH	5	90	%
Output Bias Current (Note 15)	I_{OUT}	0.0	10	mA
Off−chip Load (Note 16)	C_L	N/A	10	pF

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

13. Noise performance will degrade at higher temperatures.
14. T = 25°C. Excessive humidity will degrade MTTF.
15. Each output. See Figure 13. Note that the current bias affects the amplifier bandwidth.
16. With total output load capacitance of C_L = 10 pF between the outputs and AC ground.

Table 10. ABSOLUTE VOLTAGE RATINGS BETWEEN PINS

Description	Min.	Max.	Unit
RL, RR, H1S, H2S, H1BL, H2BL, H1BR, H2BR to ESD	0	17	V
Pin to Pin with ESD Protection (Note 17)	−17	17	V
VDDL, VDDR to GND	0	25	V

17. Pins with ESD protection are: RL, RR, H1S, H2S, H1BL, H2BL, H1BR, and H2BR.

Table 11. DC OPERATING CONDITIONS

Description	Symbol	Min.	Nom.	Max.	Unit	Maximum DC Current
Output Amplifier Supply (Notes 18, 21)	V_{DD}	14.75	15.0	15.25	V	2.5 mA
Ground	GND	0.0	0.0	0.0	V	
Substrate (Notes 19, 23)	SUB	8.0	V_{AB}	15.0	V	
ESD Protection (Note 20)	ESD	−9.25	−9.0	−8.75	V	2.0 mA
Output Bias Current (Note 22)	I_{OUT}	0.0	5.0	10.0	mA	

18. The maximum DC current is for one output unloaded and is shown as I_{RD} + I_{SS} in Figure 13. This is the maximum current that the first two stages of one output amplifier plus the reset drain bias circuit will draw. This value is with V_{OUT} disconnected.
19. The operating value of the substrate voltage, V_{AB}, will be marked on the shipping container for each device. The shipping container will be marked with two V_{AB} voltages. One V_{AB} will be for a 600 mV charge capacity and the other V_{AB} will be for a 1,200 mV charge capacity. The 600 mV charge capacity is for operation of the horizontal clock at frequencies greater than 20 MHz. The 1,200 mV charge capacity V_{AB} value may be used for horizontal clock frequencies at or below 20 MHz.
20. VESD must be more negative than H1L, H2L and RL during sensors operation AND during camera power turn on.
21. **Both VDDL and VDDR must both be supplied.**
22. One output.
23. Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions*.

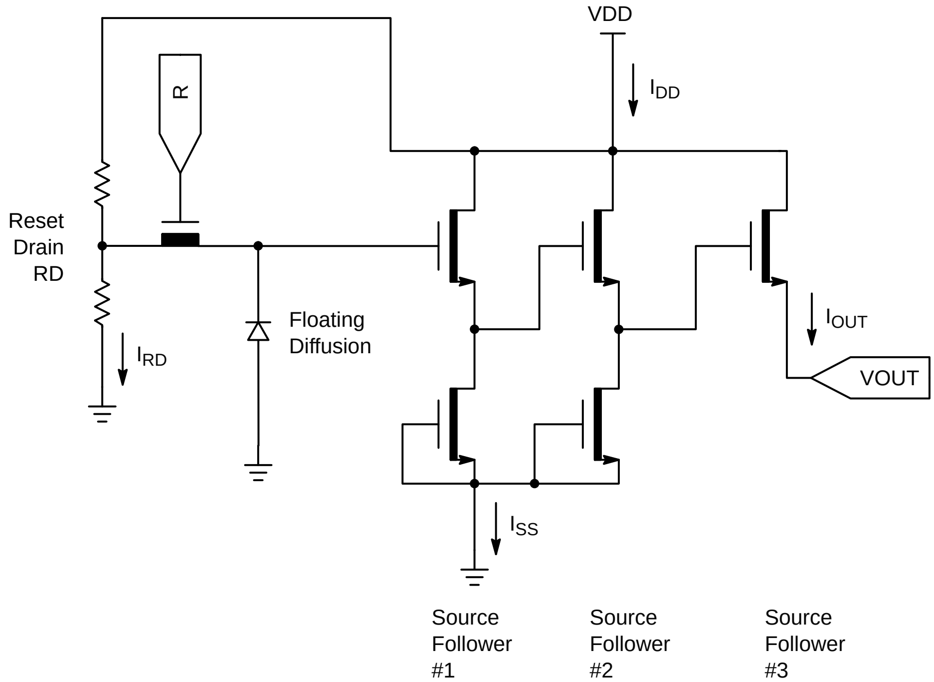


Figure 13. Output Amplifier

AC Operating Conditions

Table 12. CLOCK LEVELS

Description	Symbol	Min.	Nom.	Max.	Unit
Vertical CCD Clock High	V2H	9.5	10.0	10.5	V
Vertical CCD Clocks Midlevel	V1M, V2M	−0.2	0.0	0.2	V
Vertical CCD Clocks Low	V1L, V2L	−9.5	−9.0	−8.5	V
Horizontal CCD Clocks High (Note 24)	H1H, H2H	−0.5	0.0	0.5	V
Horizontal CCD Clocks Low (Note 24)	H1L, H2L	−5.5	−5.0	−4.5	V
Reset Clock High (Note 25)	RH	1.5	2.0	2.5	V
Reset Clock Low (Note 25)	RL	−3.5	−3.0	−2.5	V
Electronic Shutter Voltage (Note 26)	VES	44	48	52	V
Fast Dump High	FDH	4.0	5.0	5.5	V
Fast Dump Low	FDL	−9.5	−9.0	−8.5	V

24. The amplitude of the horizontal clock must be at least 4.5 V.
25. The amplitude of the reset clock must be at least 4.5 V.
26. Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions*.

The Figure 14 shows the DC bias (SUB) and AC clock (VES) applied to the SUB pin. Both the DC bias and AC clock are referenced to ground.

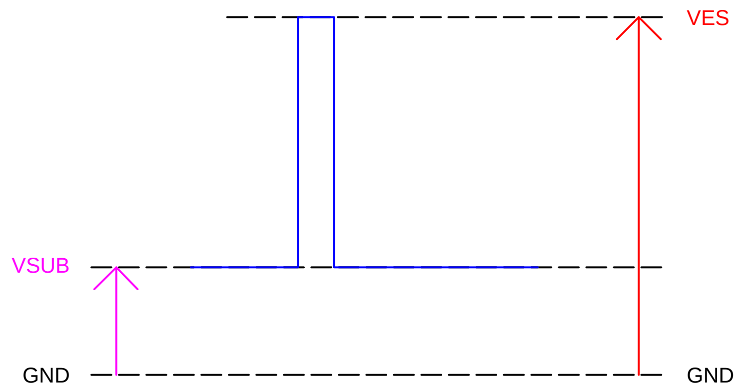


Figure 14. DC Bias and AC Clock Applied to the SUB Pin

Table 13. CLOCK LINE CAPACITANCE

Pin	Approximate Capacitance	Unit
V1C	3	nF
V1	5	nF
V2	5	nF
V2C	2	nF
H2BL	25	pF
H1BL	25	pF
H1S	40	pF
H2S	40	pF
H1BR	25	pF
H2BR	25	pF
RL	20	pF
RR	20	pF
FDC	25	pF
FD	30	pF

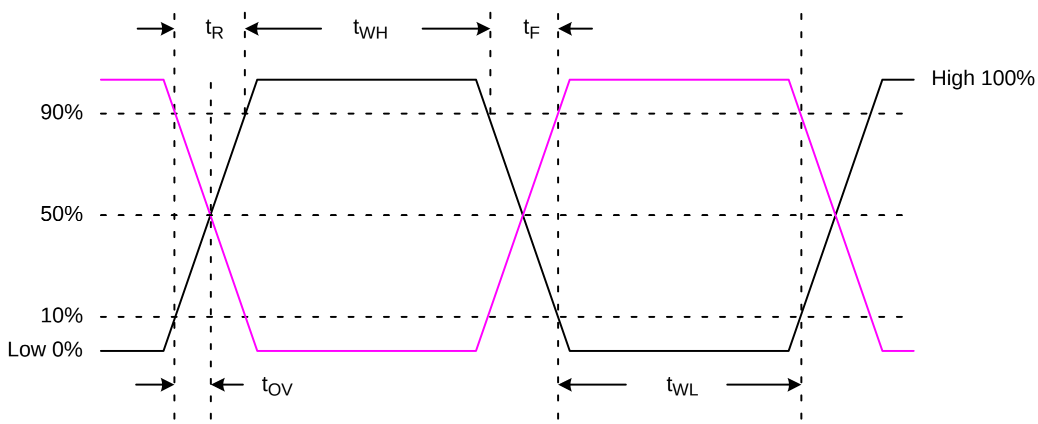
TIMING

Timing Requirements

Table 14. TIMING REQUIREMENTS

Description	Symbol	Min.	Unit
HCCD Delay	t_{HD}	200	ns
VCCD Transfer Time	t_{VCCD}	200	ns
Photodiode Transfer Time	t_{V3rd}	300	ns
VCCD Pedestal Time	t_{3P}	15	μs
VCCD Delay	t_{3D}	5	μs
VCCD Frame Delay	t_{3L}	15	μs
VCCD Line End Delay	t_{EL}	25	ns
HCCD Clock Period (Note 27)	t_H	25	ns
Reset Pulse Time	t_R	2.5	ns
Shutter Pulse Time	t_S	1.0	μs
Shutter Pulse Delay	t_{SD}	1.0	μs
Fast Line Dump Delay	t_{FD}	75	ns
VCCD Clock Overlap	t_{OV}	50	%

27. For operation at the minimum HCCD clock period (40 MHz), the substrate voltage must be set to limit the signal at the output to 600 mV.
28. Each clock pulse width is defined for t_{WH} or t_{WL}.



Timing Sequences

Timing Sequence A: Photodiode to VCCD Transfer, Entire Image

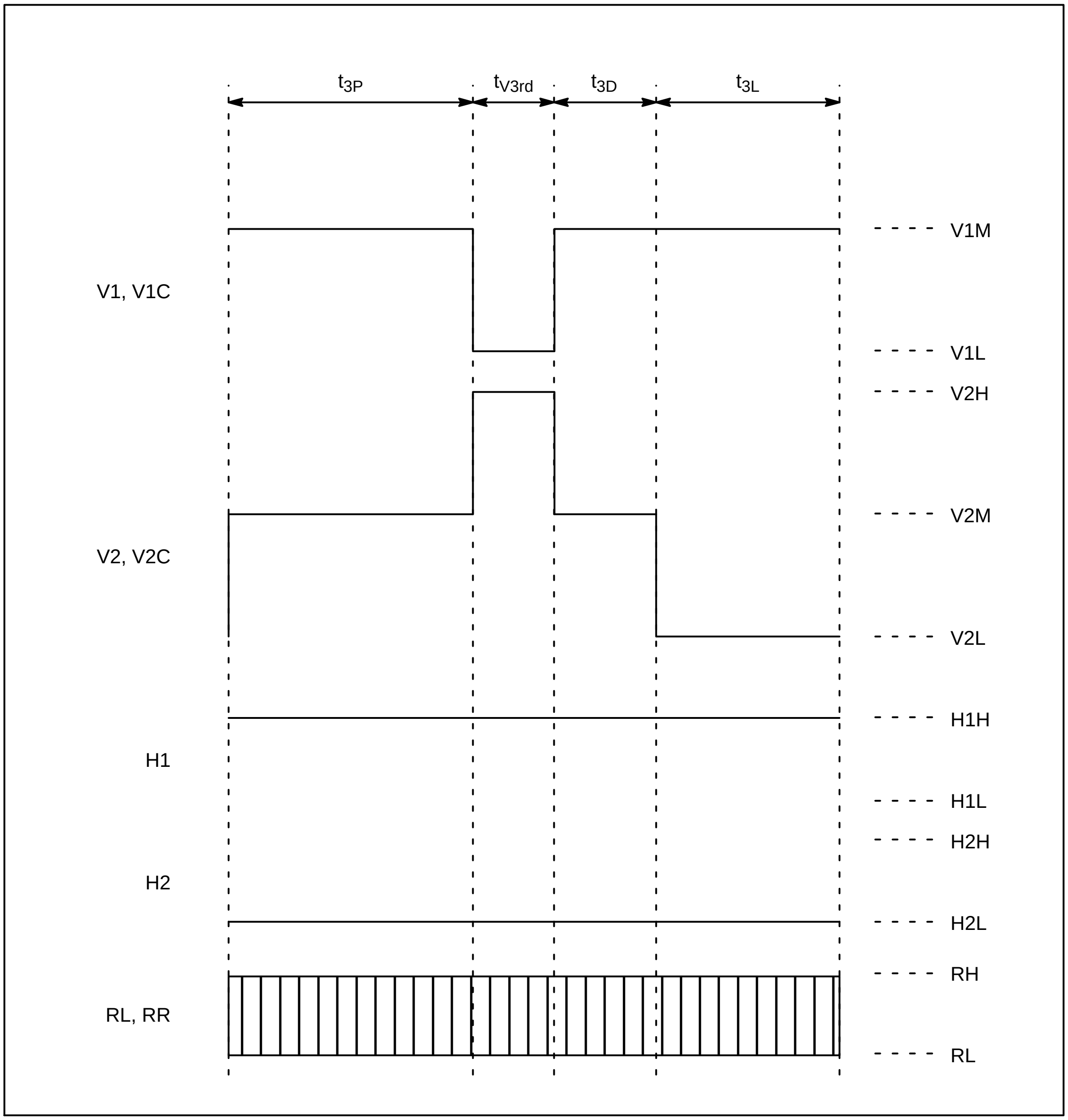


Figure 15. Timing Sequence A

Timing Sequence B: Vertical CCD Line Shift and Horizontal CCD Readout of One Line

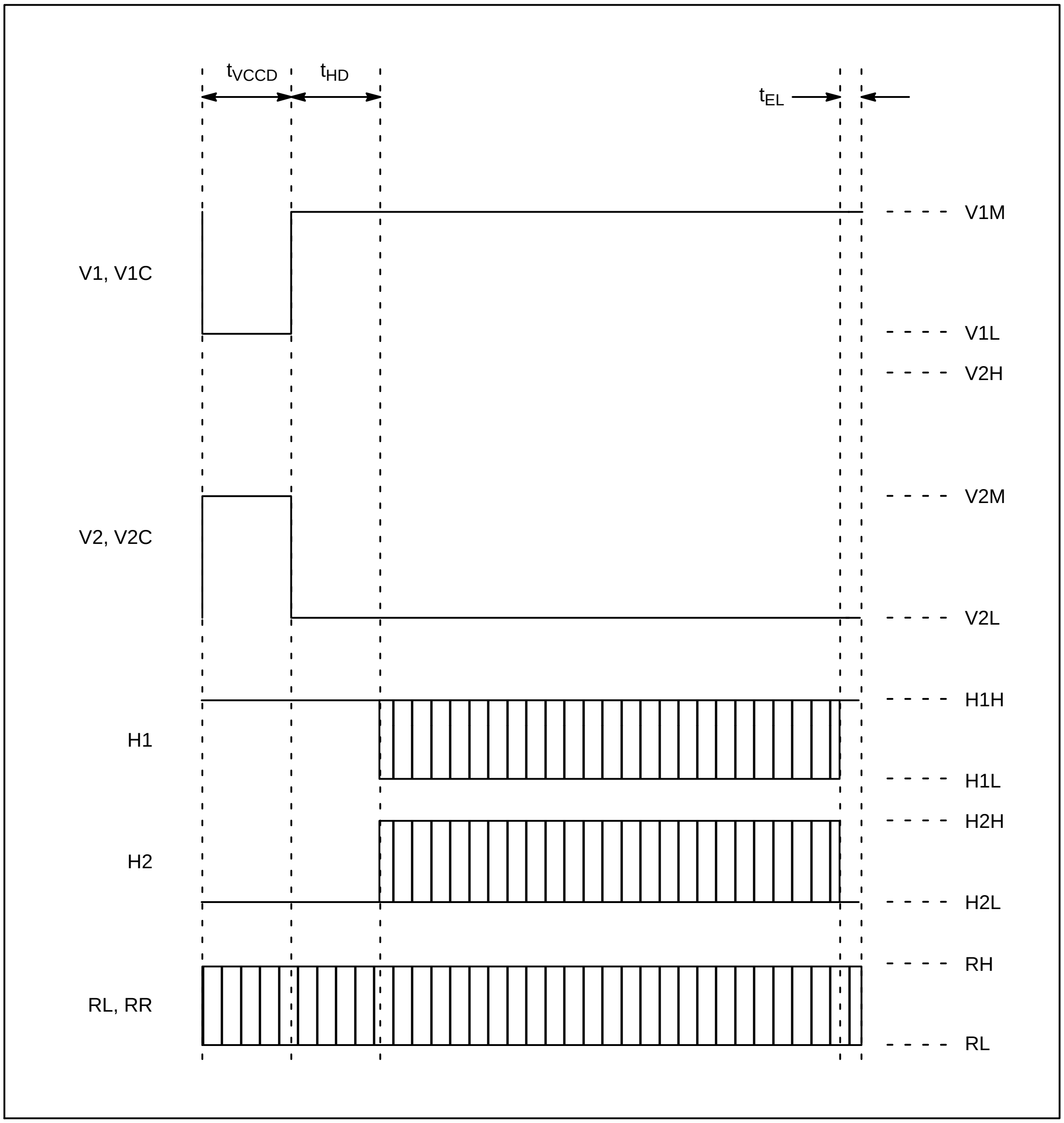


Figure 16. Timing Sequence B

Timing Sequence C: Photodiode to VCCD Transfer, Center 164 Rows

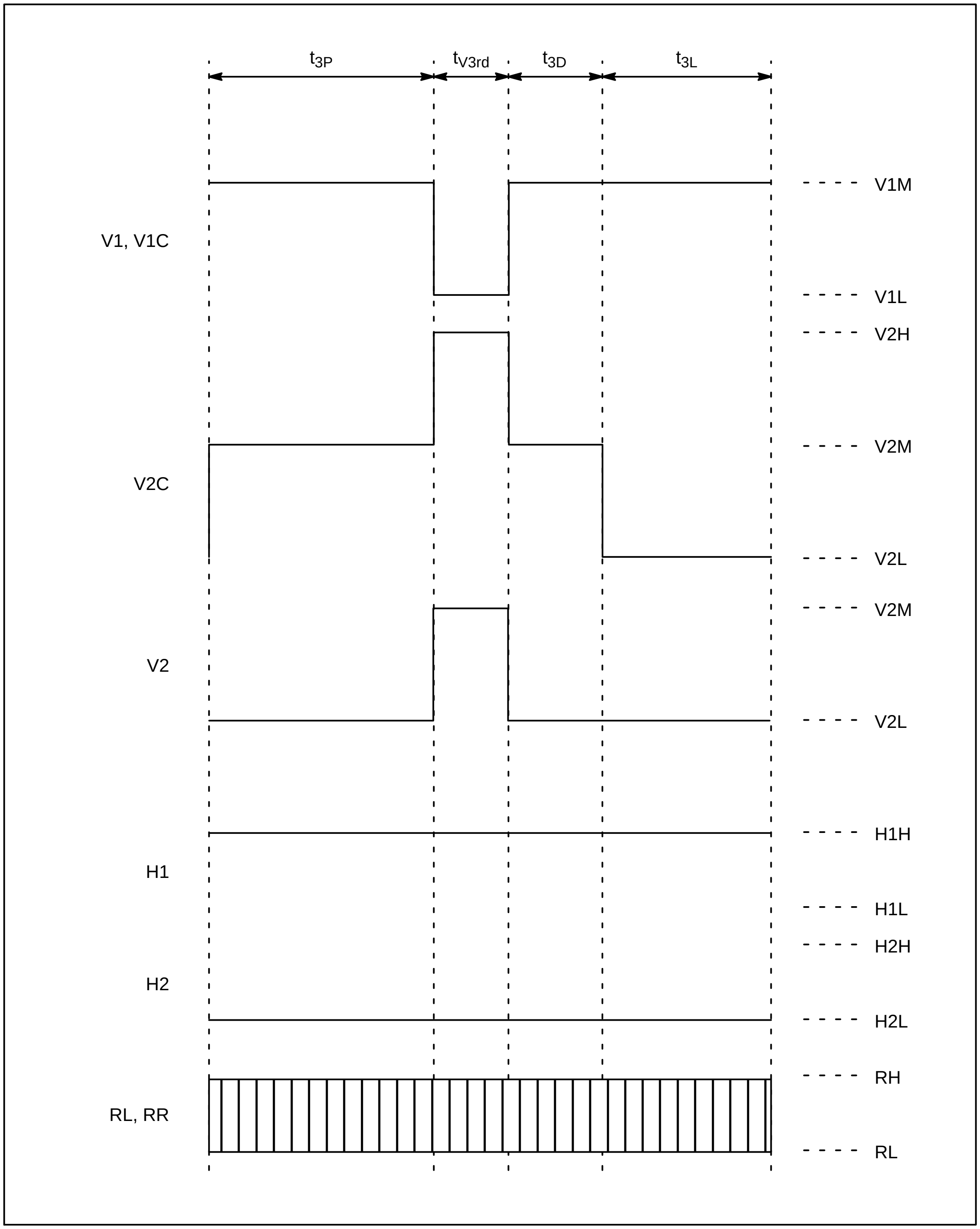


Figure 17. Timing Sequence C

Timing Sequence D: No Vertical CCD Line Transfer, Readout of One Horizontal CCD Line

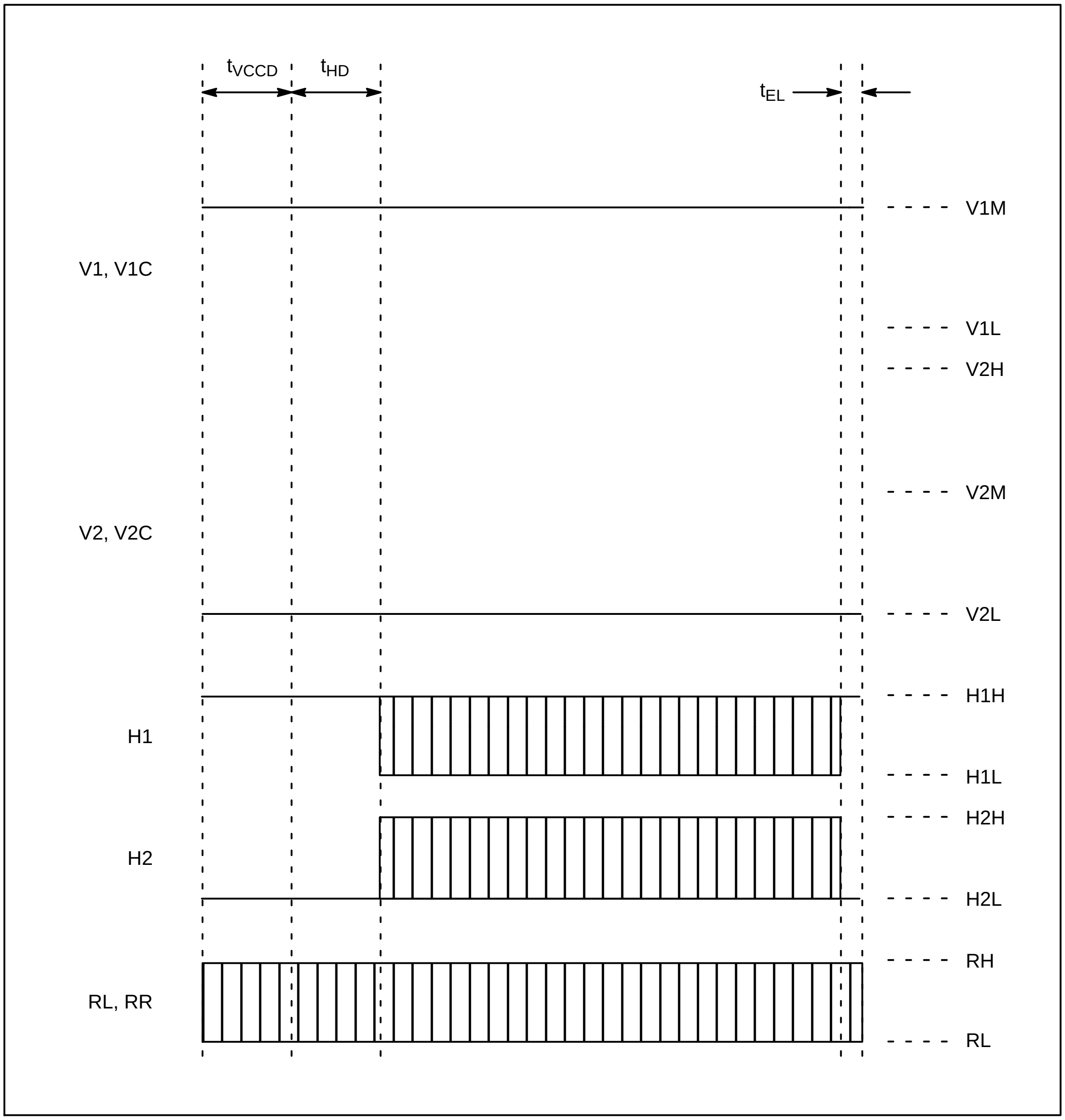


Figure 18. Timing Sequence D

Timing Modes

Sensor Architecture

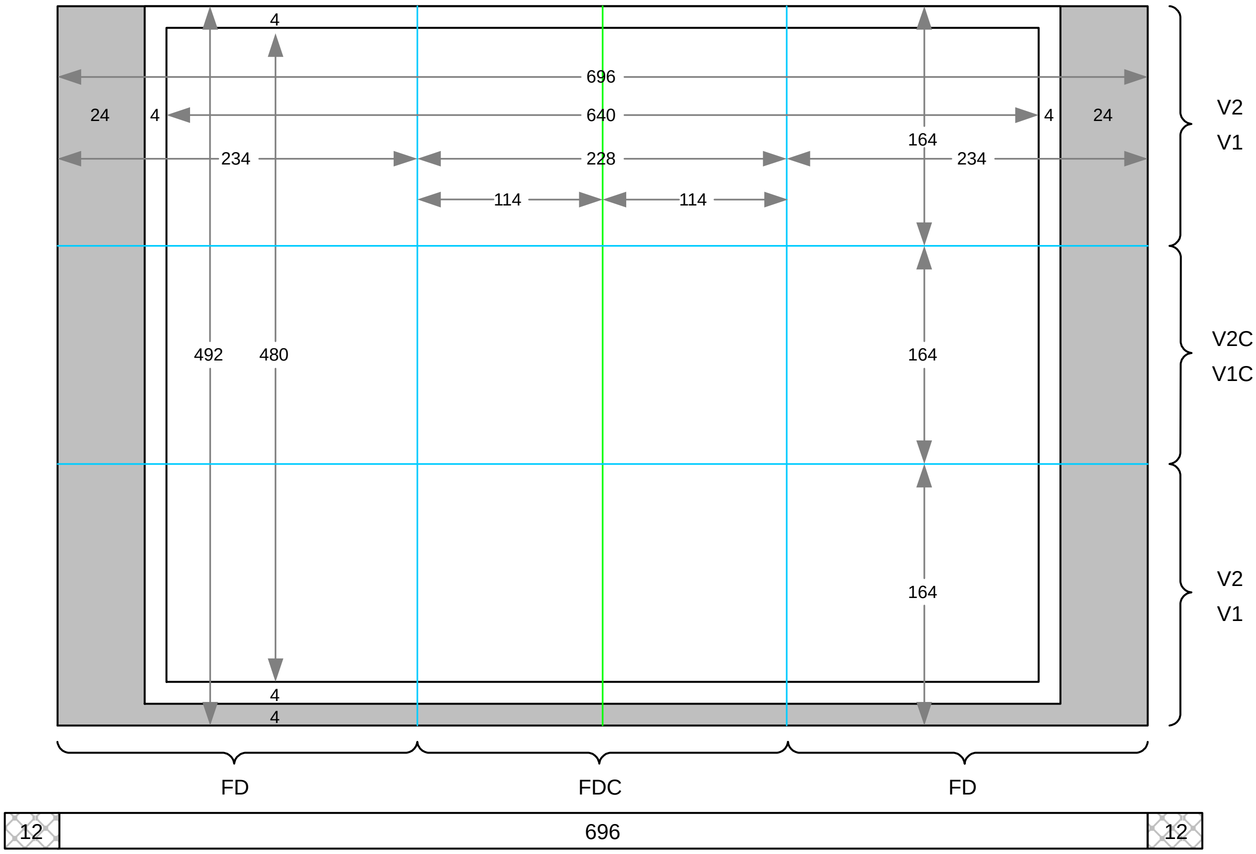
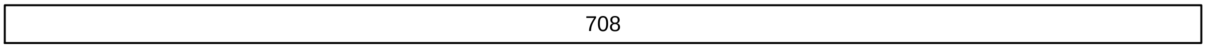
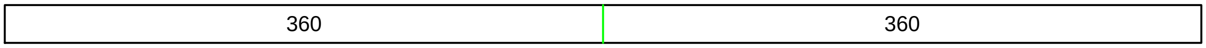


Figure 19. Sensor Architecture

When the sensor is operated in single output mode using the left output, the horizontal CCD is 708 pixels long. This assumes no horizontal over clocking is done.



When the sensor is operated in dual output mode, the horizontal CCD is dived into left and right registers. Each half of the register is 360 pixels long. This assumes no horizontal over clocking is done.



One Output Full Field

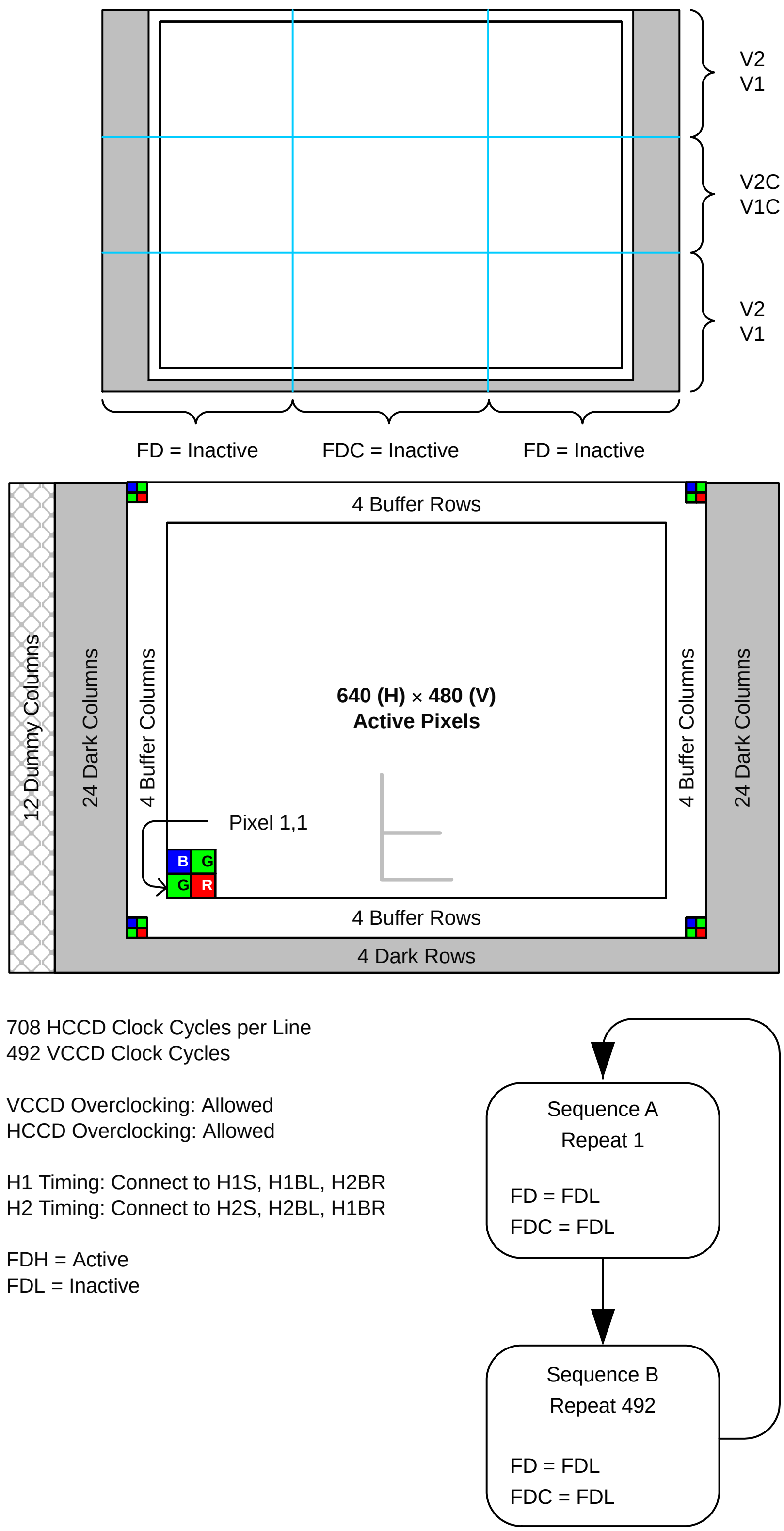
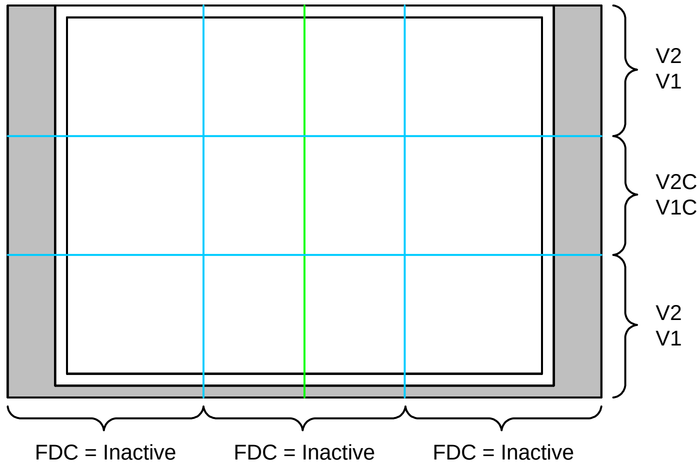
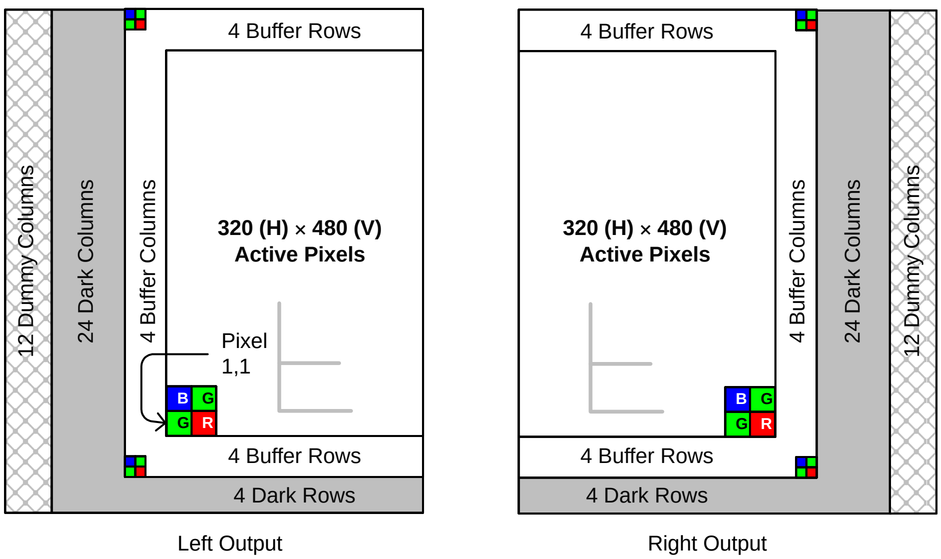


Figure 20. One Output Full Field

Two Outputs Full Field





360 HCCD Clock Cycles per Line
492 VCCD Clock Cycles

VCCD Overclocking: Allowed
HCCD Overclocking: Allowed

H1 Timing: Connect to H1S, H1BL, H1BR
H2 Timing: Connect to H2S, H2BL, H2BR

FDH = Active
FDL = Inactive

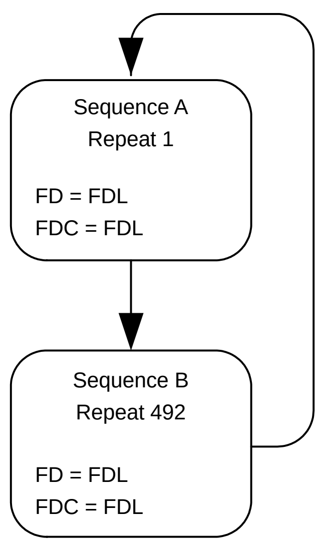
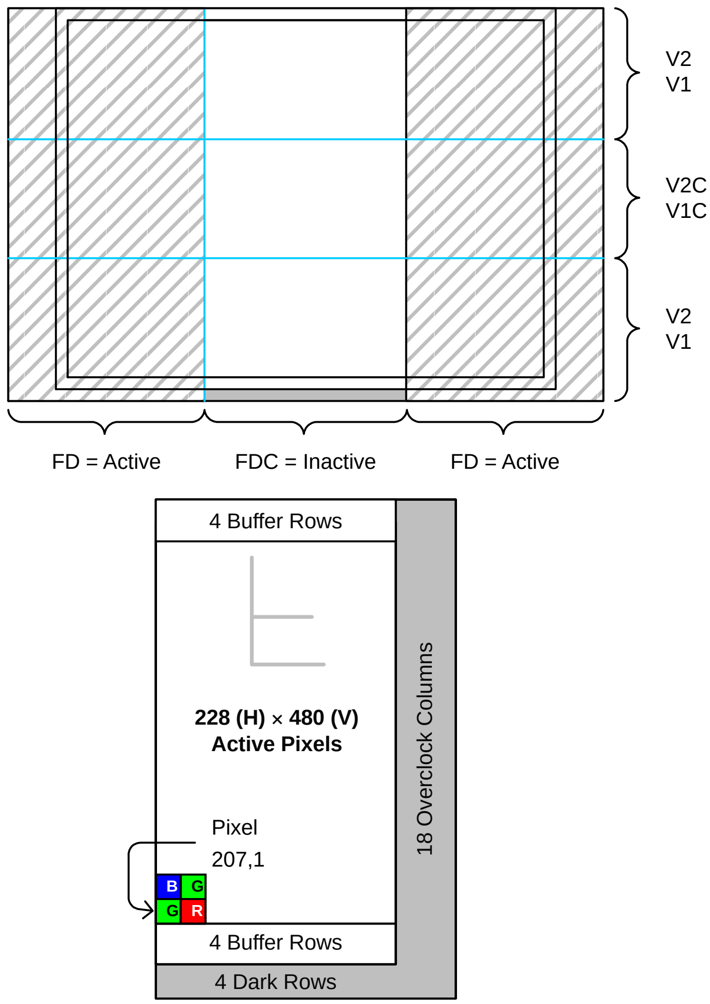


Figure 21. Two Outputs Full Field

One Output Center Columns



246 HCCD Clock Cycles per Line
492 VCCD Clock Cycles

VCCD Overclocking: Allowed
HCCD Overclocking: **Not** Allowed

H1 Timing: Connect to H1S, H1BL, H2BR
H2 Timing: Connect to H2S, H2BL, H1BR

FDH = Active
FDL = Inactive

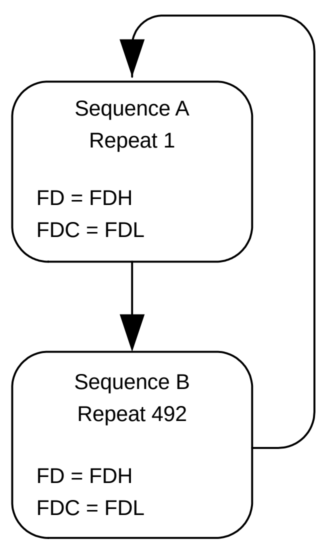
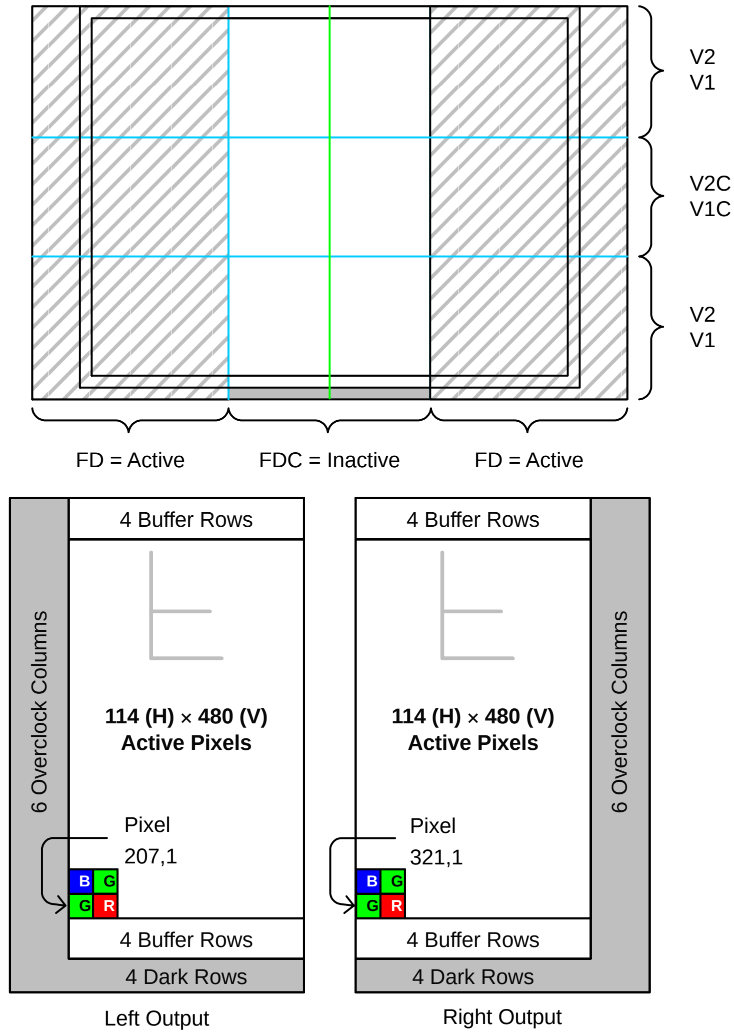


Figure 22. One Output Center Columns

Two Outputs Center Columns



120 HCCD Clock Cycles per Line
492 VCCD Clock Cycles

VCCD Overclocking: Allowed
HCCD Overclocking: **Not** Allowed

H1 Timing: Connect to H1S, H1BL, H1BR
H2 Timing: Connect to H2S, H2BL, H2BR

FDH = Active
FDL = Inactive

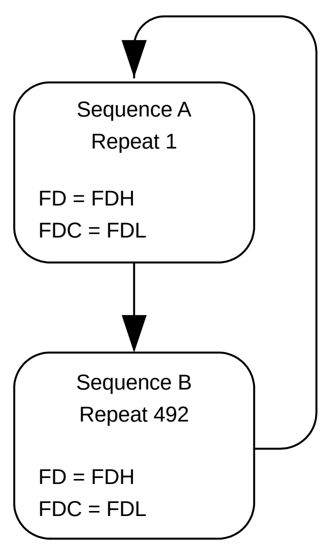


Figure 23. Two Outputs Center Columns

One Output Center Rows

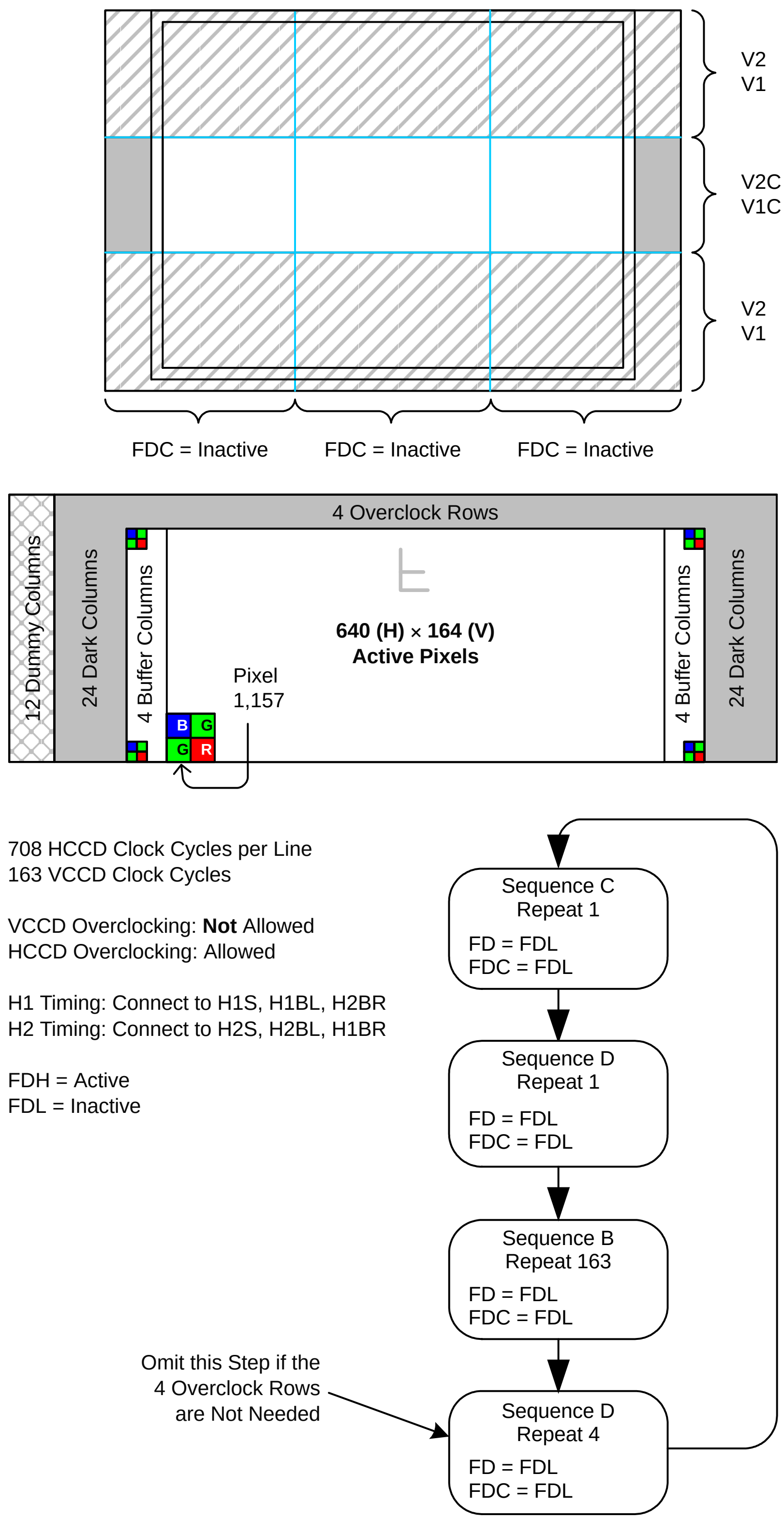
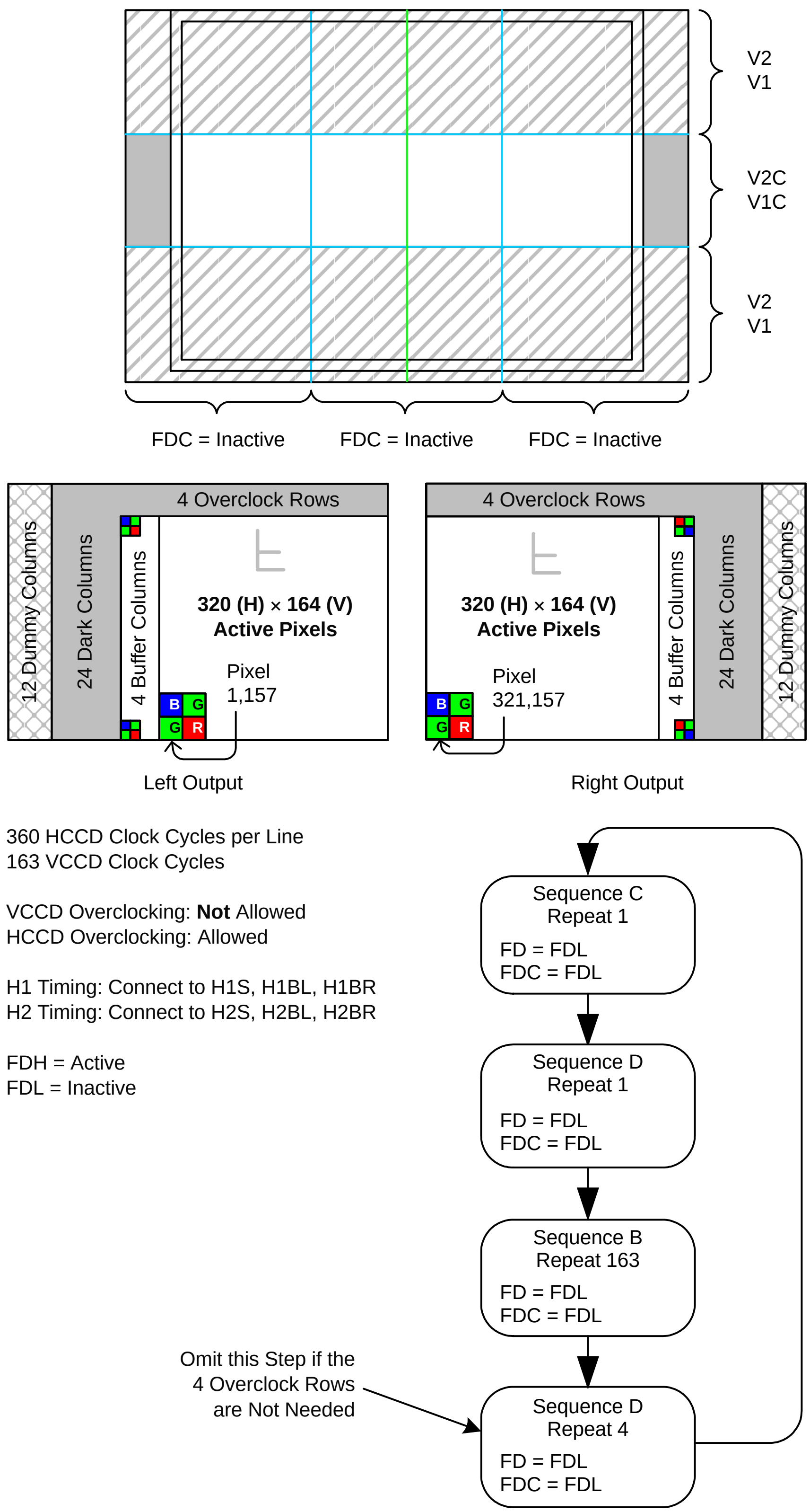


Figure 24. One Output Center Rows

Two Outputs Center Rows



360 HCCD Clock Cycles per Line
163 VCCD Clock Cycles

VCCD Overclocking: **Not** Allowed
HCCD Overclocking: Allowed

H1 Timing: Connect to H1S, H1BL, H1BR
H2 Timing: Connect to H2S, H2BL, H2BR

FDH = Active
FDL = Inactive

Figure 25. Two Outputs Center Rows

One Output Center Rows and Columns

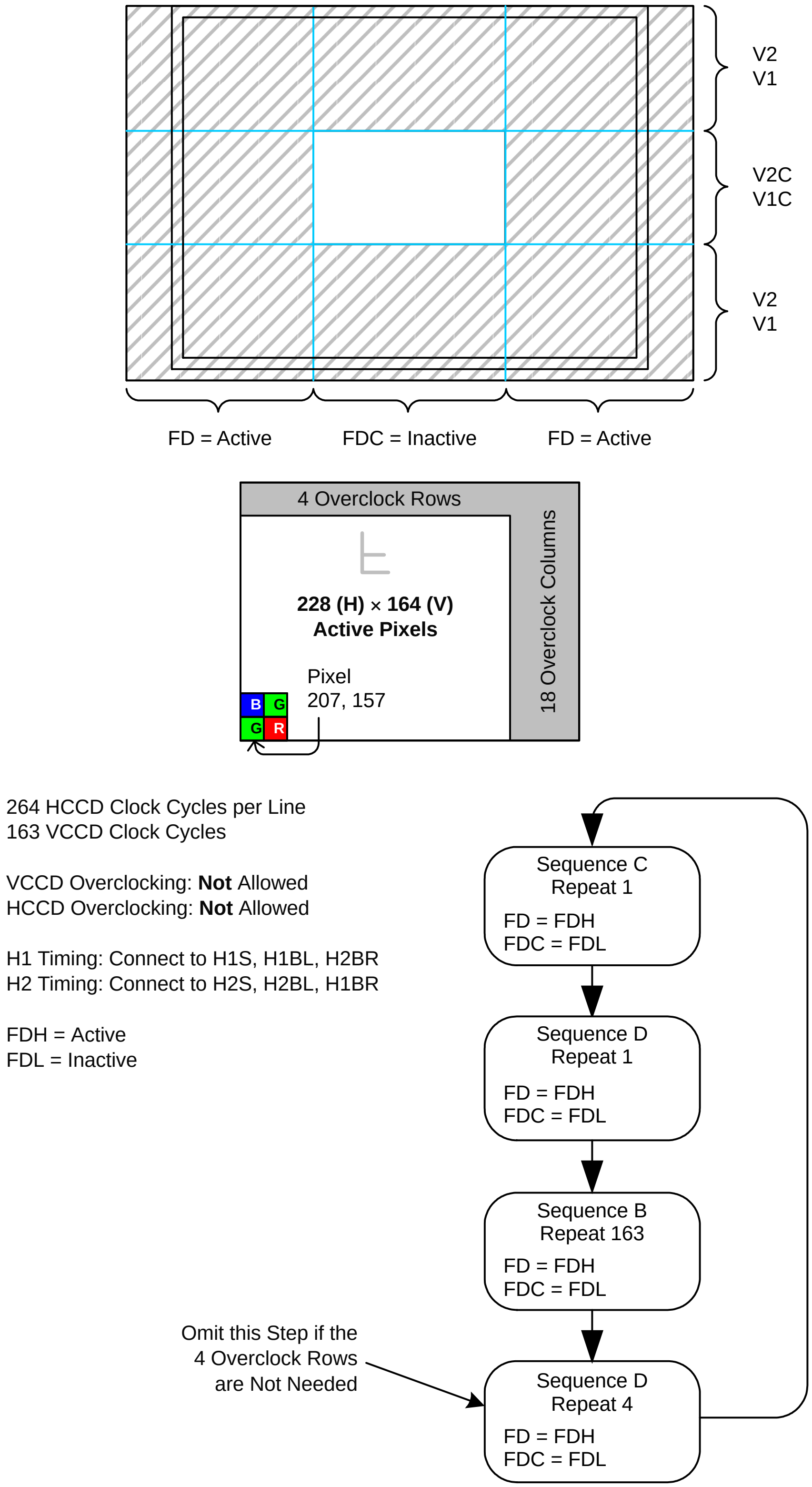


Figure 26. One Output Center Rows and Columns

Two Outputs Center Rows and Columns

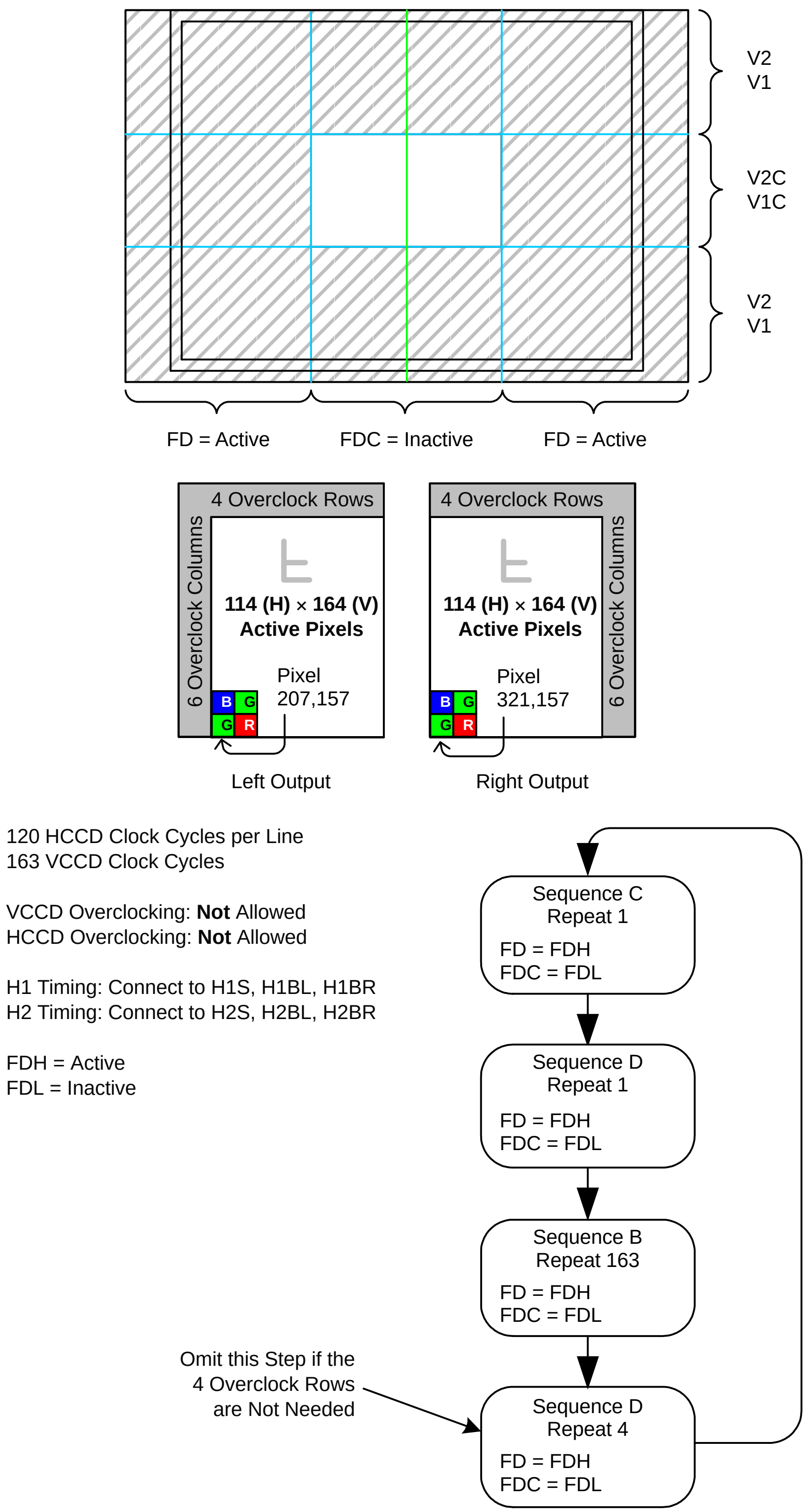


Figure 27. Two Outputs Center Rows and Columns

Timing Details

Pixel Timing

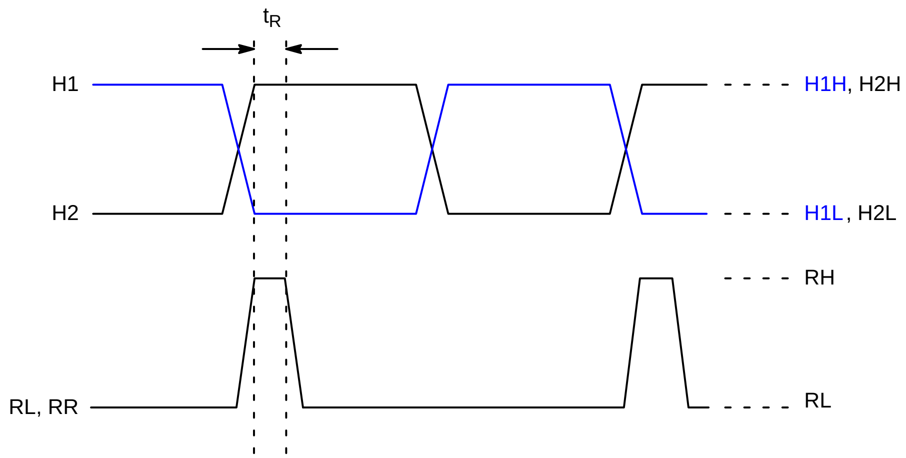


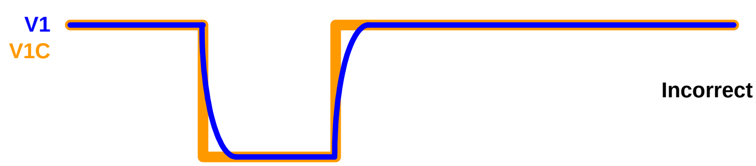
Figure 28. Pixel Timing Detail

Vertical Clock Phase 1 − Line Timing Detail

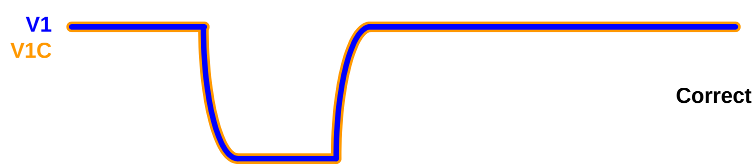
The following timing detail applies if any of the center row timing modes are selected. If the center row timing modes are not to be used, then the V1 and V1C pins should be tied together and driven from one clock driver.

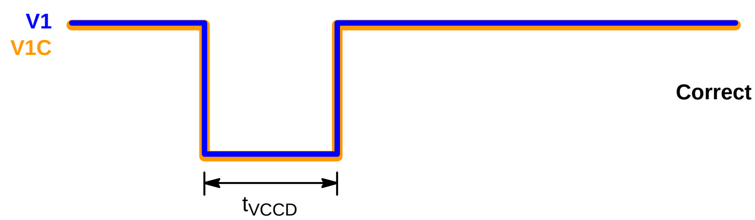
During the line timing, the V1 and V1C rise and fall times need to be identical. Since the V1 capacitance is approximately twice the V1C capacitance, the clock driver circuits must be adjusted to ensure equal rise and fall times.

The figure below is an example of unacceptable V1 and V1C clock waveforms.



The figures below are examples of acceptable V1 and V1C clock waveforms.



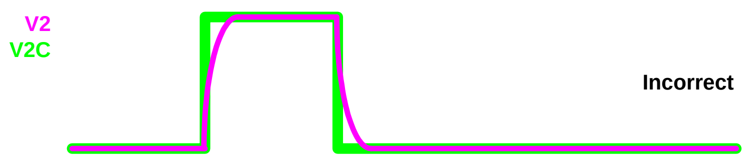


Vertical Clock Phase 2 − Line Timing Detail

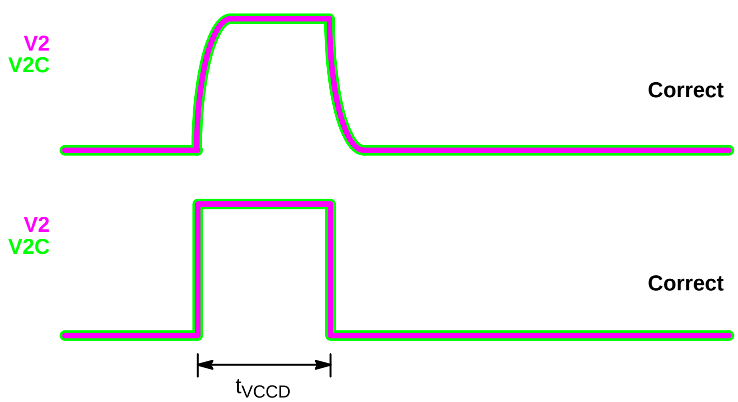
The following timing detail applies if any of the center row timing modes are selected. If the center row timing modes are not to be used, then the V2 and V2C pins should be tied together and driven from one clock driver.

During the line timing, the V2 and V2C rise and fall times need to be identical. Since the V2 capacitance is approximately twice the V2C capacitance, the clock driver circuits must be adjusted to ensure equal rise and fall times.

The figure below is an example of unacceptable V2 and V2C clock waveforms.

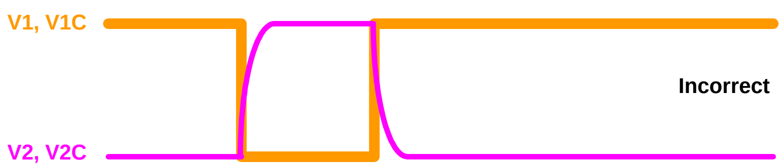


The figures below are examples of acceptable V2 and V2C clock waveforms.

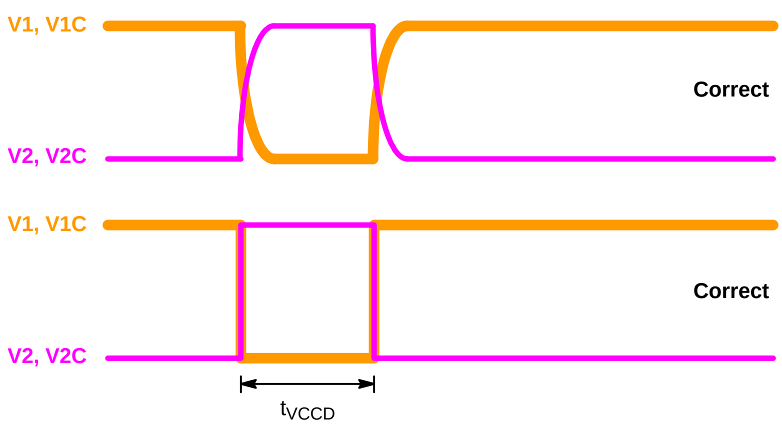


Vertical Clock Phases 1 and 2 − Line Timing Detail

The following line timing detail applies to all modes. The V1 and V1C clocks must be symmetrical to the V2 and V2C clocks. The figure below is an example of unacceptable V1, V1C, V2 and V2C clock waveforms.



The figures below are of acceptable V1, V1C, V2 and V2C clock waveforms.

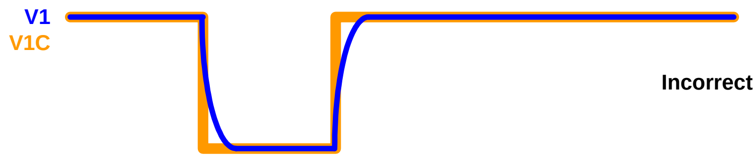


Vertical Clock Phase 1 − Frame Timing Detail

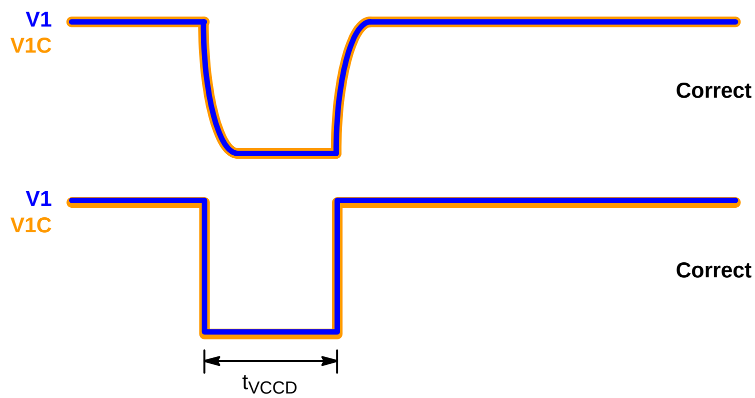
The following timing detail applies if any of the center row timing modes are selected. If the center row timing modes are not to be used, then the V1 and V1C pins should be tied together and driven from one clock driver.

During the frame timing, the V1 and V1C rise and fall times need to be identical. Since the V1 capacitance is approximately twice the V1C capacitance, the clock driver circuits must be adjusted to ensure equal rise and fall times.

The figure below is an example of unacceptable V1 and V1C clock waveforms.



The figures below are examples of acceptable V1 and V1C clock waveforms

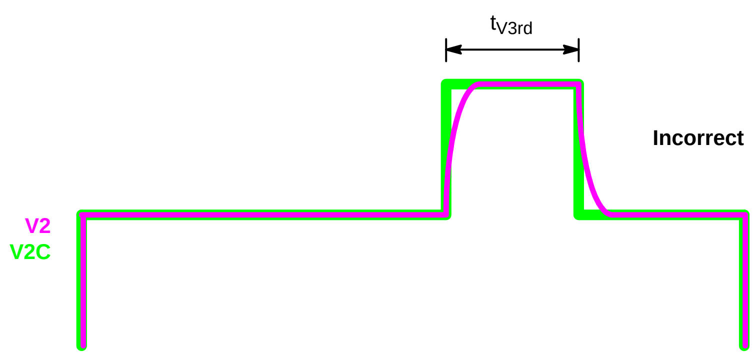


Vertical Clock Phase 2 − Frame Timing Detail

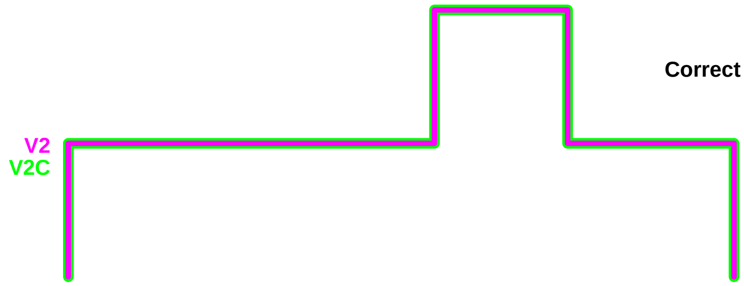
The following timing detail applies if any of the center row timing modes are selected. If the center row timing modes are not to be used, then the V2 and V2C pins should be tied together and driven from one clock driver.

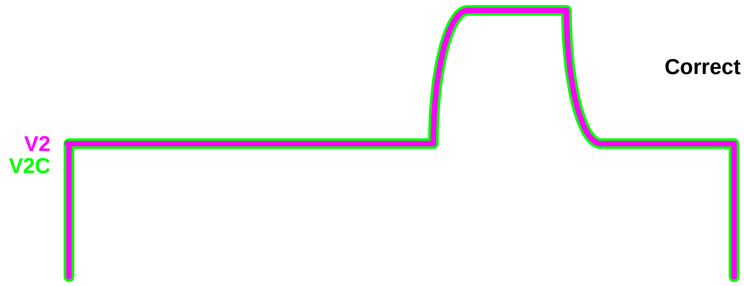
During the frame timing, the V2 and V2C rise and fall times need to be identical. Since the V2 capacitance is approximately twice the V2C capacitance, the clock driver circuits must be adjusted to ensure equal rise and fall times.

The figure below is an example of unacceptable V2 and V2C clock waveforms during the frame timing.



The figures below are examples of acceptable V2 and V2C clock waveforms during the frame timing.

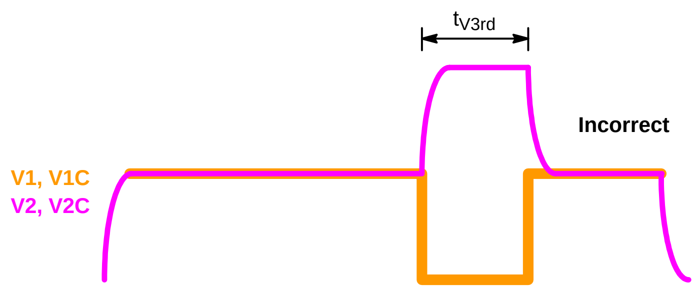




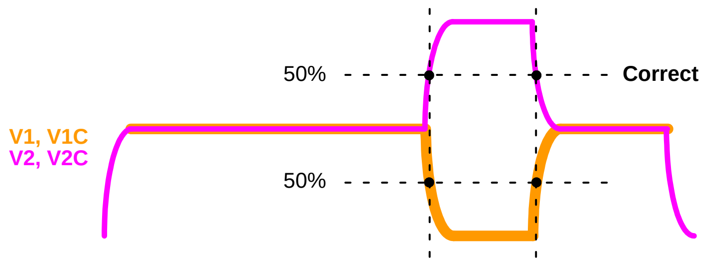
Vertical Clock Phases 1 and 2 − Frame Timing Detail

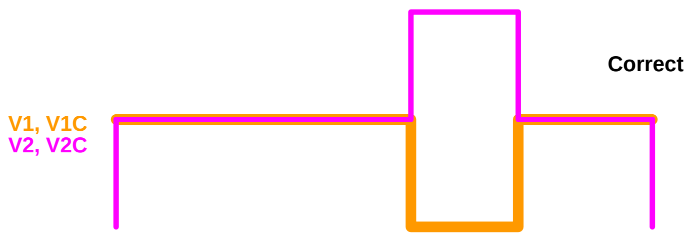
The following frame timing detail applies to all modes. The V1 and V1C clocks must be symmetrical to the V2 and V2C clocks. Also, during the t_{V3rd} timing, the V1 and V2 waveform edges should be aligned to occur at the same time.

The figure below is an example of unacceptable V1, V1C, V2 and V2C clock waveforms.



The figures below are of acceptable V1, V1C, V2 and V2C clock waveforms.





Electronic Shutter Timing

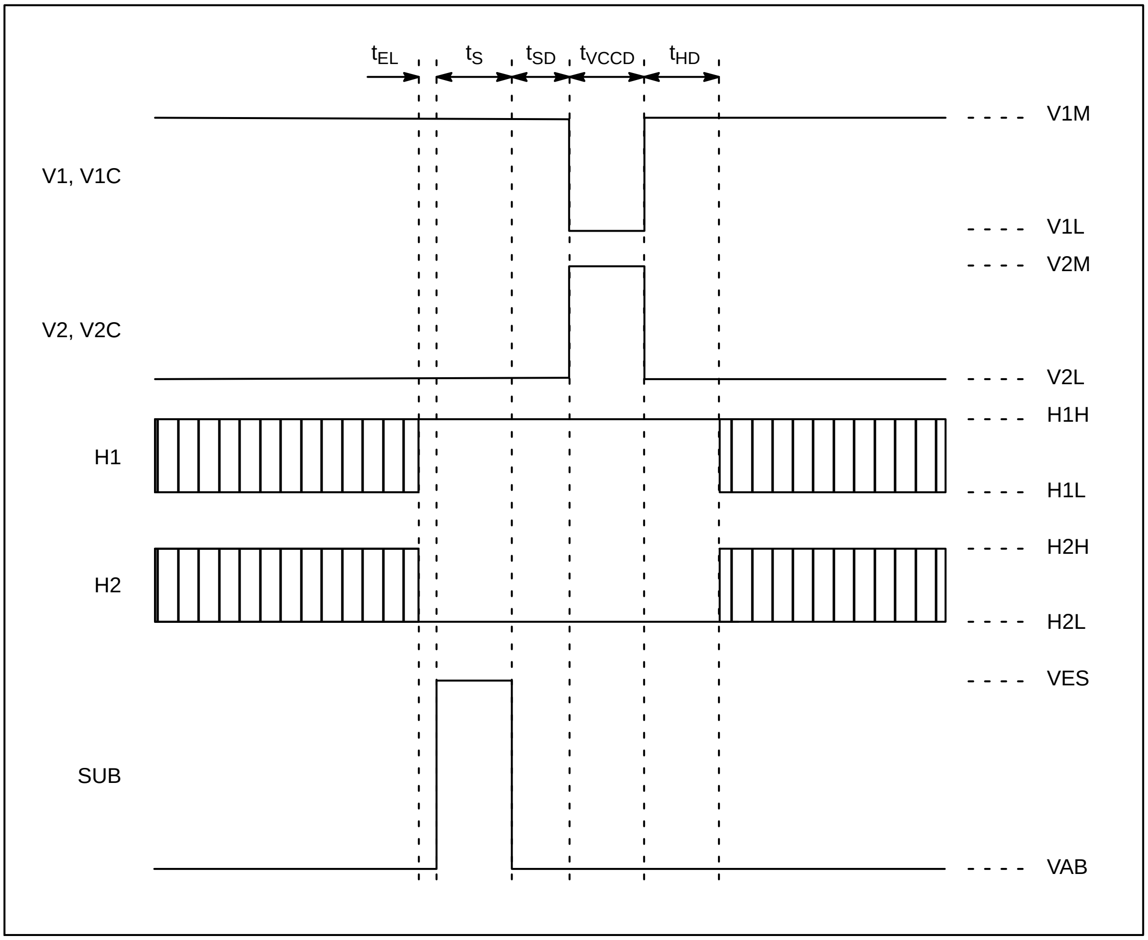


Figure 29. Electronic Shutter Timing

Electronic Shutter − Integration Time Definition

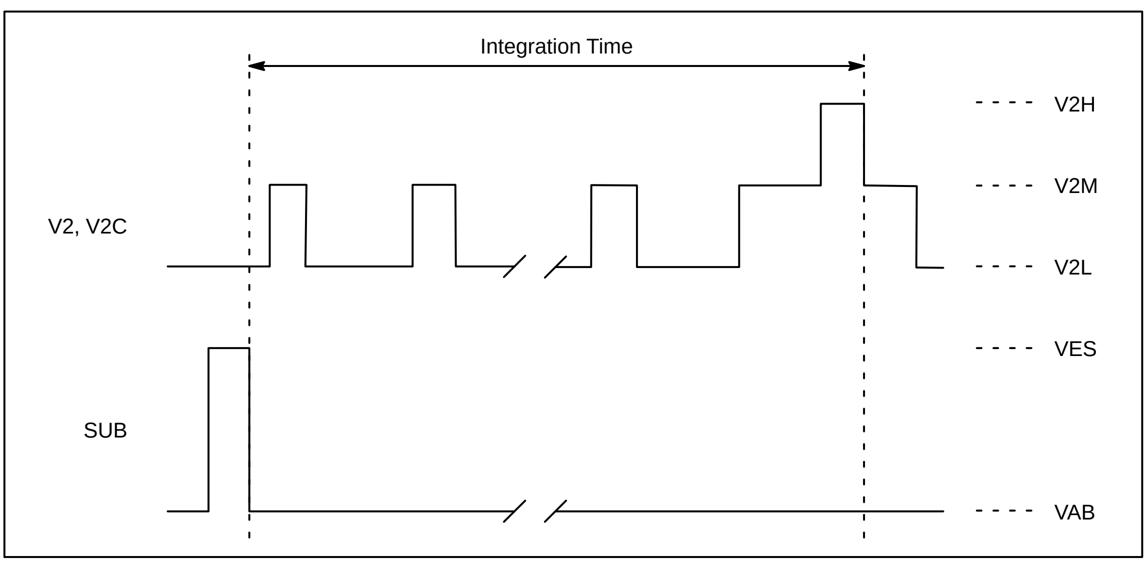


Figure 30. Integration Time Definition

Fast Line Dump Timing

The figure below shows an example of dumping three lines for all rows.

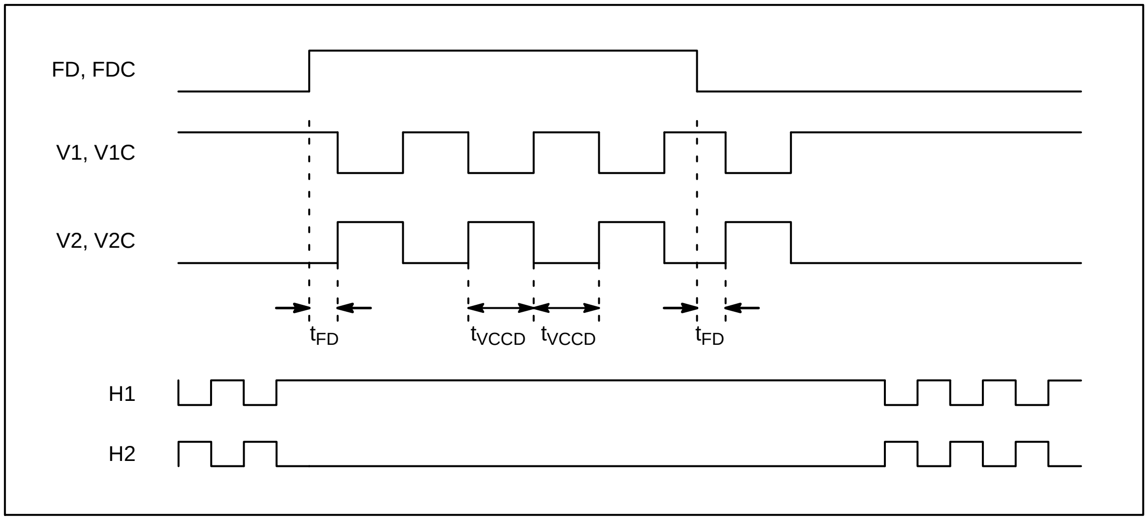


Figure 31. Fast Line Dump Timing

Example HCCD Clock Driver

The HCCD clock inputs should be driven by buffers capable of driving a capacitance of 40 pF and having a full voltage swing of at least 4.7 V. A 74AC04 or equivalent is recommended to drive the HCCD. The HCCD requires a 0.0 to 5.0 V clock. This clock level can be obtained by capacitive coupling and a diode to clamp the high level to ground. Resistors R2 and R6 are used to dampen the signal to prevent overshoots. The values of resistors R2 and R6 shown in the schematics below are only suggestions. The actual value required should be selected for each camera design.

<u>Single Output Only:</u>

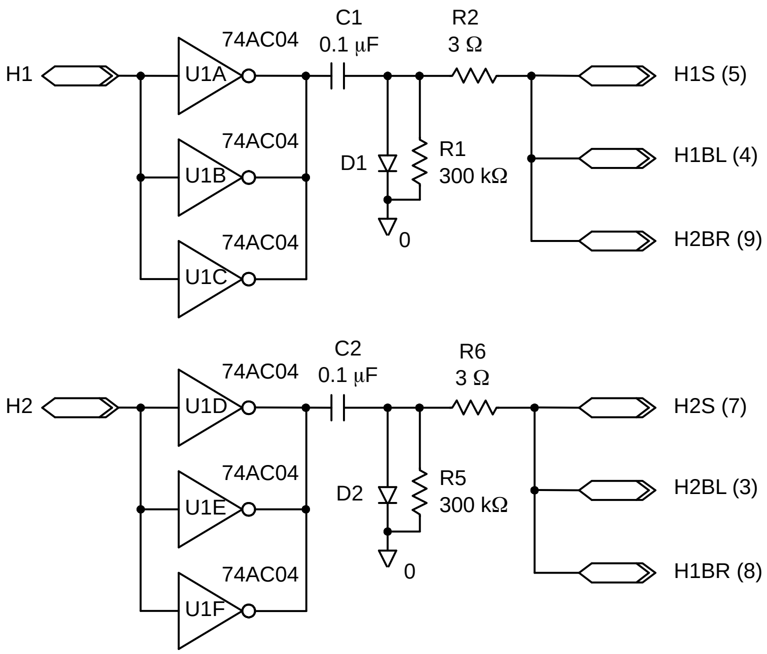


Figure 32. Single Output Only

Dual Output Only:

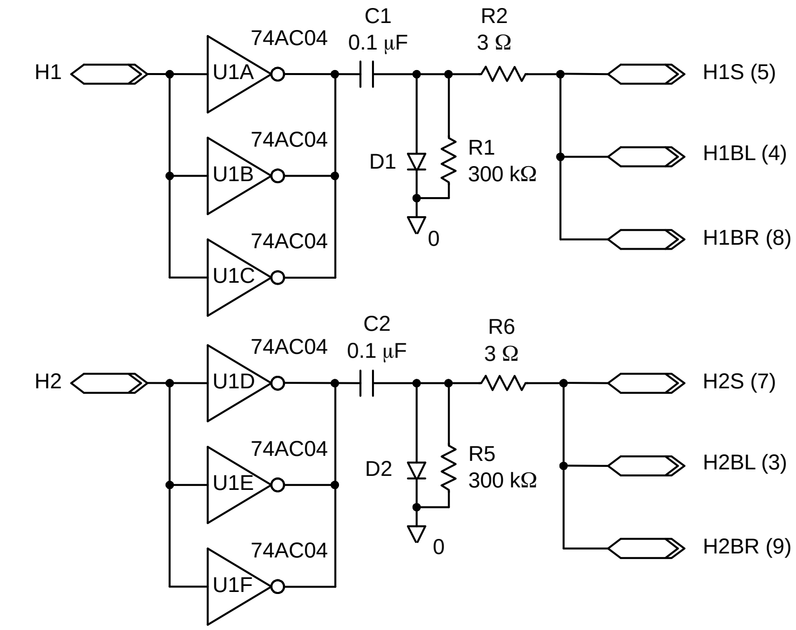


Figure 33. Dual Output Only

Selectable Single or Dual Output:

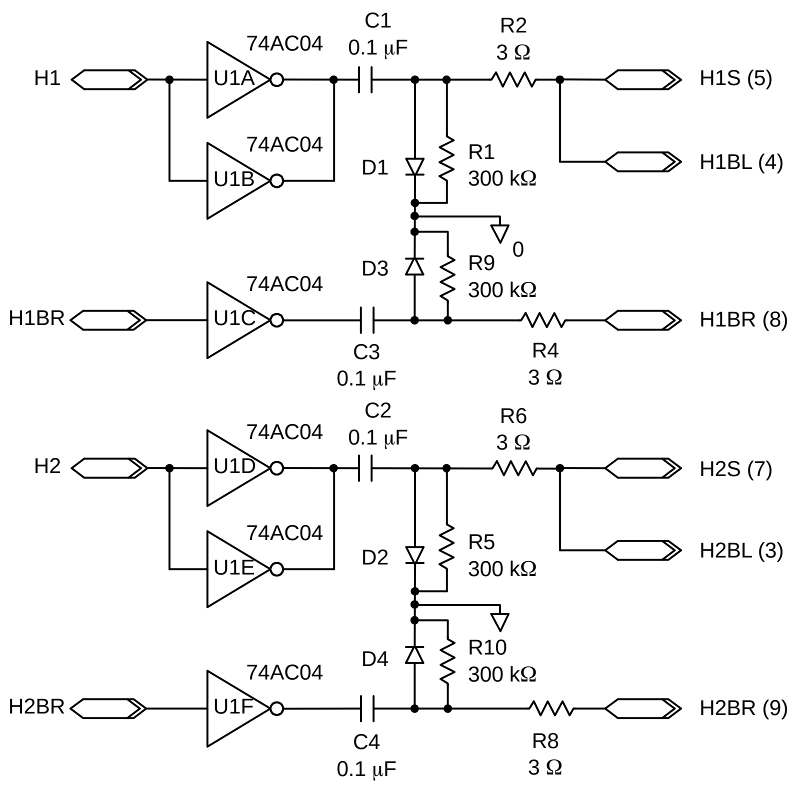


Figure 34. Selectable Single or Dual Output

The inputs to the above circuits, H1 and H2, are 5 V logic from the timing generator (a programmable gate array for example). If the camera is to have selectable single or dual output modes of operation, then the timing logic needs to generate two extra signals for the H1BR and H2BR timing. For single output mode program the timing such that H1BR = H2 and H2BR = H1. For dual output mode program the timing such that H1BR = H1 and H2BR = H2.

STORAGE AND HANDLING

Table 15. CLIMATIC REQUIREMENTS

Description	Symbol	Minimum	Maximum	Unit
Temperature (Note 29)	T_{ST}	−55	80	°C
Humidity (Note 30)	RH	5	90	%

29. Long-term exposure toward the maximum temperature will accelerate color filter degradation.
30. T = 25°C. Excessive humidity will degrade MTTF.

For information on ESD and cover glass care and cleanliness, please download the *Image Sensor Handling and Best Practices* Application Note (AN52561/D) from www.onsemi.com.

For information on environmental exposure, please download the *Using Interline CCD Image Sensors in High Intensity Lighting Conditions* Application Note (AND9183/D) from www.onsemi.com.

For information on soldering recommendations, please download the Soldering and Mounting Techniques Reference Manual (SOLDERRM/D) from www.onsemi.com.

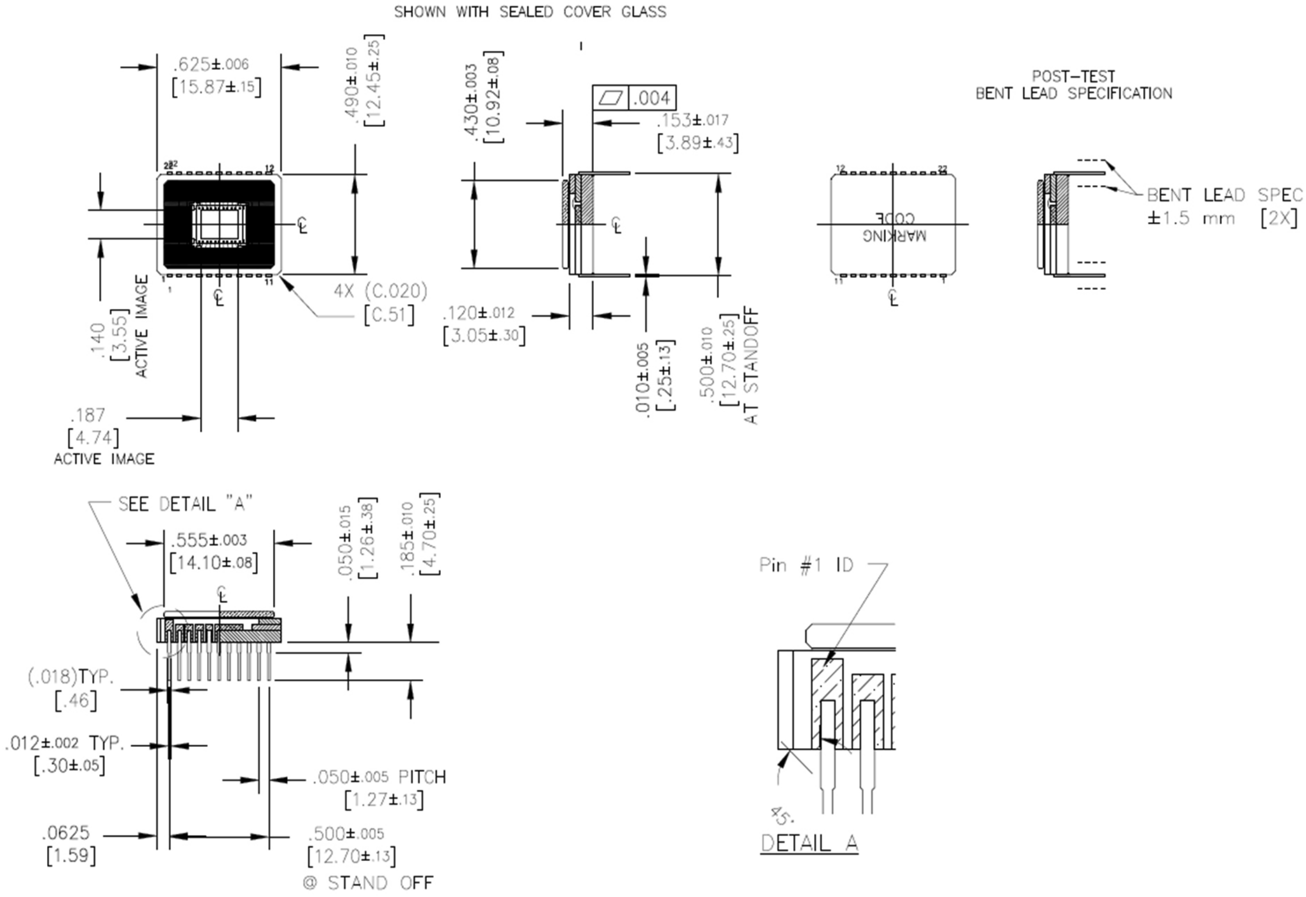
For quality and reliability information, please download the *Quality & Reliability* Handbook (HBD851/D) from www.onsemi.com.

For information on device numbering and ordering codes, please download the *Device Nomenclature* technical note (TND310/D) from www.onsemi.com.

For information on Standard terms and Conditions of Sale, please download Terms and Conditions from www.onsemi.com.

MECHANICAL INFORMATION

Completed Assembly

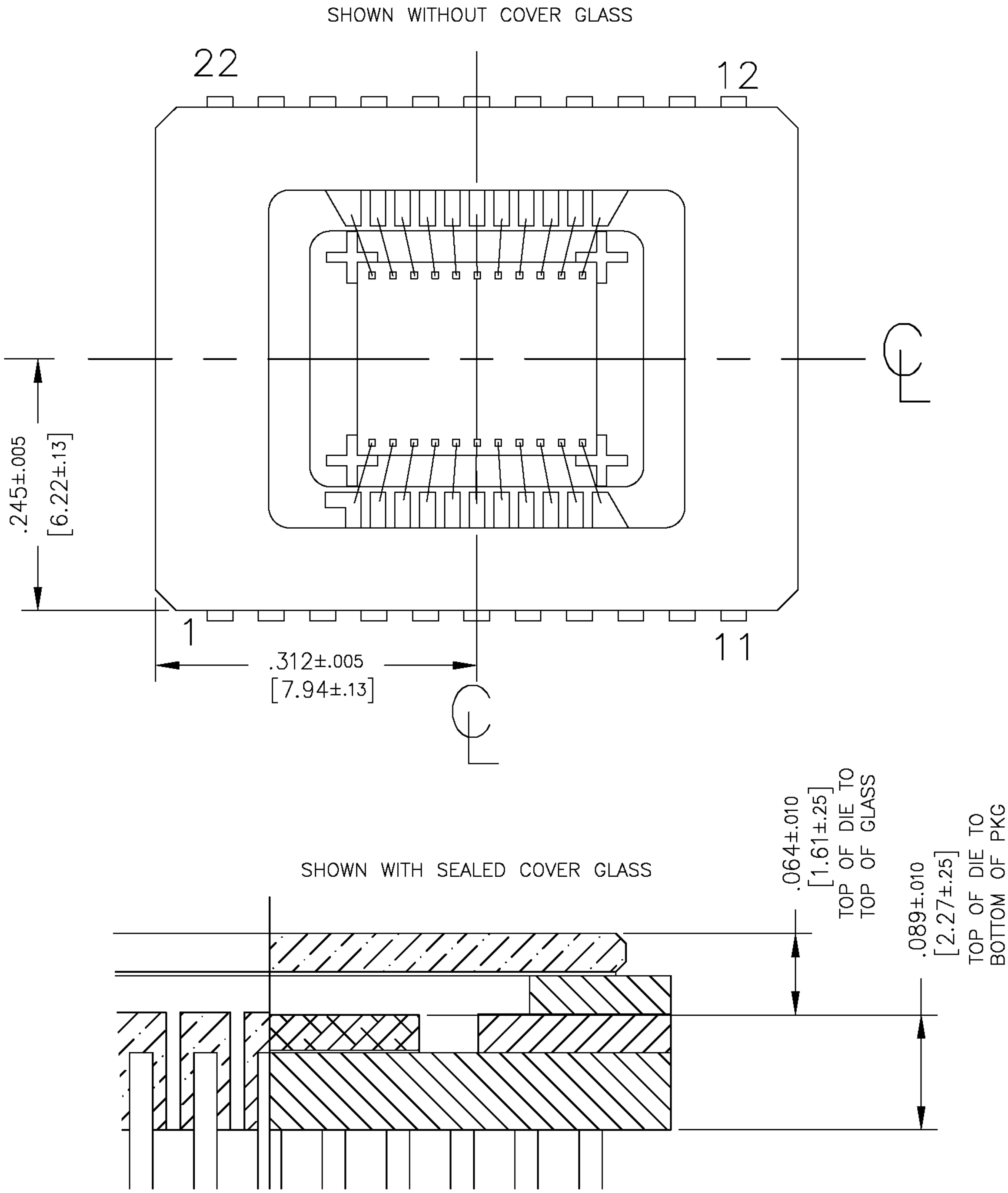


Notes:

31. See Available Part Configurations in Ordering Section for a description of the marking code.
32. Lid shall not extend beyond ceramic edge.
33. Light shield shown for reference only. Quartz version is smaller.
34. Units: IN [mm].

Figure 35. Completed Assembly

Die to Package Alignment



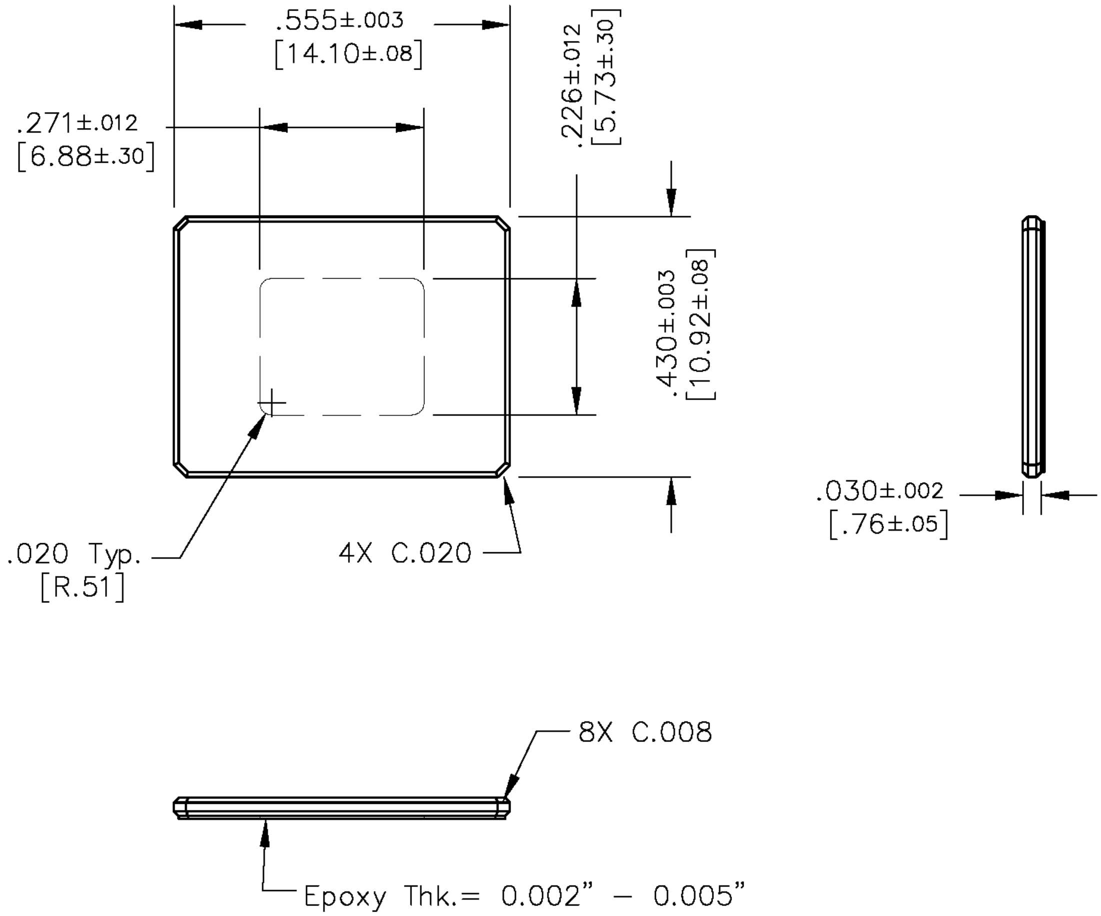
Notes:

35. Center of image area is offset from center of package by (0.00, 0.00) IN nominal.
36. Die is aligned within ±1 degree of any package cavity edge.
37. Units: IN [mm].

Figure 36. Die to Package Alignment

Glass

Clear Cover Glass

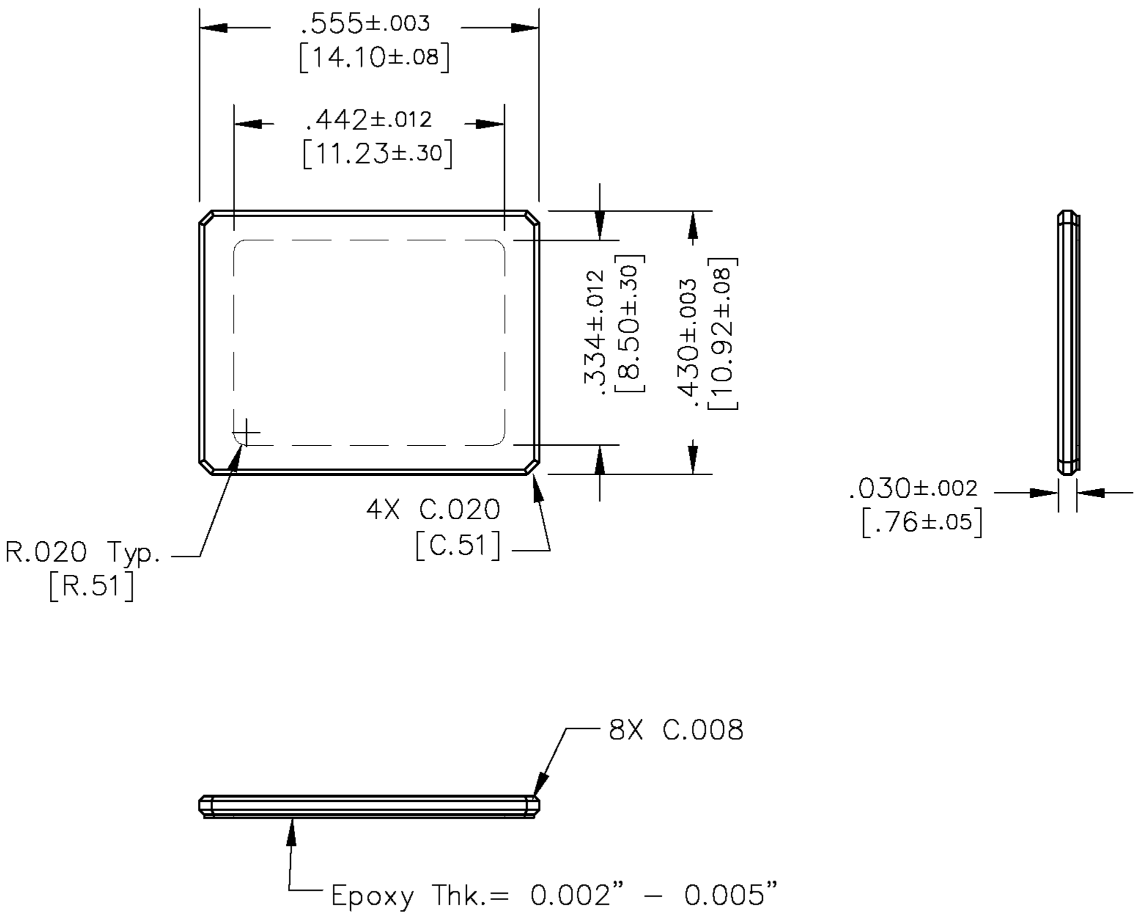


Notes:

38. Substrate: Schott D−263T eco or equivalent.
39. Top and Bottom edge chamfers = 0.008 [0.20].
40. Corner chamfers = 0.020 [0.50].
41. Dust, scratch, dig specification: 10 microns max.
42. Units: IN [mm].

Figure 37. Clear Cover Glass Drawing

Quartz Cover Glass



Notes:

43. Substrate: SK1300.
44. Top and Bottom edge chamfers = 0.008 [0.20].
45. Corner chamfers = 0.020 [0.50].
46. Dust, scratch, dig specification: 10 microns max.
47. Units: IN [mm].

Figure 38. Quartz Cover Glass Drawing

Glass Transmission

Clear Cover Glass

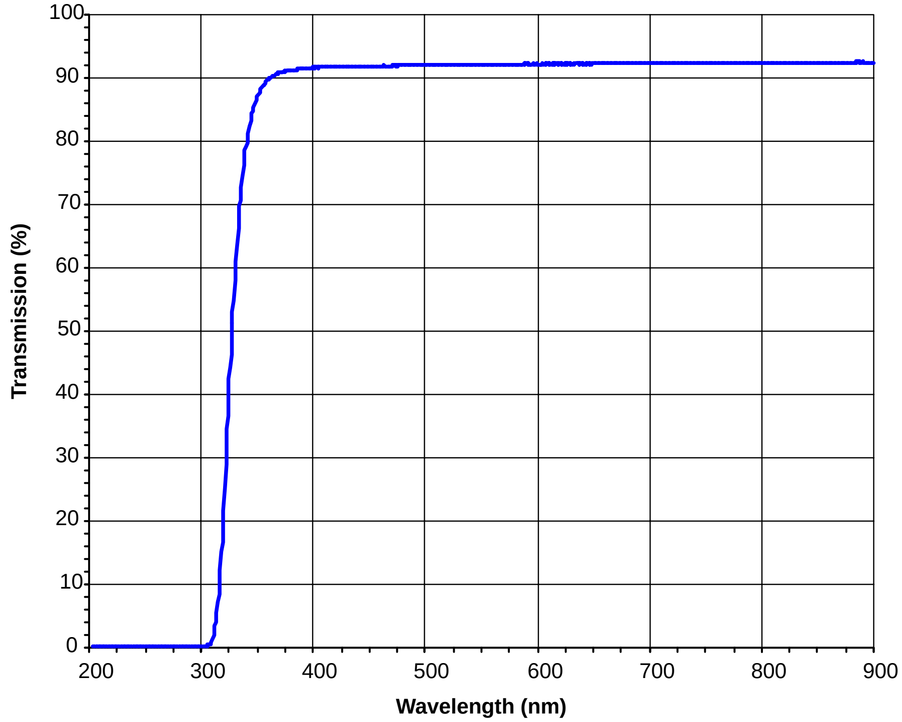


Figure 39. Clear Cover Glass Transmission

Quartz Cover Glass

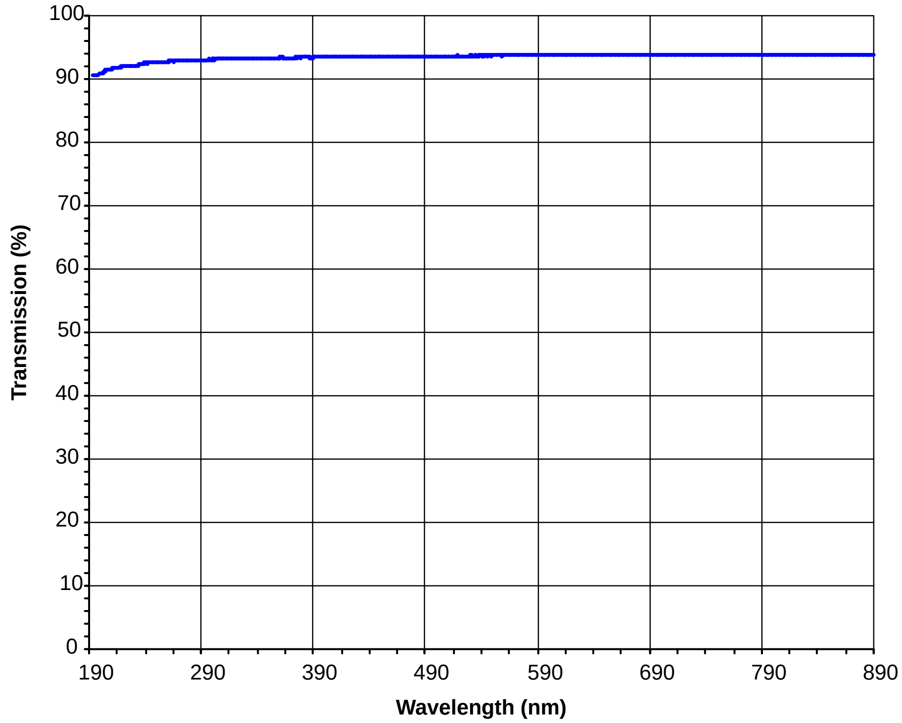


Figure 40. Quartz Cover Glass Transmission

PUBLICATION ORDERING INFORMATION

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