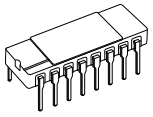
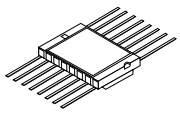
M54HC4060

RAD-HARD 14 STAGE BINARY COUNTER/OSCILLATOR

- HIGH SPEED:
  f_{MAX} = 65MHz (TYP.) at V_{CC} = 6V
- LOW POWER DISSIPATION:
  I_{CC} =4µA(MAX.) at T_A=25°C
- HIGH NOISE IMMUNITY:
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN.)
- SYMMETRICAL OUTPUT IMPEDANCE:
  $|I_{OH}| = I_{OL}$ = 4mA (MIN)
- BALANCED PROPAGATION DELAYS:
  $t_{PLH} \cong t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE:
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE WITH 54 SERIES 4060
- SPACE GRADE-1: ESA SCC QUALIFIED
- 50 krad QUALIFIED, 100 krad AVAILABLE ON REQUEST
- NO SEL UNDER HIGH LET HEAVY IONS IRRADIATION
- DEVICE FULLY COMPLIANT WITH SCC-9204-076



DILC-16



FPC-16

ORDER CODES

PACKAGE	FM	EM
DILC	M54HC4060D	M54HC4060D1
FPC	M54HC4060K	M54HC4060K1

DESCRIPTION

The M54HC4060 is an high speed CMOS 14-STAGE BINARY COUNTER/OSCILLATOR fabricated with silicon gate C^2MOS technology.

The oscillator configuration allows design of either RC or crystal oscillator circuits. A high level on the CLEAR accomplishes the reset function, i.e. all counter outputs are made low and the oscillator is disabled.
A negative transition on the clock input increments the counter. Ten kinds of divided output are provided; 4 to 10 and 12 to 14 stage inclusive. The maximum division available at Q12 is 1/16384 f oscillator.
The $\overline{Ø_1}$ input and the CLEAR input are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTION

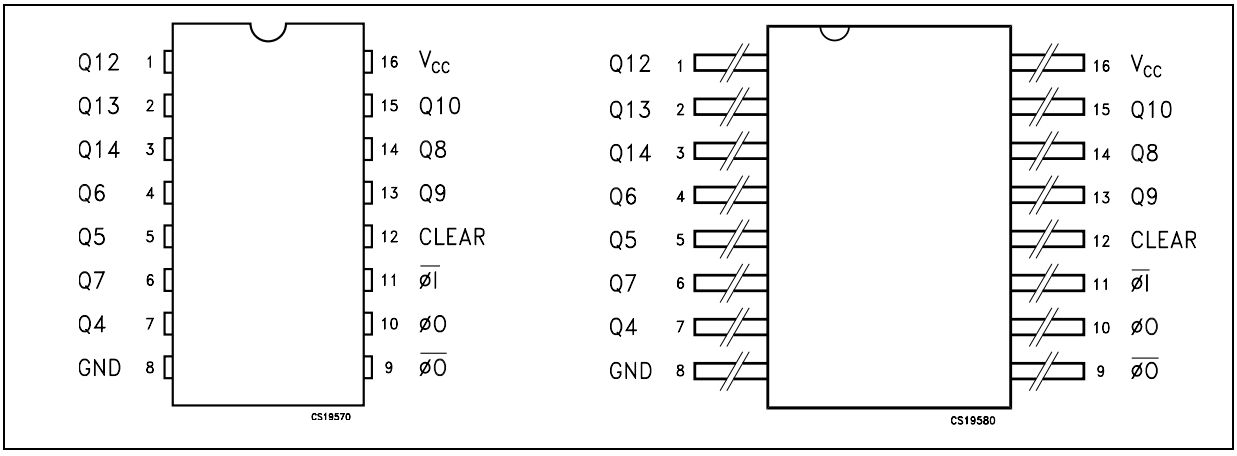


Figure 1: IEC Logic Symbols

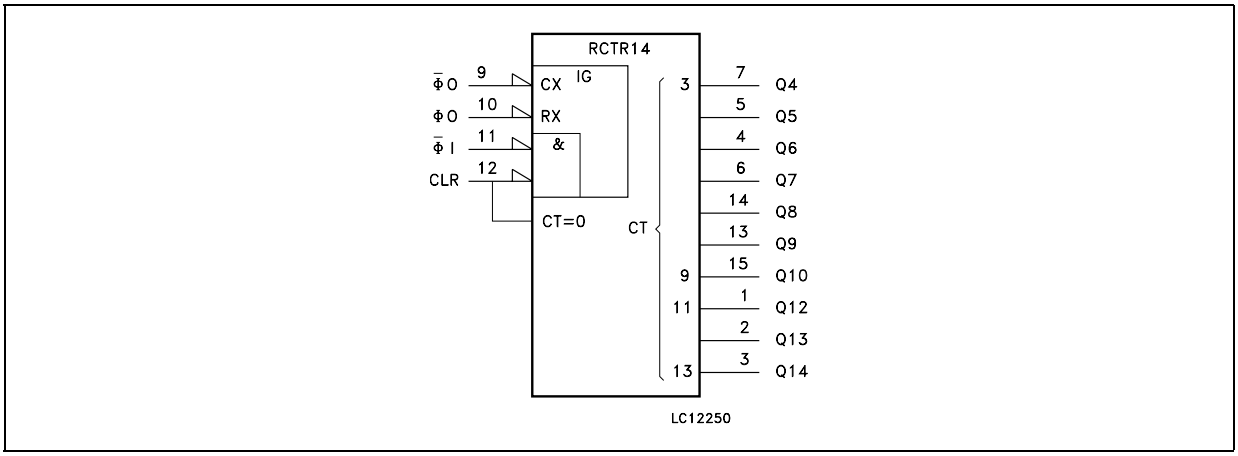


Figure 2: Input And Output Equivalent Circuit

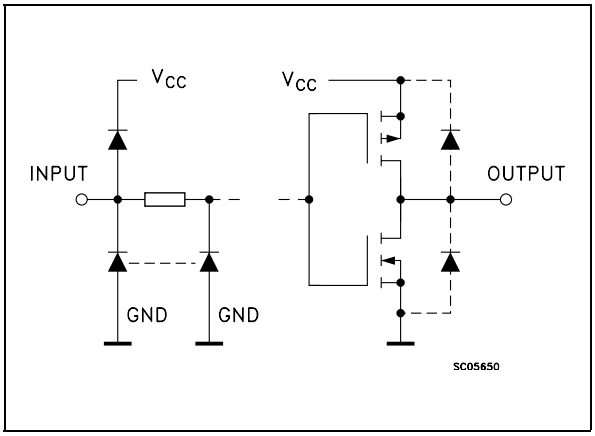


Table 1: Pin Description

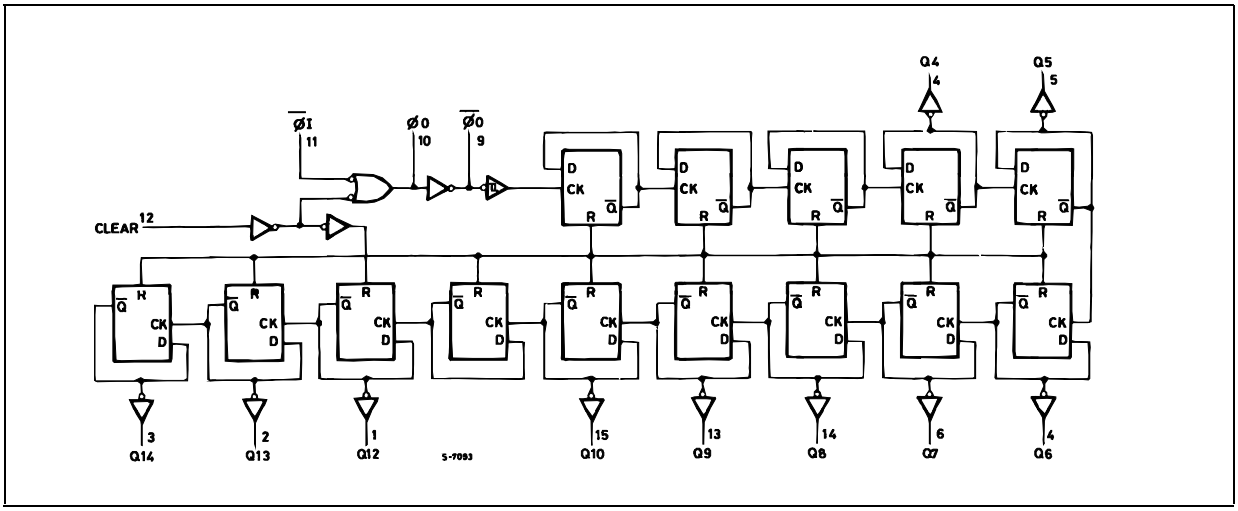
PIN N°	SYMBOL	NAME AND FUNCTION
1, 2, 3	Q12 to Q14	Counter Outputs
7, 5, 4, 6, 14, 13, 15	Q4 to Q10	Counter Outputs
9	$\overline{ØO}$	External Capacitor Connection
10	ØO	External Resistor Connection
11	$\overline{ØI}$	Clock Input / Oscillator Pin
12	CLEAR	Master Reset
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

Table 2: Truth Table

$\overline{ØI}$	CLEAR	FUNCTION
X	H	COUNTER IS RESET TO ZERO STATE $\overline{ØO}$ OUTPUT GOES TO HIGH LEVEL ØO OUTPUT GOES TO LOW LEVEL
⌐	L	COUNT UP ONE STEP
⌐	L	NO CHANGE

X : Don't Care

Figure 3: Logic Diagram



This logic diagram has not be used to estimate propagation delays

Table 3: Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	300	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	265	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

Table 4: Recommended Operating Conditions

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature		-55 to 125	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2.0V	0 to 1000	ns
		V_{CC} = 4.5V	0 to 500	ns
		V_{CC} = 6.0V	0 to 400	ns

Table 5: DC Specifications

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0		1.5			1.5		1.5		V
		4.5		3.15			3.15		3.15		
		6.0		4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0				0.5		0.5		0.5	V
		4.5				1.35		1.35		1.35	
		6.0				1.8		1.8		1.8	
V_{OH}	High Level Output Voltage (Q Output)	2.0	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5	I_O=-20 µA	4.4	4.5		4.4		4.4		
		6.0	I_O=-20 µA	5.9	6.0		5.9		5.9		
		4.5	I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0	I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage (Q Output)	2.0	I_O=20 µA		0.0	0.1		0.1		0.1	V
		4.5	I_O=20 µA		0.0	0.1		0.1		0.1	
		6.0	I_O=20 µA		0.0	0.1		0.1		0.1	
		4.5	I_O=4.0 mA		0.17	0.26		0.33		0.40	
		6.0	I_O=5.2 mA		0.18	0.26		0.33		0.40	
V_{OH}	High Level Output Voltage (ØO, $\overline{ØO}$ Output)	2.0	I_O=-20 µA	1.8	2.0		1.8		1.8		V
		4.5	I_O=-20 µA	4.4	4.5		4.0		4.0		
		6.0	I_O=-20 µA	5.5	5.9		5.5		5.5		
V_{OL}	Low Level Output Voltage (ØO, $\overline{ØO}$ Output)	2.0	I_O=-20 µA		0.0	0.2		0.2		0.2	V
		4.5	I_O=-20 µA		0.0	0.5		0.5		0.5	
		6.0	I_O=-20 µA		0.1	0.5		0.5		0.5	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND			± 0.1		± 1		± 1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND			4		40		80	µA

Table 6: AC Electrical Characteristics (C_L = 50 pF, Input $t_r = t_f$ = 6ns)

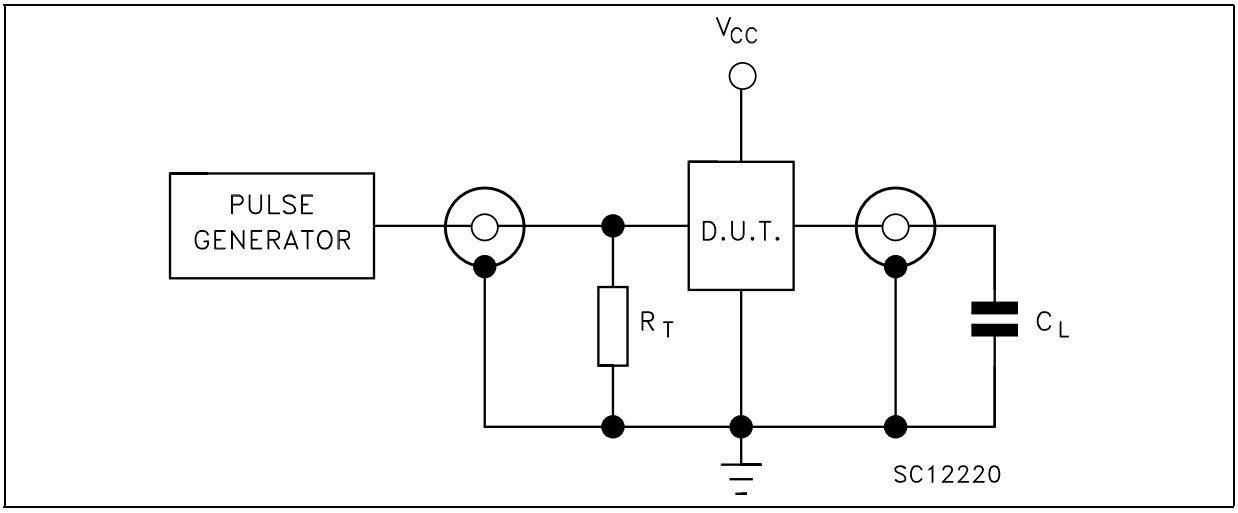
Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{ØI}$ - Q4)	2.0			170	300		375		450	ns
		4.5			41	60		75		90	
		6.0			30	51		64		76	
t_{PD}	Propagation Delay Time Difference (Qn - Qn+1)	2.0			32	75		95		110	ns
		4.5			7	15		19		22	
		6.0			5	13		16		19	
t_{PHL}	Propagation Delay Time (CLEAR - Qn)	2.0			85	195		245		295	ns
		4.5			23	39		49		59	
		6.0			17	33		42		50	
f_{MAX}	Maximum Clock Frequency	2.0		6	12		5		4		MHz
		4.5		30	50		24		20		
		6.0		35	65		28		24		
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width ($\overline{ØI}$)	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
$t_{W(H)}$	Minimum Pulse Width (CLEAR)	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{REM}	Minimum Removal Time	2.0			40	100		125		150	ns
		4.5			10	20		25		30	
		6.0			9	17		21		26	

Table 7: Capacitive Characteristics

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
C_{IN}	Input Capacitance	5.0			5	10		10		10	pF
C_{PD}	Power Dissipation Capacitance (note 1)	5.0			27						pF

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}$

Figure 4: Test Circuit



C_L = 50pF or equivalent (includes jig and probe capacitance)
$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 5: Waveform - Propagation Delay Times, Minimum Pulse Width ($\overline{ØI}$) (f=1MHz; 50% duty cycle)

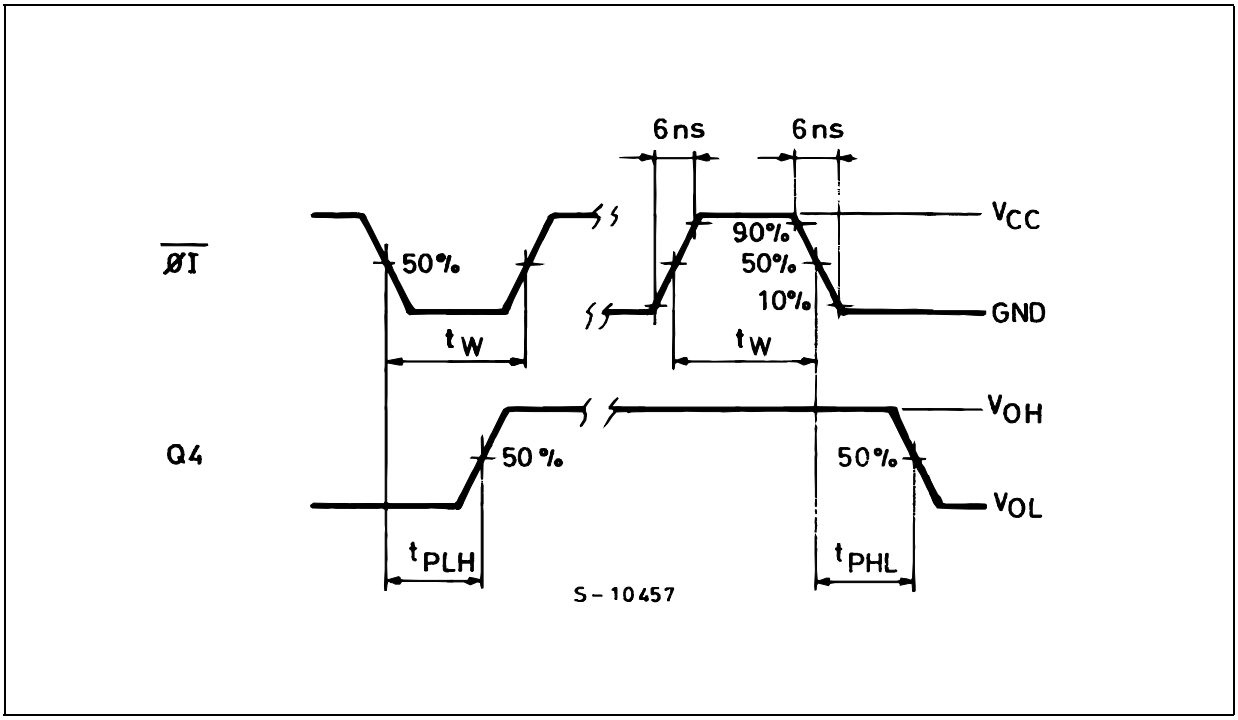


Figure 6: Waveform - Propagation Delay Times, Minimum Pulse Width (CLEAR) (f=1MHz; 50% duty cycle)

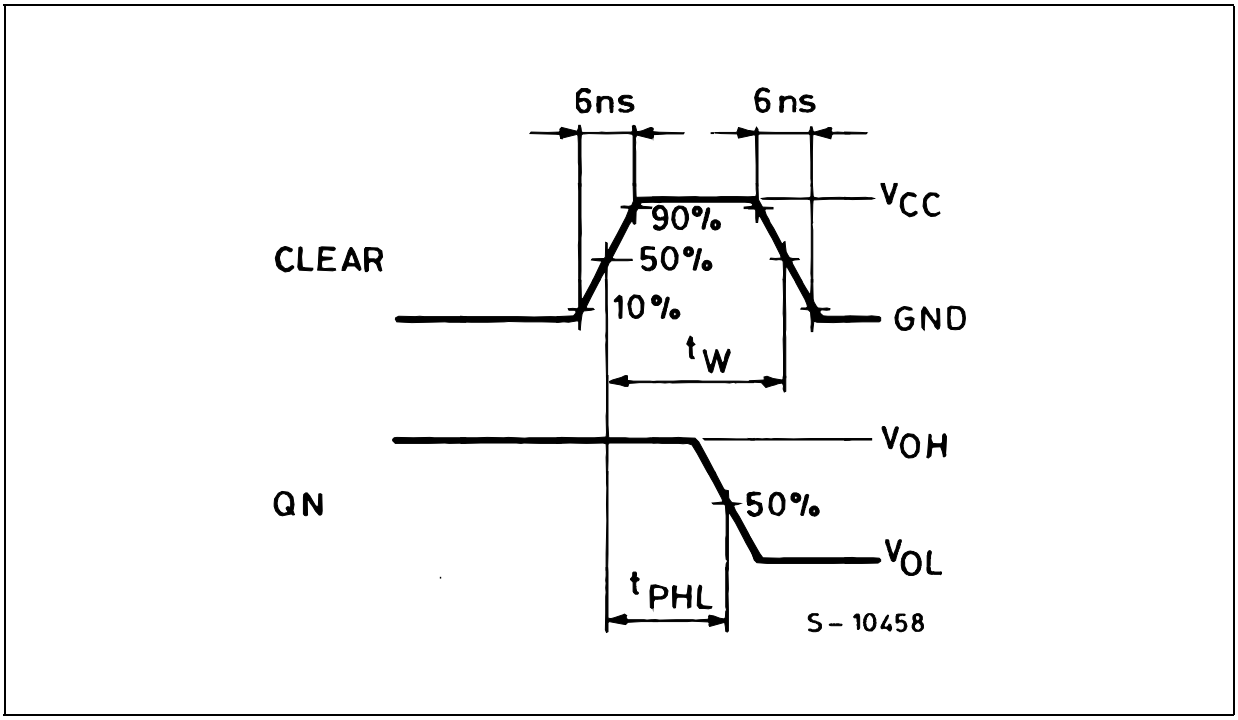


Figure 7: Waveform - Propagation Delay Times (f=1MHz; 50% duty cycle)

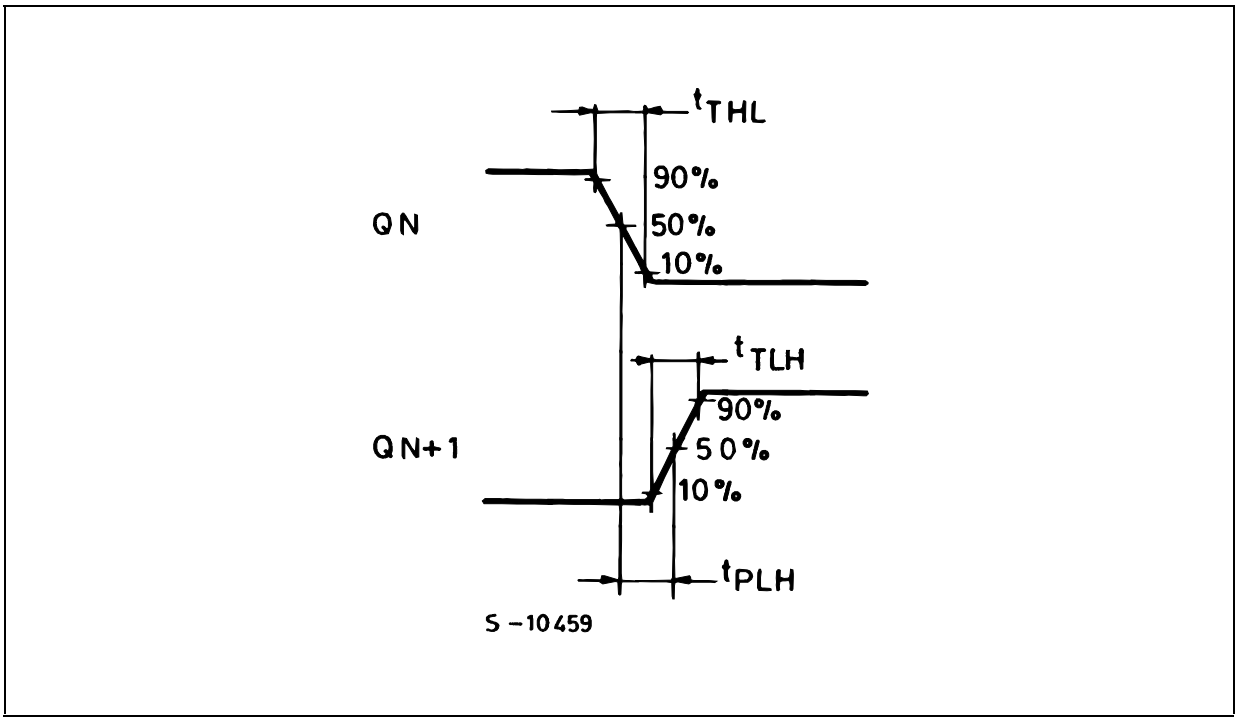


Figure 8: Waveform - Propagation Delay Times (f=1MHz; 50% duty cycle)

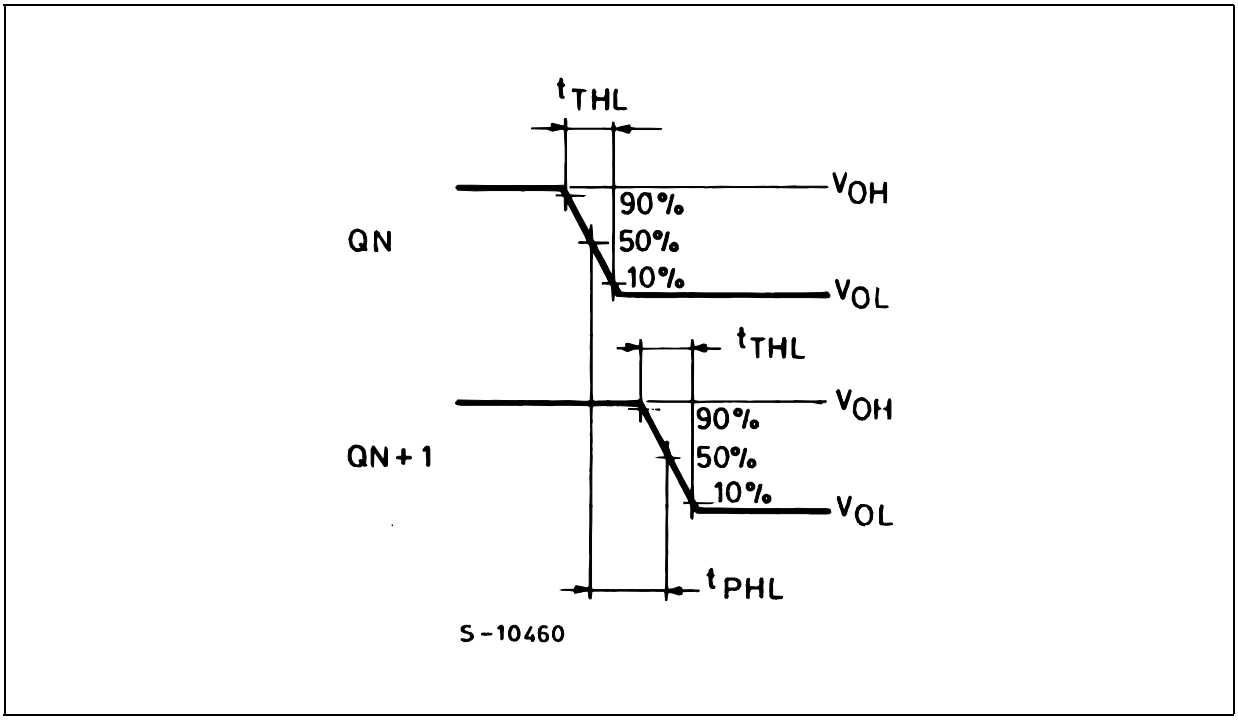
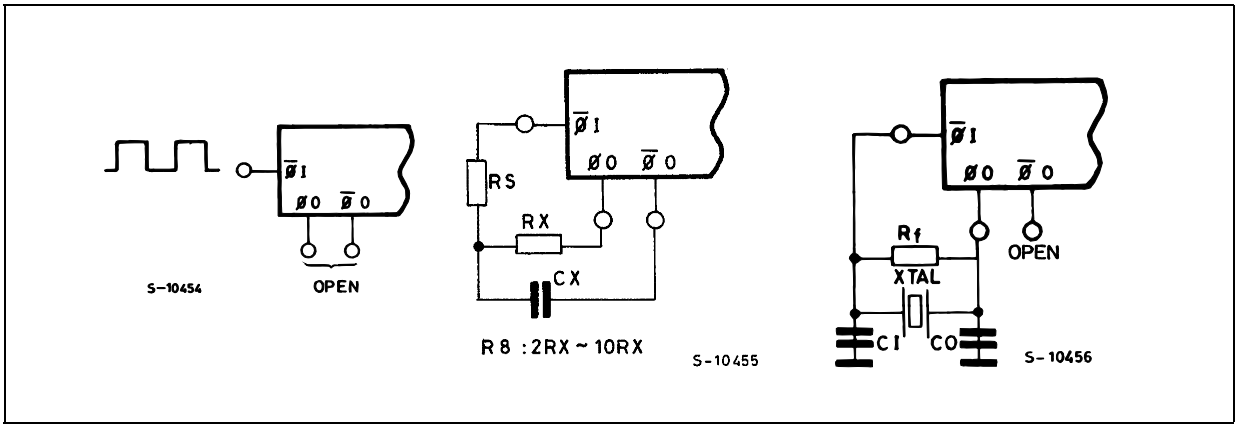
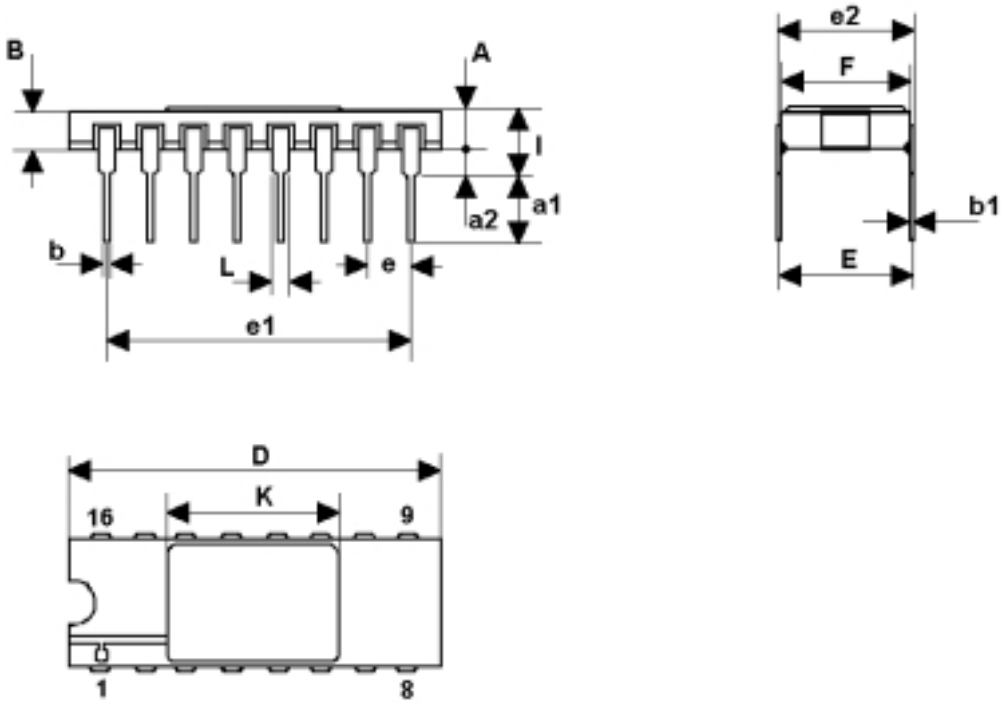


Figure 9: Typical Clock Drive Circuits



DILC-16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	2.1		2.71	0.083		0.107
a1	3.00		3.70	0.118		0.146
a2	0.63	0.88	1.14	0.025	0.035	0.045
B	1.82		2.39	0.072		0.094
b	0.40	0.45	0.50	0.016	0.018	0.020
b1	0.20	0.254	0.30	0.008	0.010	0.012
D	20.06	20.32	20.58	0.790	0.800	0.810
E	7.36	7.62	7.87	0.290	0.300	0.310
e		2.54			0.100	
e1	17.65	17.78	17.90	0.695	0.700	0.705
e2	7.62	7.87	8.12	0.300	0.310	0.320
F	7.29	7.49	7.70	0.287	0.295	0.303
I			3.83			0.151
K	10.90		12.1	0.429		0.476
L	1.14		1.5	0.045		0.059



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FPC-16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	6.75	6.91	7.06	0.266	0.272	0.278
B	9.76	9.94	10.14	0.384	0.392	0.399
C	1.49		1.95	0.059		0.077
D	0.102	0.127	0.152	0.004	0.005	0.006
E	8.76	8.89	9.01	0.345	0.350	0.355
F		1.27			0.050	
G	0.38	0.43	0.48	0.015	0.017	0.019
H	6.0			0.237		
L	18.75		22.0	0.738		0.867
M	0.33	0.38	0.43	0.013	0.015	0.017
N		4.31			0.170	

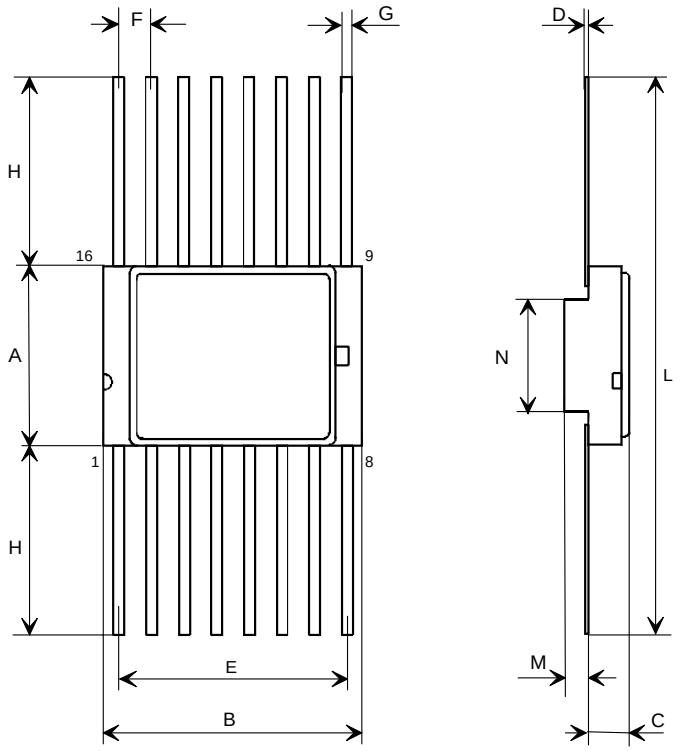

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Table 8: Revision History

Date	Revision	Description of Changes
14-May-2004	1	First Release