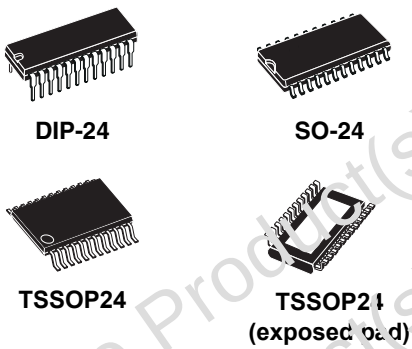
STP16CL596

Low voltage 16-Bit, constant current LED sink driver

Features

- Low voltage power supply down to 3V
- 16 constant current output channels
- Adjustable output current through external resistor
- Serial data IN/parallel data OUT
- Serial OUT changes state on the falling edges of clock
- 3.3V micro driver-able
- Output current: 15-90mA
- 25Mhz clock freqrequency
- available in high thermal efficiency TSSOP exposed pad



Description

The STP16CL596 is a monolithic, medium-voltage, low current power 16-bit shift register designed for LED panel displays.
The device contains a 16-bit serial IN, parallel-OUT shift register that feeds a 16-bit, D-type storage register. In the output stage, sixteen regulated current sources are designed to provide 15-90mA constant current to drive the LEDs.

The serial output change state on the falling edges of clock, this special feature will provide an improved performance of the application when the clock signal is skewed because the daisy chain is too long.

Through an external resistor, users may adjust the STP16CL596 output current, controlling in this way the light intensity of LEDs.

The STP16CL596 guarantees a 16V output driving capability, allowing users to connect more LEDs in series. The high clock frequency, 25MHz, also satisfies the system demand for high volume data transmission, the 3.3V of voltage supply is well useful for applications that interface any micro from 3.3V.

Compared with a standard TSSOP package, the TSSOP exposed pad increases heat dissipation capability by a 2.5 factor.

Order Codes

Part Number	Package	Packaging
STP16CL596B1R	DIP-24	15 parts per tube
STP16CL596M	SO-24 (Tube)	40 parts per tube
STP16CL596MTR	SO-24 (Tape & Reel)	1000 parts per reel
STP16CL596TTR	TSSOP24 (Tape & Reel)	2500 parts per reel
STP16CL596XTTR	TSSOP24 Exposed-Pad (Tape & Reel)	2500 parts per reel

Contents

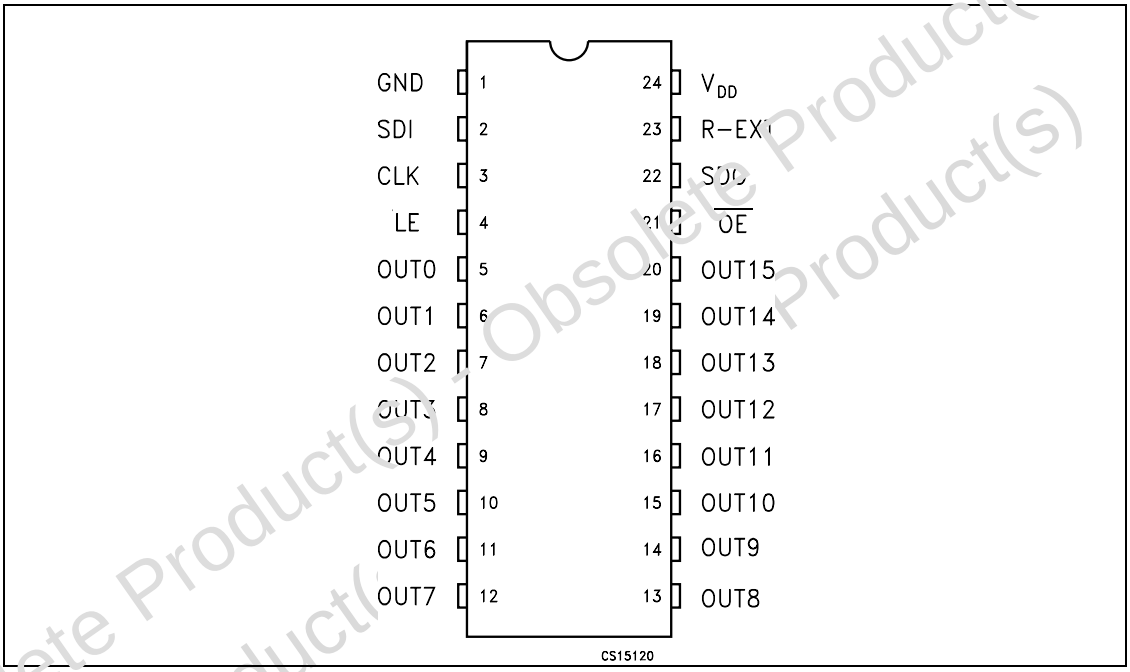
1 Summary description

Table 1. Current accuracy

Output voltage	Current accuracy		Output current
	Between bits	Between ICs	
≥ 0.7V	± 3%	± 10%	15 to 90mA

1.1 Pin connection and description

Figure 1. Connections diagram



Note: The Exposed-Pad is electrically not connected

Table 2. Pin description

PIN N°	Symbol	Name and function
1	GND	Ground terminal
2	SDI	Serial data input terminal
3	CLK	Clock input terminal
4	LE	Latch input terminal
5-20	OUT 0-15	Output terminal
21	$\overline{OE}$	Input terminal of output enable (active low)
22	SDO	Serial data out terminal
23	R-EXT	Input terminal of an external resistor for constant current programing
24	V_{DD}	Supply voltage terminal

2 Equivalent circuit of inputs and outputs

Figure 2. $\overline{OE}$ terminal

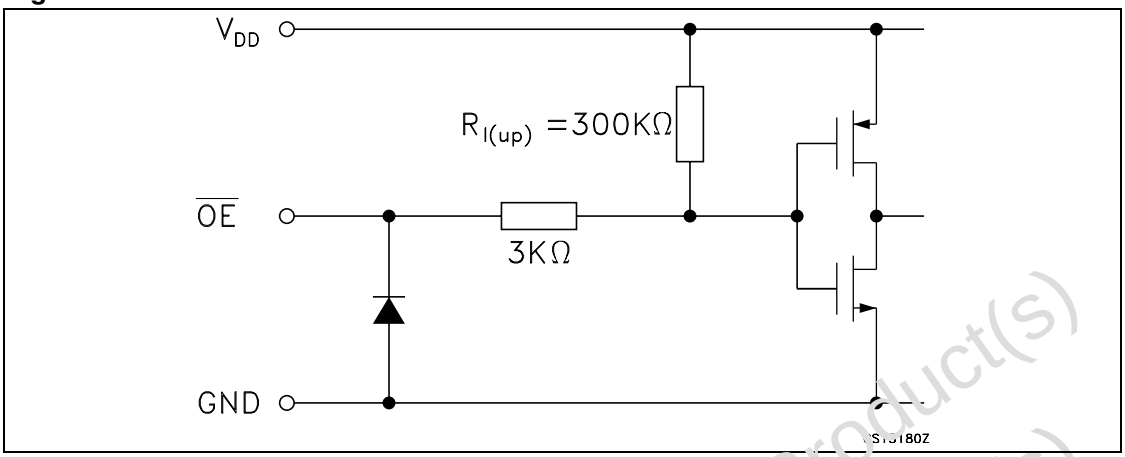


Figure 3. LE terminal

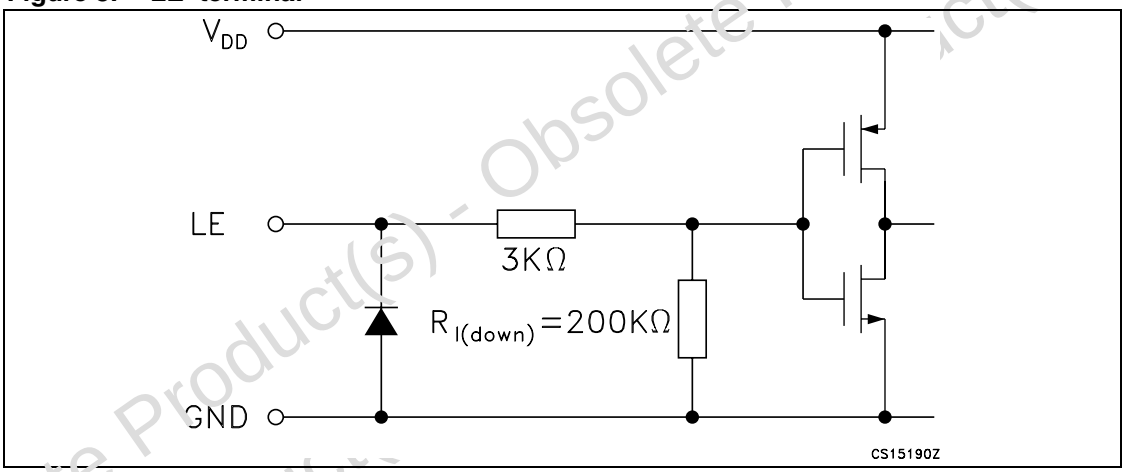


Figure 4. CLK, SDI terminal

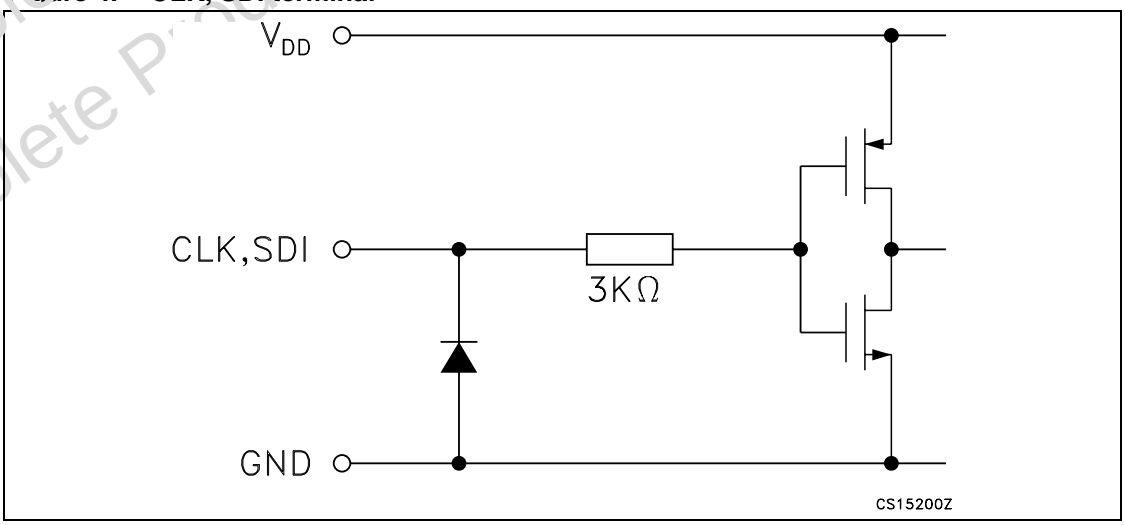


Figure 5. SDO terminal

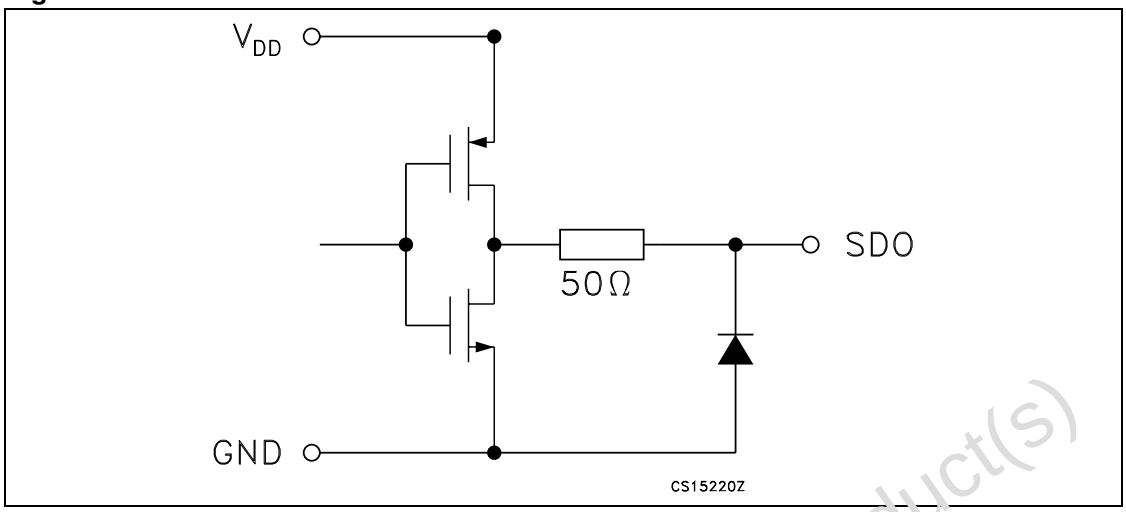
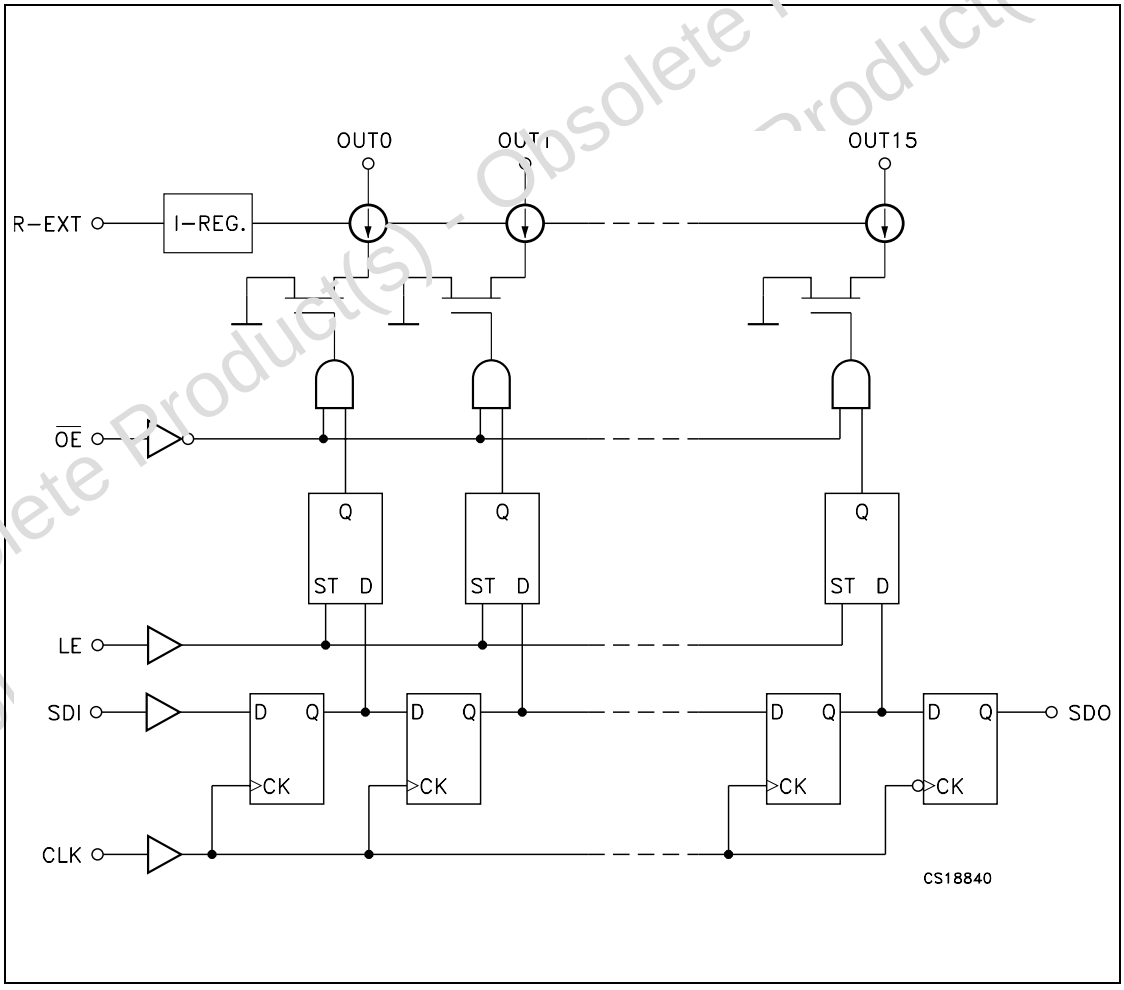


Figure 6. Block diagram - normal mode



2.1 Truth table

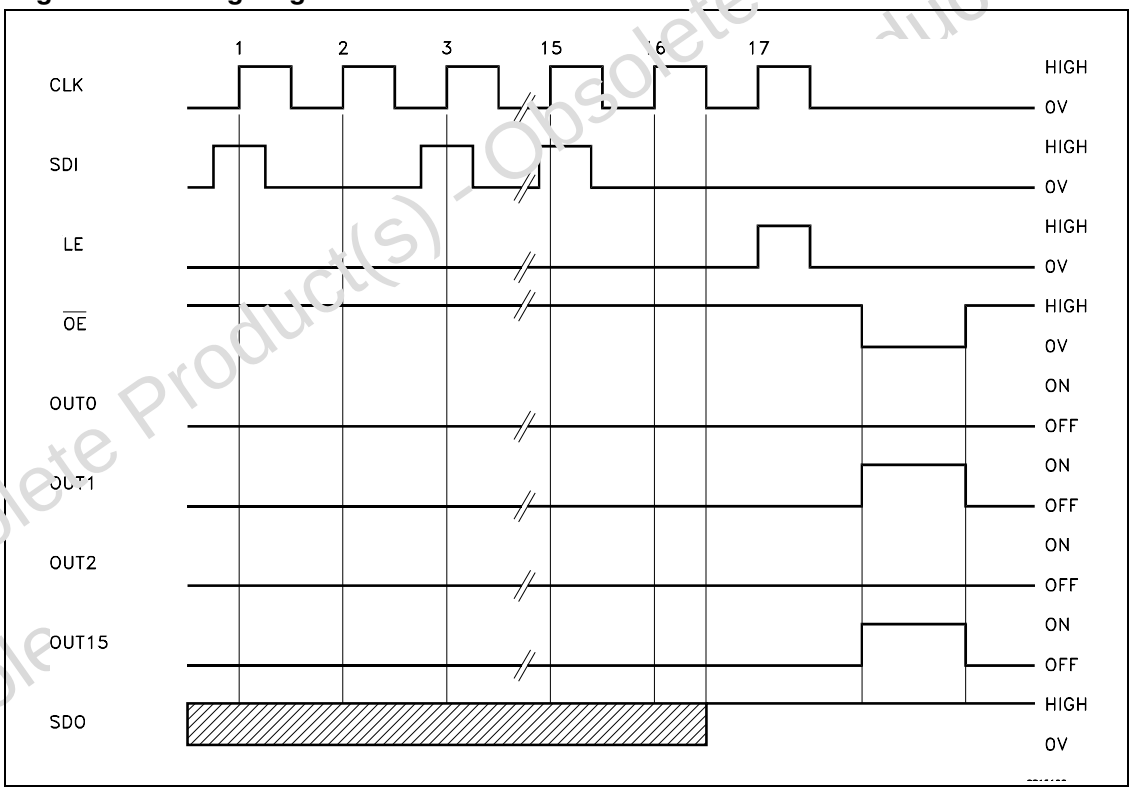
Table 3. Truth table

Clock	LE	$\overline{OE}$	SERIAL-IN	OUT0 ..... OUT7 ..... OUT15	SDO
↑	H	L	Dn	Dn ..... Dn -7 ..... Dn -15	Dn -15
↑	L	L	Dn + 1	No Change	Dn -14
↑	H	L	Dn + 2	Dn -2 ..... Dn -5 ..... Dn -13	Dn -13
↓	X	L	Dn + 3	Dn -2 ..... Dn -5 ..... Dn -13	Dn -13
↓	X	L	Dn + 3	ON	Dn -13

Note: OUT0 to OUT15 = ON when Dn = H; OUT0 to OUT15 = OFF when Dn = L.

2.2 Timing diagram

Figure 7. Timing diagram - normal mode



Note: Note: The latches circuit holds data when the LE terminal is Low.

When the LE terminal is at High level, latch circuit doesn't hold the data it passes from the input to the output.

When the $\overline{OE}$ terminal is at Low level, output terminals OUT0 to OUT15 respond to the data, either ON or OFF.

When the $\overline{OE}$ terminal is at High level, it switches off all the data on the output terminal.

Figure 8. Clock, Serial-In, Serial-Out

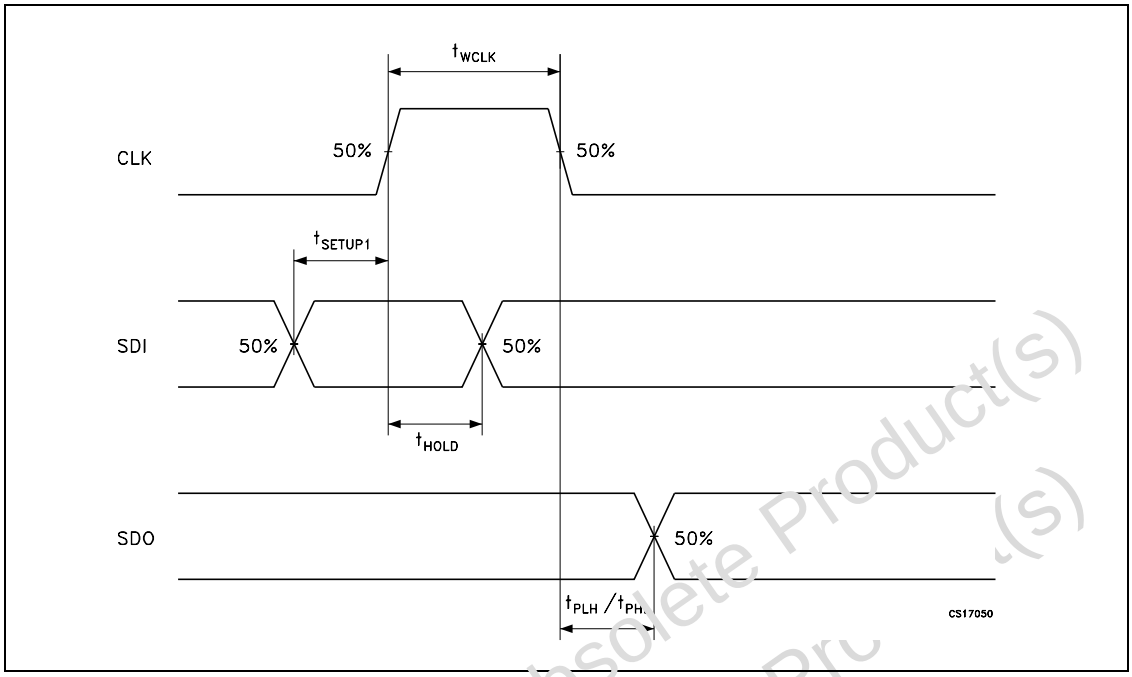


Figure 9. Clock, Serial-In, Latch, Enable Outputs

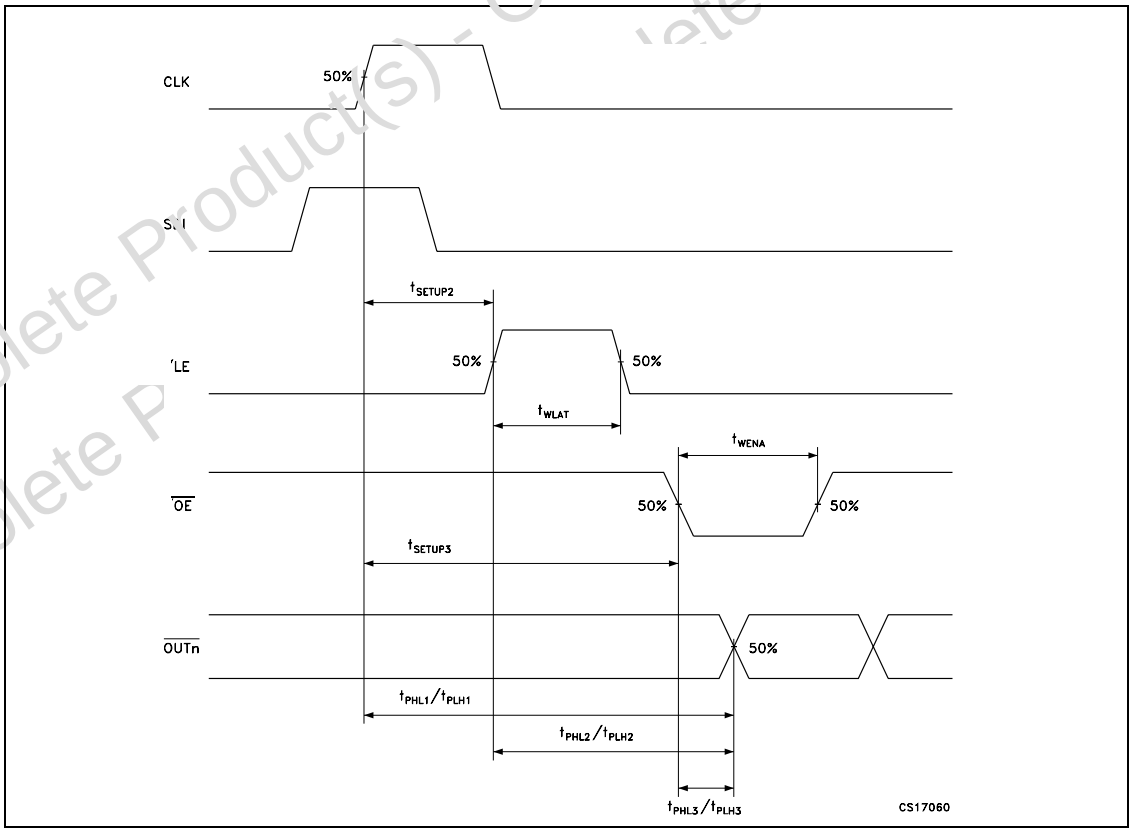
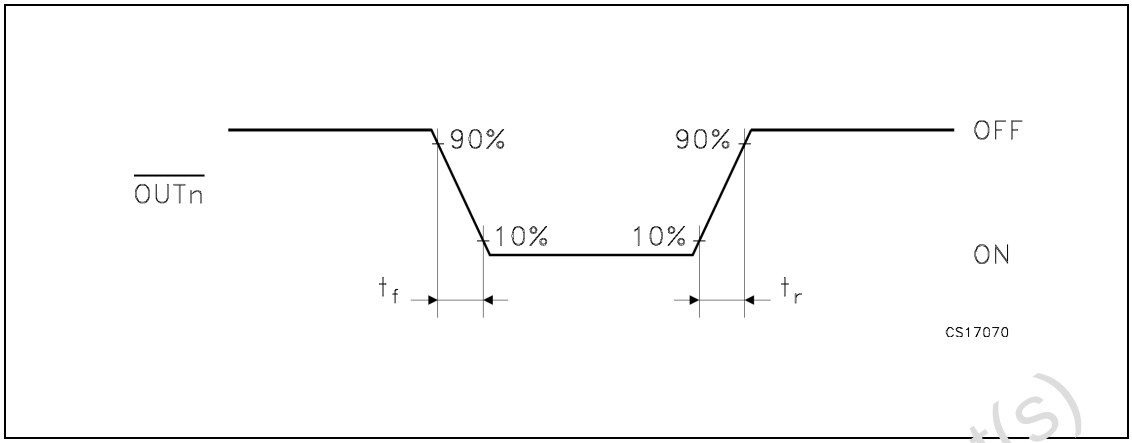


Figure 10. Outputs



3 Maximum rating

Stressing the device above the rating listed in the “Absolute Maximum Ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage	0 to 7	V
V_O	Output voltage	-0.5 to 16	V
I_O	Output current	90	mA
V_I	Input voltage	-0.4 to V_{DD}+0.4	V
I_{GND}	GND terminal current	1440	mA
f_{CLK}	Clock frequency	25	MHz
T_{OPR}	Operating temperature range	-40 to +125	°C
T_{STG}	Storage temperature range	-65 to +150	°C

3.1 Thermal data

Table 5. Thermal data

Symbol	Parameter	DIP-24	SO-24	TSSOP-24	TSSOP-24(1) (exposed pad)	Unit
$R_{th(j-a)}$	Thermal resistance junction-ambient	60	75	85	37.5	°C/W

1. The Exposed-Pad should be soldered to the PBC to realize the thermal benefits

3.2 Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage		3.0	3.3	3.6	V
V_O	Output voltage				16.0	V
I_O	Output current	OUTn	5		90	mA
I_{OH}	Output current	SERIAL-OUT			+1	mA
I_{OL}	Output current	SERIAL-OUT			-1	mA
V_{IH}	Input voltage		$0.7V_{DD}$		V_{DD}	V
V_{IL}	Input voltage		-0.3		$0.3V_{DD}$	V
t_{wLAT}	LE pulse width	V_{DD} = 3.0 to 3.6V	20			ns
t_{wCLK}	CLK pulse width		20			ns
t_{wEN}	$\overline{OE}$ pulse width		400			ns
$t_{SETUP(D)}$	Setup time for DATA		20			ns
$t_{HOLD(D)}$	Hold time for DATA		15			ns
$t_{SETUP(L)}$	Setup time for LATCH		15			ns
f_{CLK}	Clock frequency	Cascade operation (1)			25	MHz

1. If the device is connected in cascade, it may not be possible achieve the maximum data transfer. Please considered the timings carefully.

4 Electrical characteristics

Table 7. Electrical characteristics (V_{DD} = 3.3V, T = 25°C, unless otherwise specified.)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IH}	Input voltage high level		0.7V_{DD}		V_{DD}	V
V_{IL}	Input voltage low level		GND		0.3V_{DD}	V
I_{OH}	Output leakage current	V_{OH} = 16V			10	µA
V_{OL}	Output voltage (Serial-OUT)	I_{OL} = 1mA			0.4	V
V_{OH}	Output voltage (Serial-OUT)	I_{OH} = -1mA	V_{DD}- 0.4V			V
I_{OL1}	Output current	V_O = 0.7V R_{EXT} = 910Ω	19.2	20.3	22.0	mA
I_{OL2}		V_O = 0.7V R_{EXT} = 360Ω	48.2	50.2	54.2	mA
ΔI_{OL1}	Output current error between bit (All Output ON)	V_O = 0.7V R_{EXT} = 910Ω		± 4	± 5	%
ΔI_{OL2}		V_O = 0.7V R_{EXT} = 360Ω		± 3	± 4	%
$R_{SIN(up)}$	Pull-up resistor		150	300	600	KΩ
$R_{SIN(down)}$	Pull-down resistor		100	200	400	KΩ
$I_{DD(OFF1)}$	Supply current (OFF)	R_{EXT} = OPEN OUT 0 to 15 = OFF		0.3	0.6	mA
$I_{DD(OFF2)}$		R_{EXT} = 470Ω OUT 0 to 15 = OFF		5.5	7.7	
$I_{DD(OFF3)}$		R_{EXT} = 250Ω OUT 0 to 15 = OFF		10.1	14.1	
$I_{DD(ON1)}$	Supply current (ON)	R_{EXT} = 470Ω OUT 0 to 15 = ON		5.5	7.7	
$I_{DD(ON2)}$		R_{EXT} = 250Ω OUT 0 to 15 = ON		10.1	14.1	

5 Switching characteristics

Table 8. Switching characteristics (V_{DD} = 3.3V, T = 25°C, unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{PLH1}	Propagation delay time, CLK-$\overline{OUT}$n, LE = H, $\overline{OE}$ = L	V_{DD} = 3.3V, V_{IH} = V_{DD}, V_{IL} = GND, C_L = 13pF, I_O = 40mA, V_L = 3V, R_{EXT} = 470Ω, R_L = 65Ω		250	280	ns
t_{PLH2}	Propagation delay time, LE-$\overline{OUT}$n, $\overline{OE}$ = L			220	250	ns
t_{PLH3}	Propagation delay time, $\overline{OE}$-$\overline{OUT}$n, LE = H			200	250	ns
t_{PLH}	Propagation delay time, CLK-SDO			25	50	ns
t_{PHL1}	Propagation delay time, CLK-$\overline{OUT}$n, LE = H, $\overline{OE}$ = L			25	50	ns
t_{PHL2}	Propagation delay time, LE-$\overline{OUT}$n, $\overline{OE}$ = L			25	50	ns
t_{PHL3}	Propagation delay time, $\overline{OE}$-$\overline{OUT}$n, LE = H			50	70	ns
t_{PHL}	Propagation delay time, CLK-SDO			25	50	ns
t_r	Output rise time			200	250	ns
t_f	Output fall time			17	25	ns

Note: 1 To prevent current overshoct, during the Outputs switching, the overhead output voltage must be less than 1V

2 The Maximum suggested swithching frequency is up tp 10KHz

6 Test circuit

Figure 11. DC characteristics

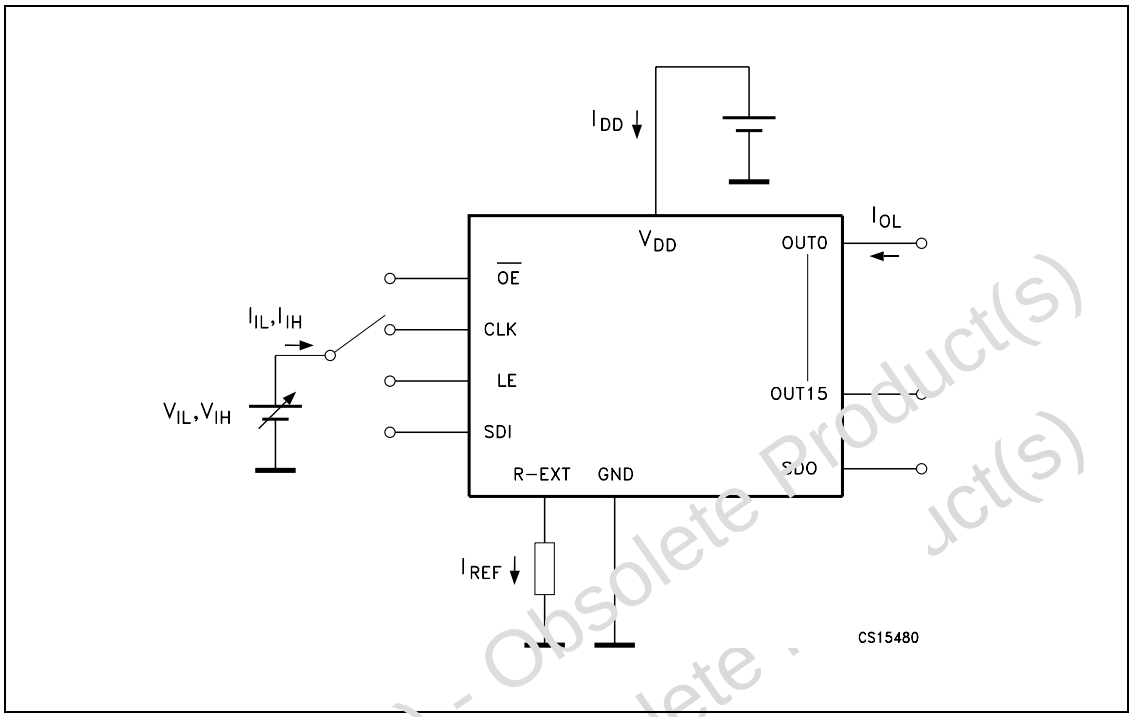
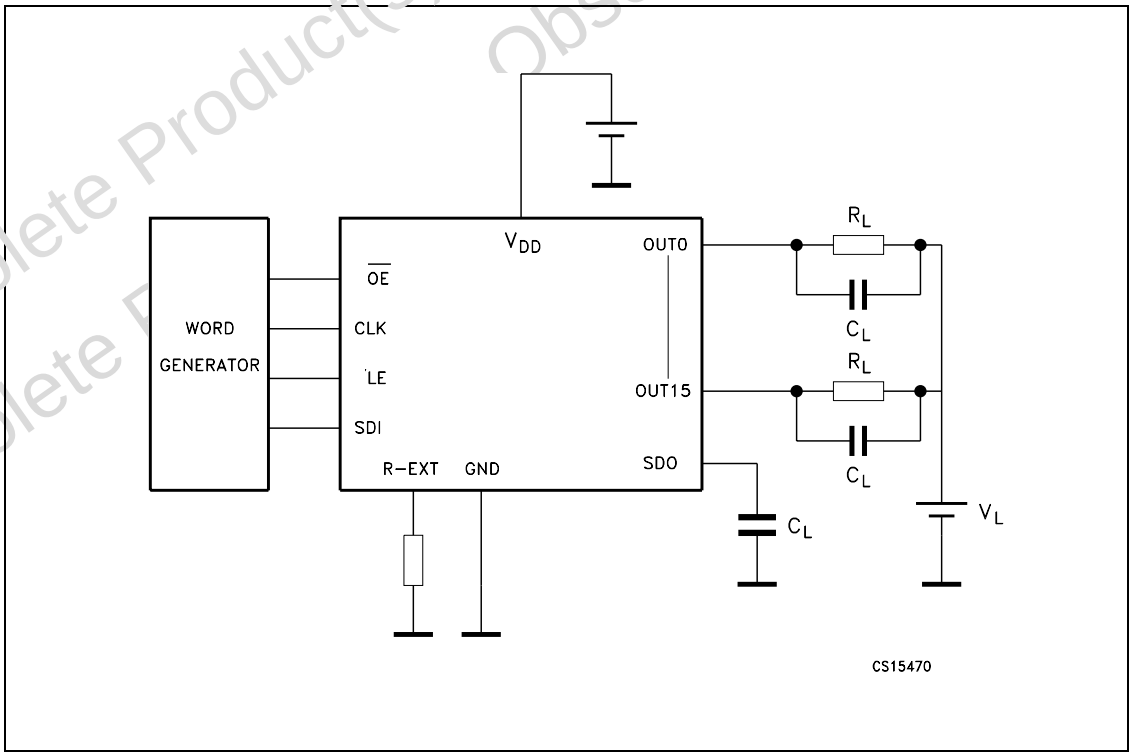


Figure 12. AC characterist cs



7 Typical characteristics

Figure 13. Output current-REXT resistor

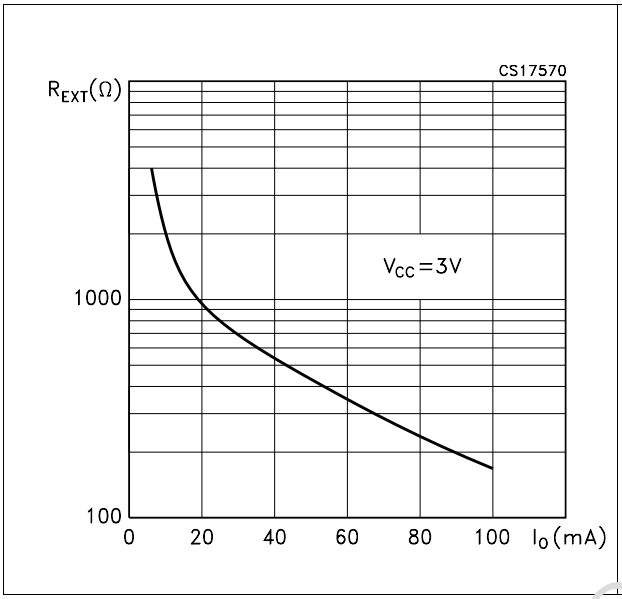


Figure 14. Power dissipation vs temperature package

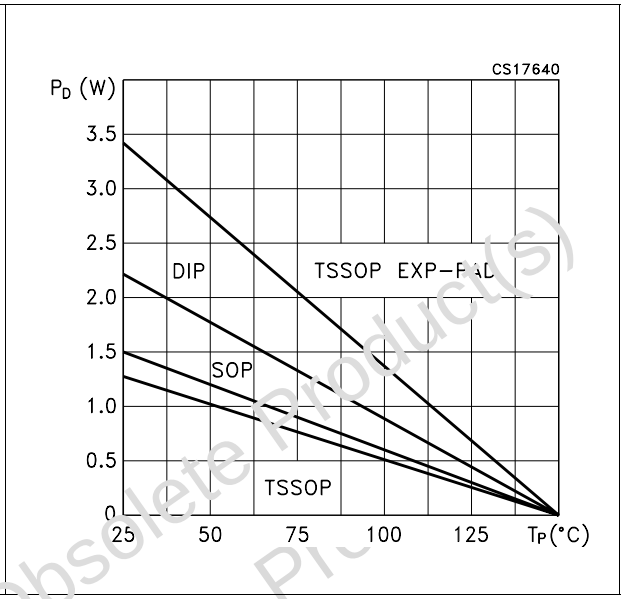


Figure 15. Output current vs drop voltage

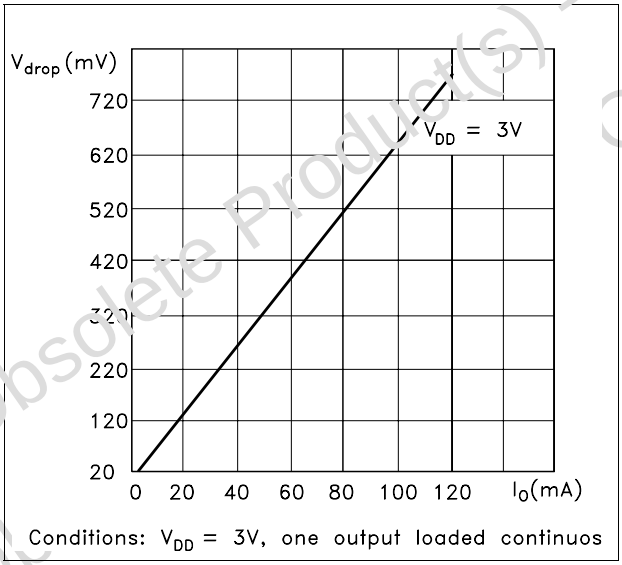
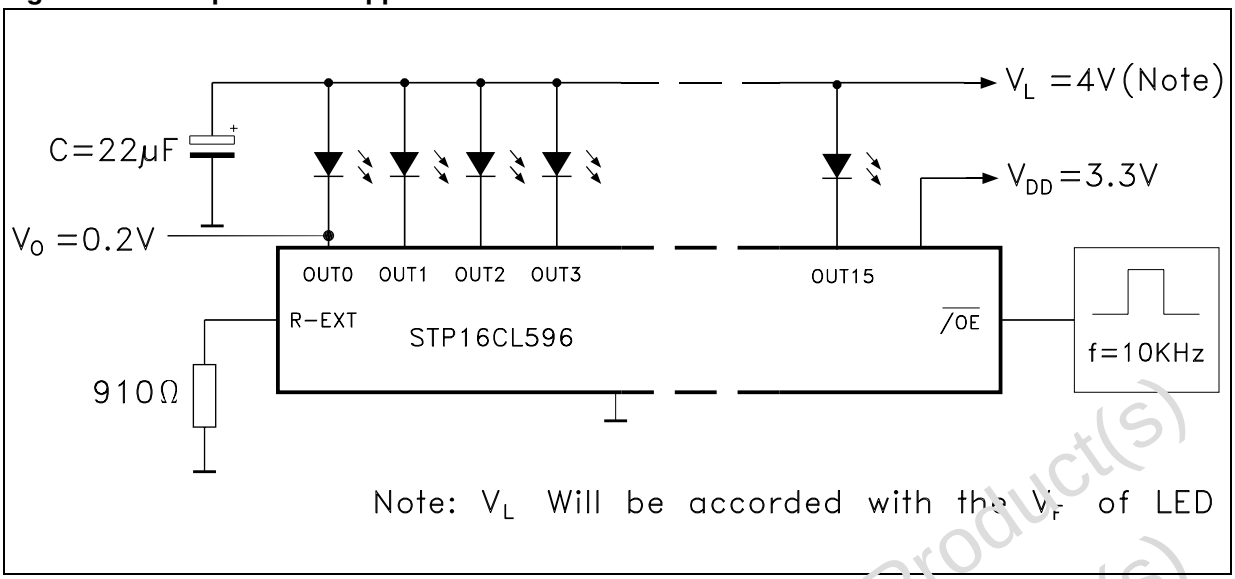


Figure 16. Blue powerLED application circuit



8 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Table 9. Plastic DIP-24 (0.25) mechanical data

Ref	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A			4.32			0.170
A1	0.38			0.015		
A2		3.3			0.130	
B	0.41	0.46	0.51	0.016	0.018	0.020
B1	1.40	1.52	1.65	0.055	0.060	0.065
c	0.20	0.25	0.30	0.008	0.010	0.012
D	31.62	31.75	31.88	1.245	1.250	1.255
E	7.62		8.26	0.300		0.325
E1	6.35	6.60	6.86	0.250	0.260	0.270
e		2.54			0.100	
E1		7.62			0.300	
L	3.18		3.43	0.125		0.135
M	0°		15°	0°		15°

Figure 17. Plastic DIP-24 (0.25) Package dimensions

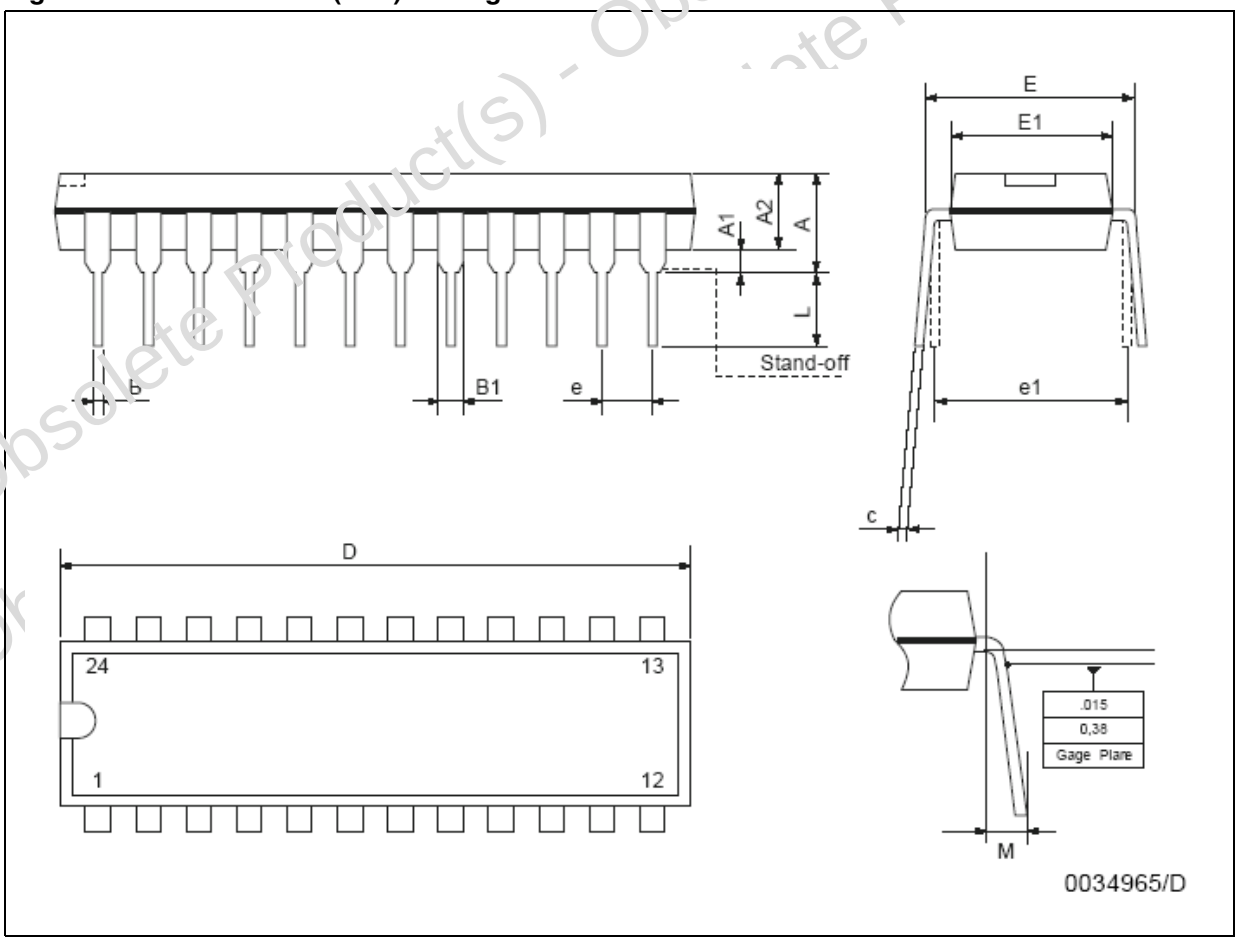


Table 10. TSSOP24 Mechanical data

Ref	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A			1.1			0.043
A1	0.05		0.15	0.002		0.006
A2		0.9			0.035	
b	0.19		0.30	0.0075		0.0118
c	0.09		0.20	0.0035		0.0079
D	7.7		7.9	0.303		0.311
E	4.3		4.5	0.169		0.177
e		0.65 BSC			0.0256 BSC	
H	6.25		6.5	0.246		0.256
K	0°		8°	0°		8°
L	0.50		0.70	0.020		0.028

Figure 18. TSSOP24 Package dimensions

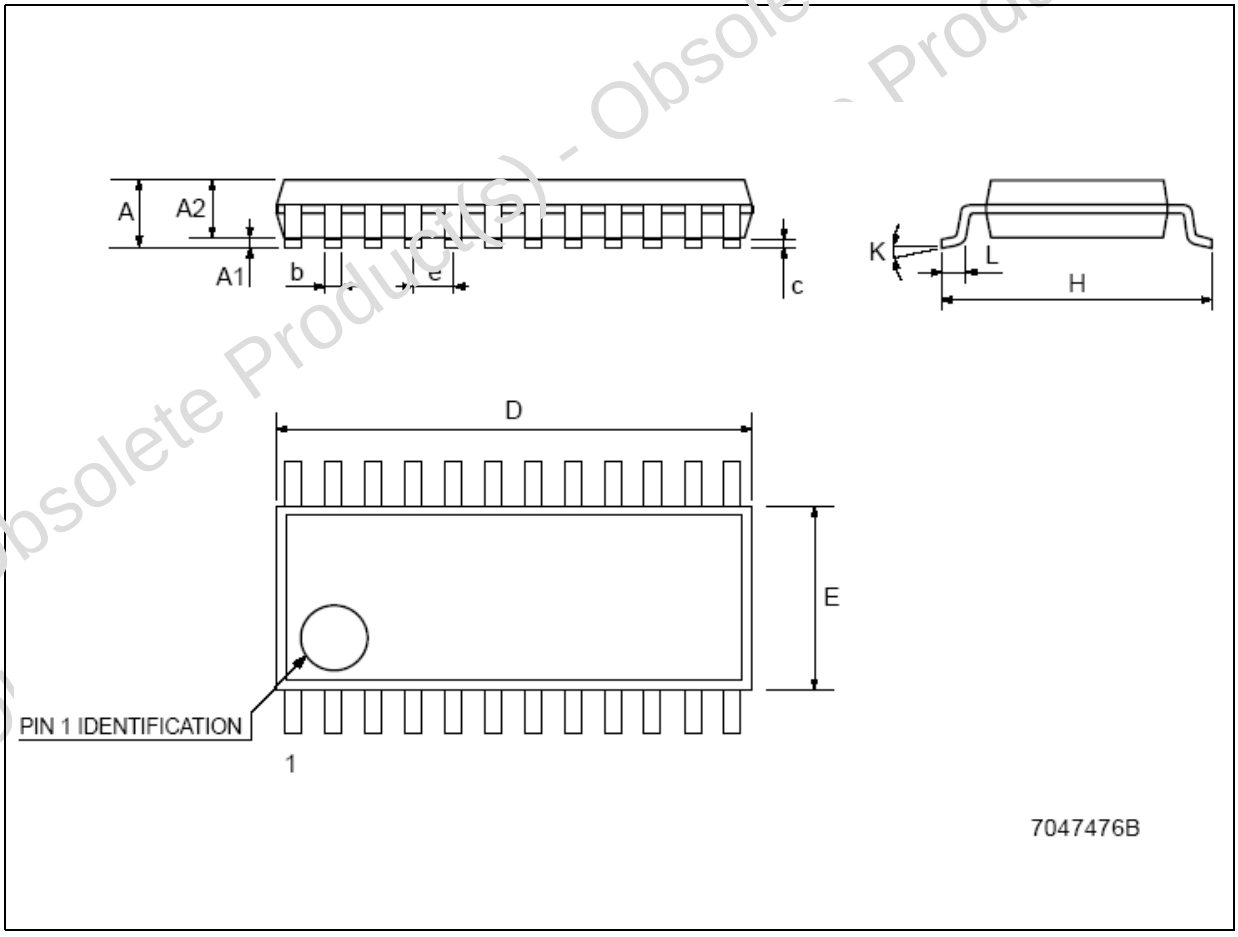


Table 11. Tape & Reel TSSOP24

Ref	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	6.8		7	0.268		0.276
Bo	8.2		8.4	0.323		0.331
Ko	1.7		1.9	0.067		0.075
Po	3.9		4.1	0.153		0.161
P	11.9		12.1	0.468		0.476

Figure 19. Reel dimensions

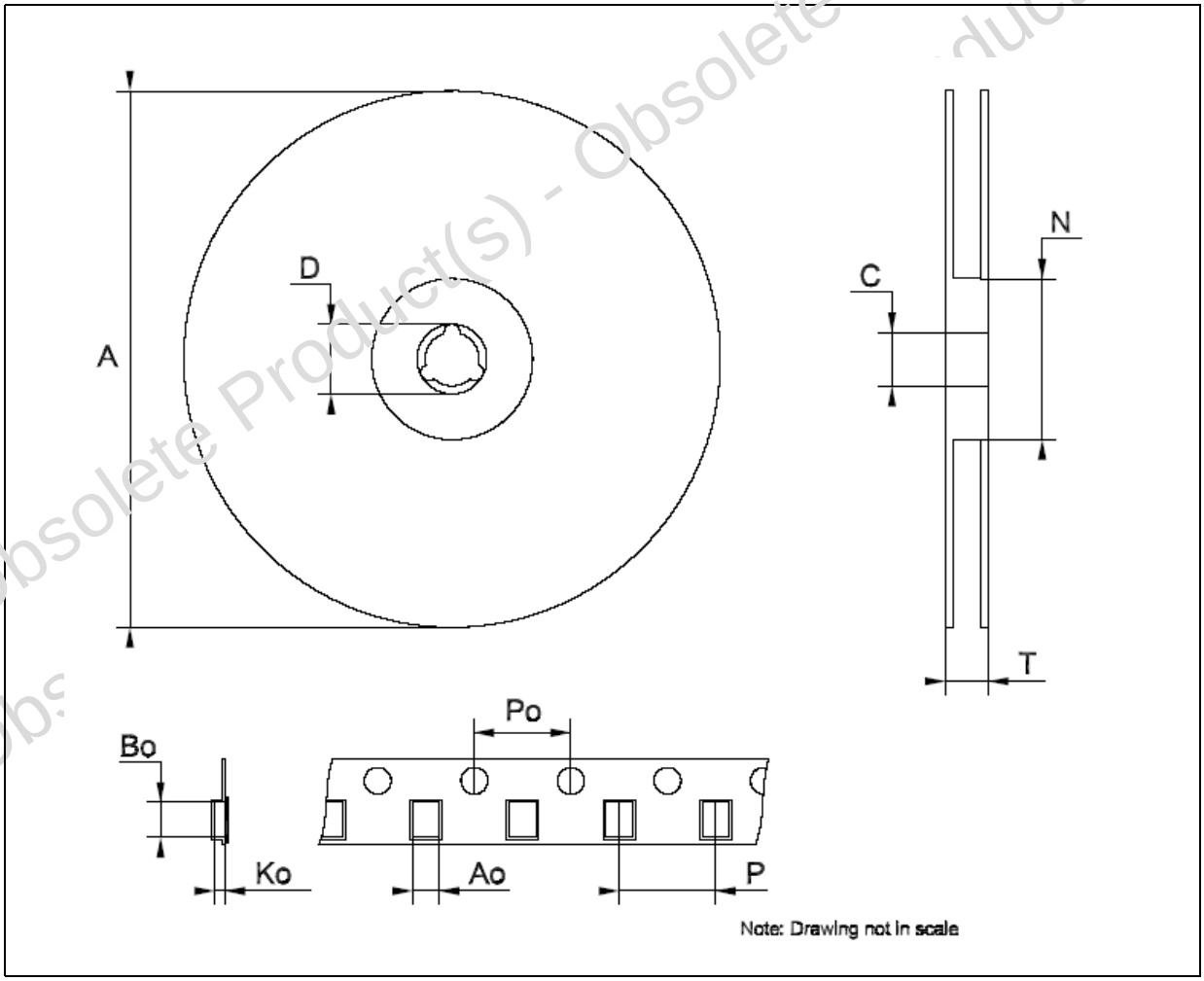


Table 12. SO-24 Mechanical Data

Ref	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A			2.65			0.104
a1	0.1		0.2	0.004		0.008
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.012
C		0.5			0.020	
c1	45°(typ.)					
D	15.20		15.60	0.598		0.614
E	10.00		10.65	0.393		0.419
e		1.27			0.050	
e3		13.97			0.550	
F	7.40		7.60	0.291		0.300
L	0.50		1.27	0.020		0.050
S	°(max.) 8					

Figure 20. SO-24 Package dimensions

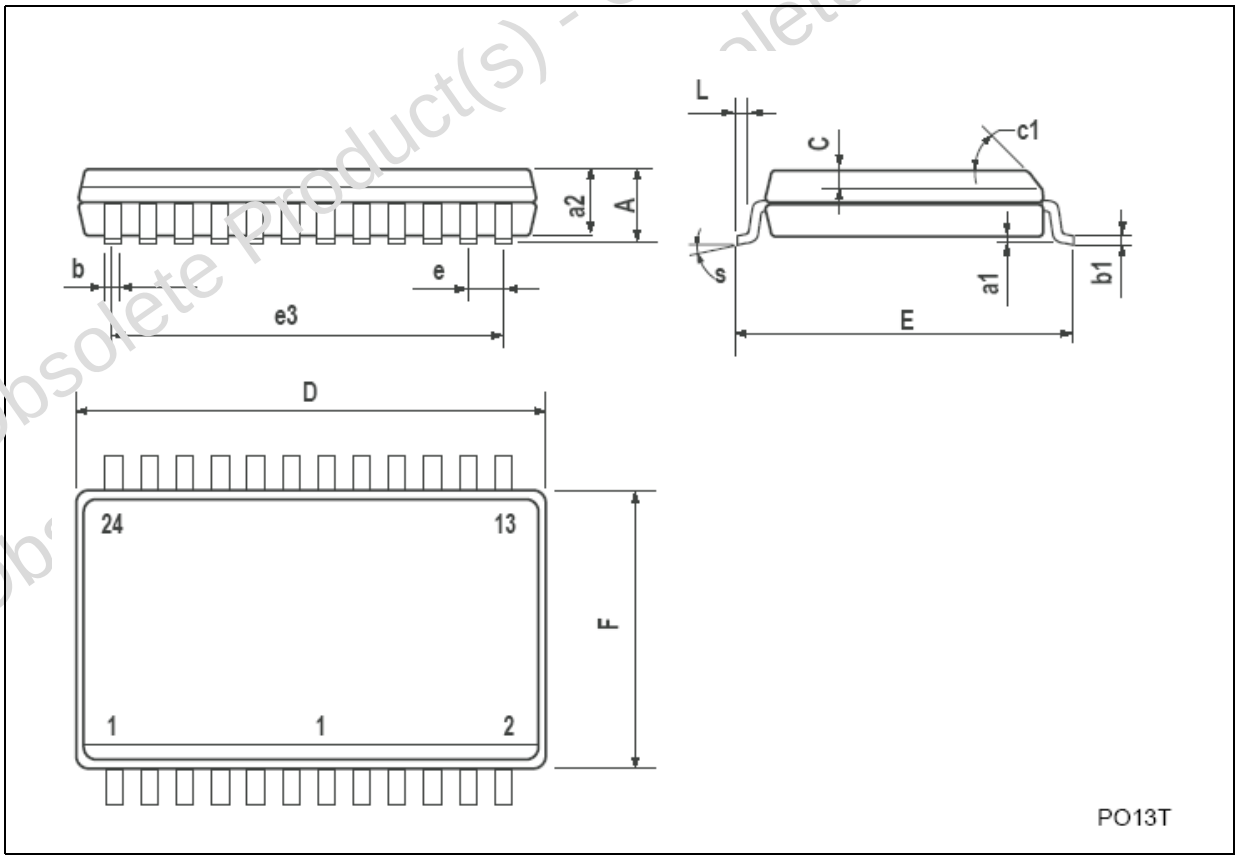


Table 13. Tape & Reel SO-24

Ref	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			30.4			1.197
Ao	10.8		11.0	0.425		0.433
Bo	15.7		15.9	0.618		0.626
Ko	2.9		3.1	0.114		0.122
Po	3.9		4.1	0.153		0.161
P	11.9		12.1	0.468		0.476

Figure 21. Reel dimensions

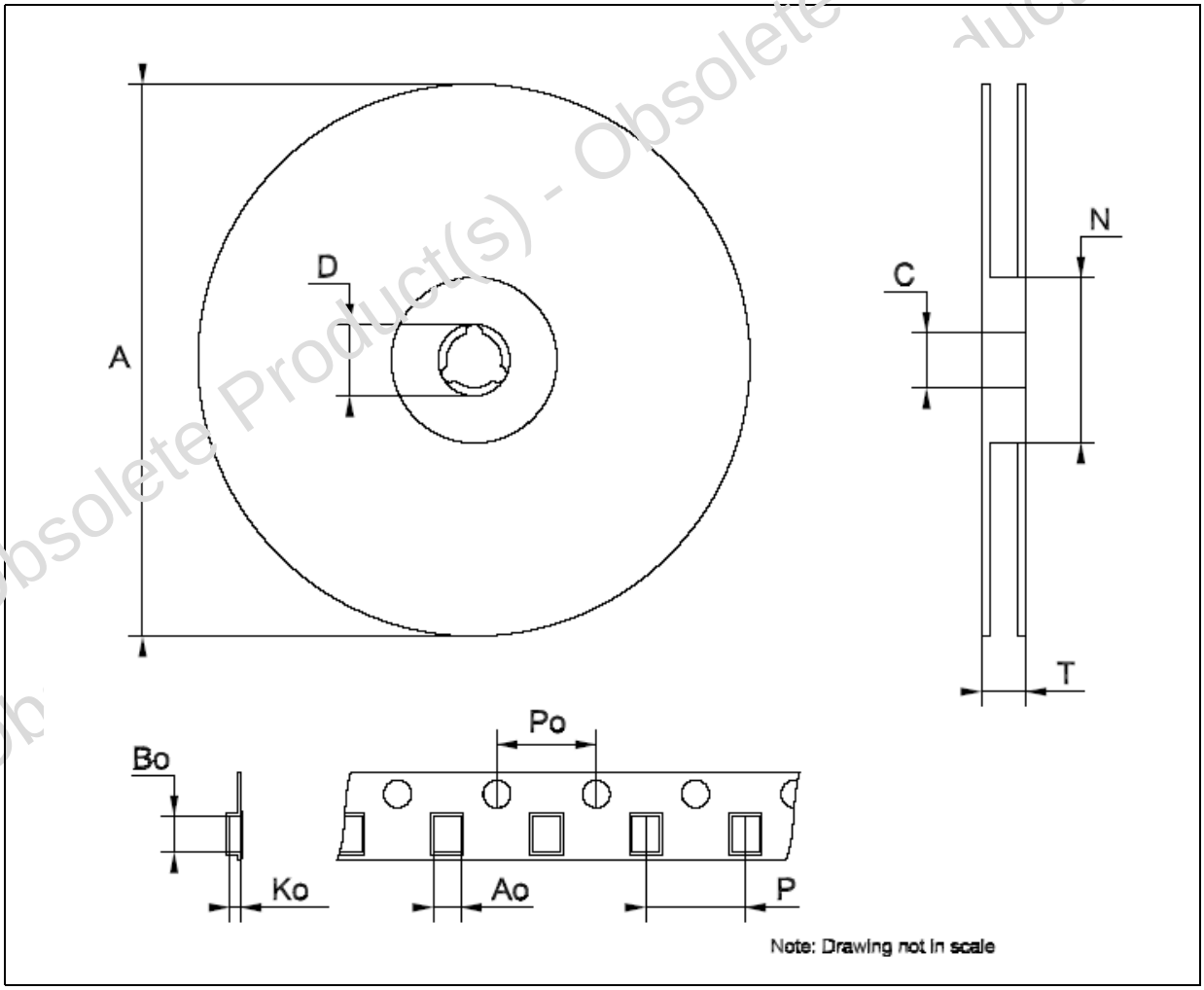
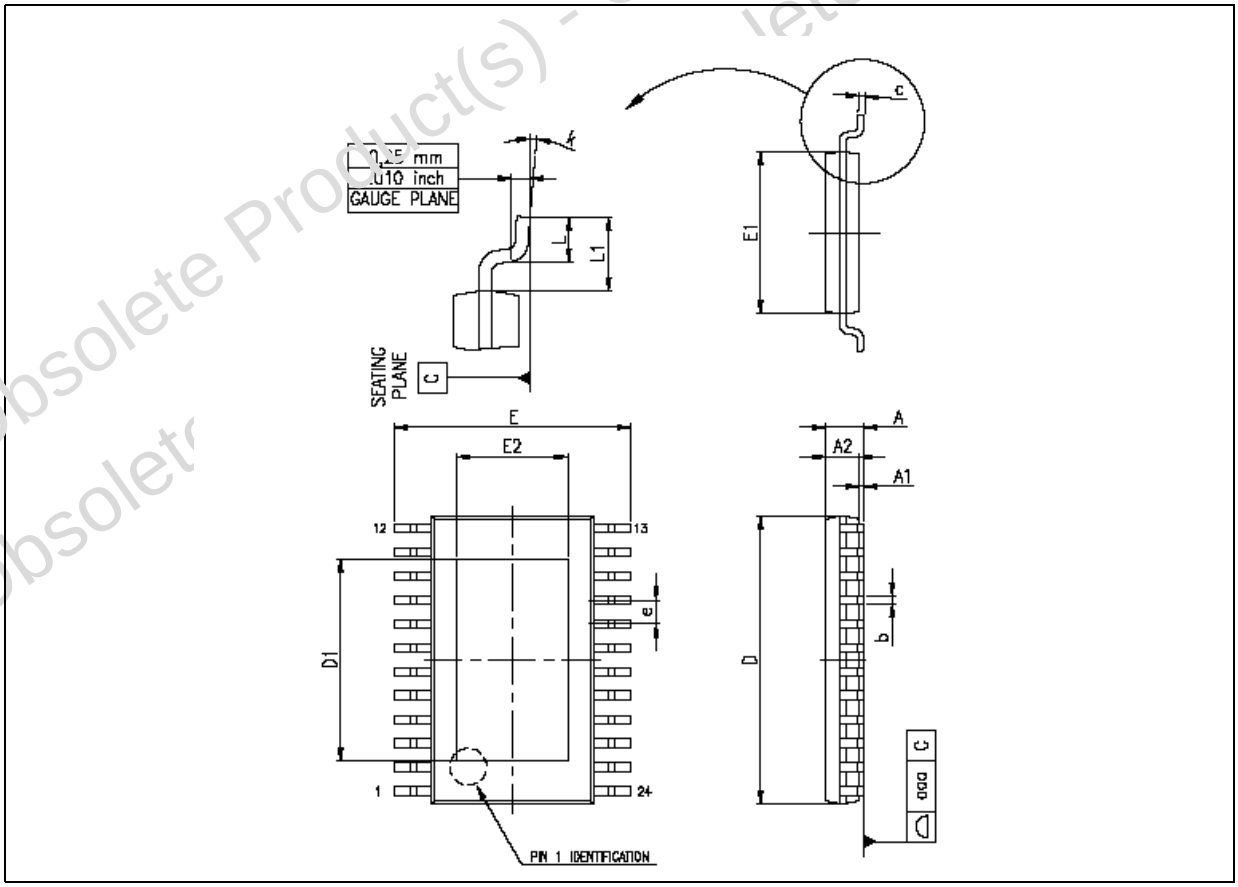


Table 14. TSSOP24 Exposed-pad

Ref	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A			1.2			0.047
A1			0.15		0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	7.7	7.8	7.9	0.303	0.307	0.311
D1		2.7		0.106		
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.5	0.169	0.173	0.177
E2		1.5		0.059		
e		0.65			0.0256	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030

Figure 22. TSSOP24 dimensions



9 Revision history

Table 15. Revision history

Date	Revision	Change
06-May-2004	4	Table 6 and Table 7 parameters changed
03-Aug-2004	5	Figure 14 - pag. 10 is changed.
31-Mar-2005	6	Mistake on Fig. 7.
02-May-2005	7	Typing Error on the description features.
22-Jul-2005	8	Add note on Fig. 1 and Table 5.
16-May-2006	9	New template, few updates
26-Jul-2006	10	Block diagram *Figure 6 on page 5* and *Section 2: Equivalent circuit of inputs and outputs on page 4*

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