**Product data sheet** 

## 1. General description

P-channel enhancement mode Field-Effect Transistor (FET) in an MLPAK33 (SOT8002) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

### 2. Features and benefits

- Logic-level compatible
- Trench MOSFET technology
- MLPAK33 package (3.3 x 3.3 mm footprint)

# 3. Applications

- · High-side load switch
- · Battery management
- DC-to-DC conversion
- Switching circuits

### 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
$V_{DS}$	drain-source voltage	T <sub>j</sub> = 25 °C		-	-	-30	V
$V_{GS}$	gate-source voltage			-25	-	25	V
I <sub>D</sub>	drain current	V <sub>GS</sub> = -10 V; T <sub>amb</sub> = 25 °C; t ≤ 5 s	[1]	-	-	-15.2	Α
Static characteristics							
R <sub>DSon</sub>	rociotopoo	$V_{GS} = -10 \text{ V}; I_D = -9 \text{ A}; T_j = 25 \text{ °C}$		-	11.1	12.8	mΩ
		$V_{GS} = -4.5 \text{ V}; I_D = -7.6 \text{ A}; T_j = 25 ^{\circ}\text{C}$		-	14.5	17.7	mΩ

<sup>[1]</sup> Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 6 cm<sup>2</sup>.



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# 5. Pinning information

#### **Table 2. Pinning information**

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	1 2 3 4	
2	S	source		
3	S	source		D
4	G	gate	]	
5	D	drain		
6	D	drain	المممكا	\$ 017aaa257
7	D	drain	8 7 6 5	
8	D	drain	MLPAK33 (SOT8002-1)	

# 6. Ordering information

### **Table 3. Ordering information**

Type number	Package							
	Name	Description	Version					
PXP012-30QL		plastic thermal enhanced surface mounted package; mini leads; 8 terminals; pitch 0.65 mm; 3.3 x 3.3 x 0.8 mm body	SOT8002-1					

# 7. Marking

#### Table 4. Marking codes

Type number	Marking code
PXP012-30QL	9AU

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# 8. Limiting values

#### Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V <sub>DS</sub>	drain-source voltage	T <sub>j</sub> = 25 °C		-	-30	V
V <sub>GS</sub>	gate-source voltage			-25	25	V
I <sub>D</sub>	drain current	V <sub>GS</sub> = -10 V; T <sub>amb</sub> = 25 °C; t ≤ 5 s	[1]	-	-15.2	Α
		V <sub>GS</sub> = -10 V; T <sub>amb</sub> = 25 °C	[1]	-	-8.9	Α
		V <sub>GS</sub> = -10 V; T <sub>amb</sub> = 100 °C	[1]	-	-5.7	Α
		V <sub>GS</sub> = -10 V; T <sub>sp</sub> = 25 °C		-	-38.8	Α
I <sub>DM</sub>	peak drain current	$T_{amb}$ = 25 °C; single pulse; $t_p \le 10 \mu s$		-	-62.9	Α
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = 25 °C; t ≤ 5 s	[1]	-	4.8	W
		T <sub>amb</sub> = 25 °C	[1]	-	1.7	W
		T <sub>sp</sub> = 25 °C		-	32	W
Tj	junction temperature			-55	150	°C
T <sub>amb</sub>	ambient temperature			-55	150	°C
T <sub>stg</sub>	storage temperature			-65	150	°C
Source-drai	n diode		'	'	'	,
I <sub>S</sub>	source current	T <sub>amb</sub> = 25 °C	[1]	-	-1.7	Α

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 6 cm<sup>2</sup>.

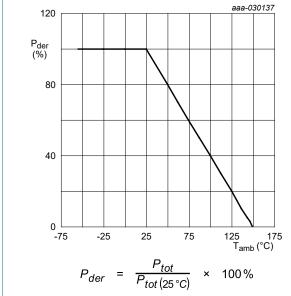


Fig. 1. Normalized total power dissipation as a function of ambient temperature

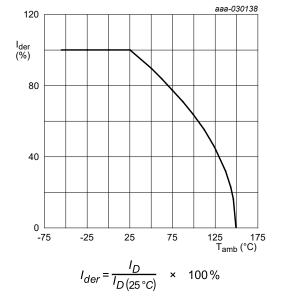


Fig. 2. Normalized continuous drain current as a function of ambient temperature

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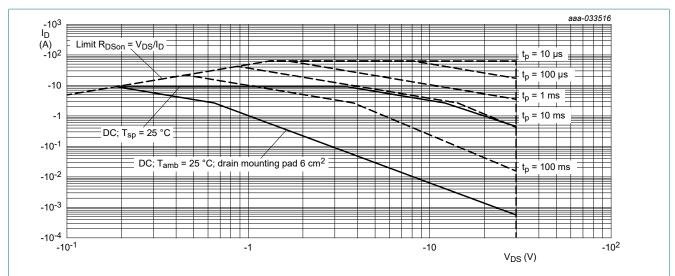


Fig. 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drainsource voltage

### 9. Thermal characteristics

**Table 6. Thermal characteristics** 

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
R <sub>th(j-a)</sub>	thermal resistance from	in free air [	[1]	-	150	190	K/W
	junction to ambient		[2]	-	60	75	K/W
		in free air; t ≤ 5 s	[2]	-	21	26	K/W
R <sub>th(j-sp)</sub>	thermal resistance from junction to solder point			-	2.5	4	K/W

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 6 cm<sup>2</sup>.

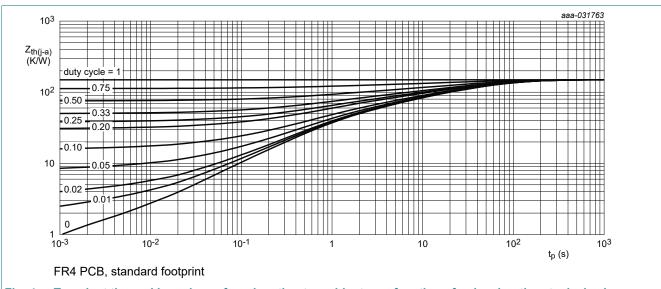
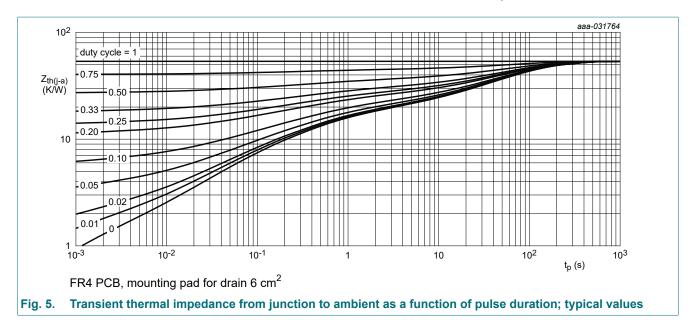


Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

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# 10. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	ecteristics					
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	$I_D$ = -250 $\mu$ A; $V_{GS}$ = 0 V; $T_j$ = 25 °C	-30	-	-	V
$V_{GSth}$	gate-source threshold voltage	$I_D$ = -250 $\mu$ A; $V_{DS}$ = $V_{GS}$ ; $T_j$ = 25 °C	-1	-1.5	-2	V
I <sub>DSS</sub>	drain leakage current	V <sub>DS</sub> = -30 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	-	-1	μA
I <sub>GSS</sub>	gate leakage current	V <sub>GS</sub> = -20 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	-	-100	nA
		V <sub>GS</sub> = 20 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	-	100	nA
R <sub>DSon</sub>	drain-source on-state	$V_{GS} = -10 \text{ V}; I_D = -9 \text{ A}; T_j = 25 ^{\circ}\text{C}$	-	11.1	12.8	mΩ
	resistance	V <sub>GS</sub> = -10 V; I <sub>D</sub> = -9 A; T <sub>j</sub> = 150 °C	-	18	20.7	mΩ
		$V_{GS} = -4.5 \text{ V}; I_D = -7.6 \text{ A}; T_j = 25 \text{ °C}$	-	14.5	17.7	mΩ
9 <sub>fs</sub>	forward transconductance	$V_{DS}$ = -10 V; $I_D$ = -9 A; $T_j$ = 25 °C	-	25	-	S
R <sub>G</sub>	gate resistance	f = 1 MHz	-	20.3	-	Ω
Dynamic ch	aracteristics					
Q <sub>G(tot)</sub>	total gate charge	$V_{DS}$ = -15 V; $I_{D}$ = -9 A; $V_{GS}$ = -10 V; $T_{j}$ = 25 °C	-	28.9	43.4	nC
		V <sub>DS</sub> = -15 V; I <sub>D</sub> = -7.6 A; V <sub>GS</sub> = -4.5 V;	-	14.1	21.2	nC
Q <sub>GS</sub>	gate-source charge	T <sub>j</sub> = 25 °C	-	3.3	-	nC
Q <sub>GS(th)</sub>	pre-threshold gate- source charge		-	2.1	-	nC
Q <sub>GS(th-pl)</sub>	post-threshold gate- source charge		-	1.2	-	nC
Q <sub>GD</sub>	gate-drain charge		-	5.3	-	nC
$V_{GSpl}$	gate-source plateau voltage	$V_{DS} = -15 \text{ V}; I_D = -7.6 \text{ A}; T_j = 25 \text{ °C}$	-	-2.4	-	V
C <sub>iss</sub>	input capacitance	V <sub>DS</sub> = -15 V; f = 1 MHz; V <sub>GS</sub> = 0 V;	-	1400	-	pF
C <sub>oss</sub>	output capacitance	T <sub>j</sub> = 25 °C	-	170	-	pF
C <sub>rss</sub>	reverse transfer capacitance		-	140	-	pF
t <sub>d(on)</sub>	turn-on delay time	$V_{DS}$ = -15 V; $I_D$ = -7.6 A; $V_{GS}$ = -4.5 V;	-	4	-	ns
t <sub>r</sub>	rise time	$R_{G(ext)} = 5 \Omega; T_j = 25 ^{\circ}C$	-	27	-	ns
t <sub>d(off)</sub>	turn-off delay time	1	-	68	-	ns
t <sub>f</sub>	fall time	1	-	55	-	ns
Source-drai	n diode		I		1	
V <sub>SD</sub>	source-drain voltage	I <sub>S</sub> = -1.7 A; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	-0.6	-1.2	V
t <sub>rr</sub>	reverse recovery time	I <sub>S</sub> = -1.7 A; dI <sub>S</sub> /dt = 100 A/μs;	-	13	-	ns
Q <sub>r</sub>	recovered charge	$V_{GS} = -4.5 \text{ V}; V_{DS} = -15 \text{ V}; T_j = 25 \text{ °C}$	-	4	-	nC
t <sub>a</sub>	reverse recovery rise time		-	7	-	ns
t <sub>b</sub>	reverse recovery fall time		-	6	-	ns

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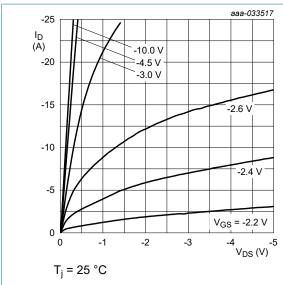


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

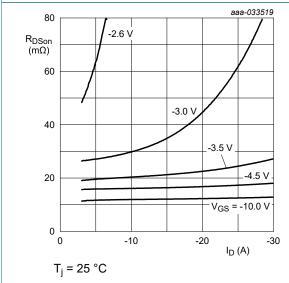


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

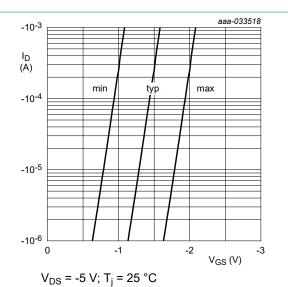


Fig. 7. Sub-threshold drain current as a function of gate-source voltage

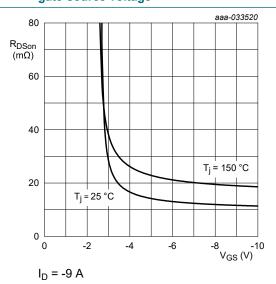


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

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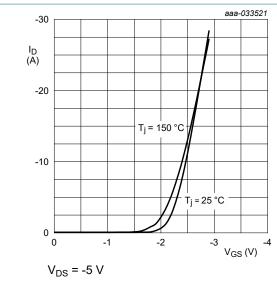


Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

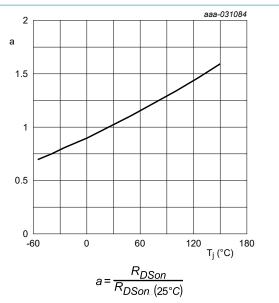


Fig. 11. Normalized drain-source on-state resistance factor as a function of junction temperature; typical values

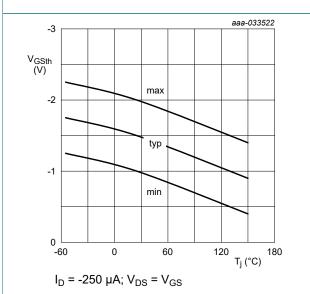
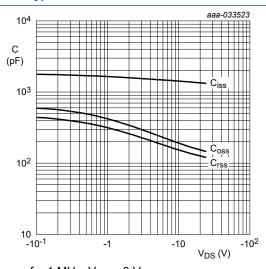


Fig. 12. Gate-source threshold voltage as a function of junction temperature



f = 1 MHz; V<sub>GS</sub> = 0 V Input, output and reverse tran

Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

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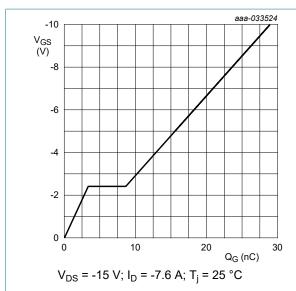


Fig. 14. Gate-source voltage as a function of gate charge; typical values

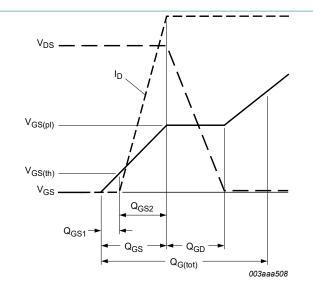


Fig. 15. Gate charge waveform definitions

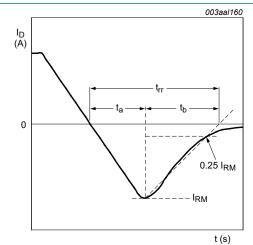


Fig. 16. Reverse recovery timing definition

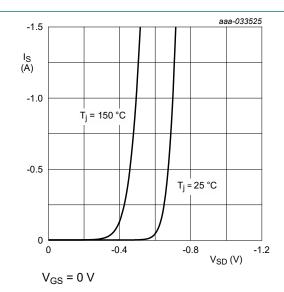
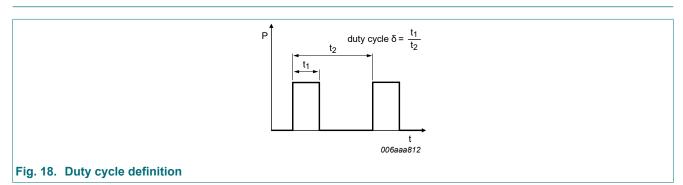


Fig. 17. Source current as a function of source-drain voltage; typical values

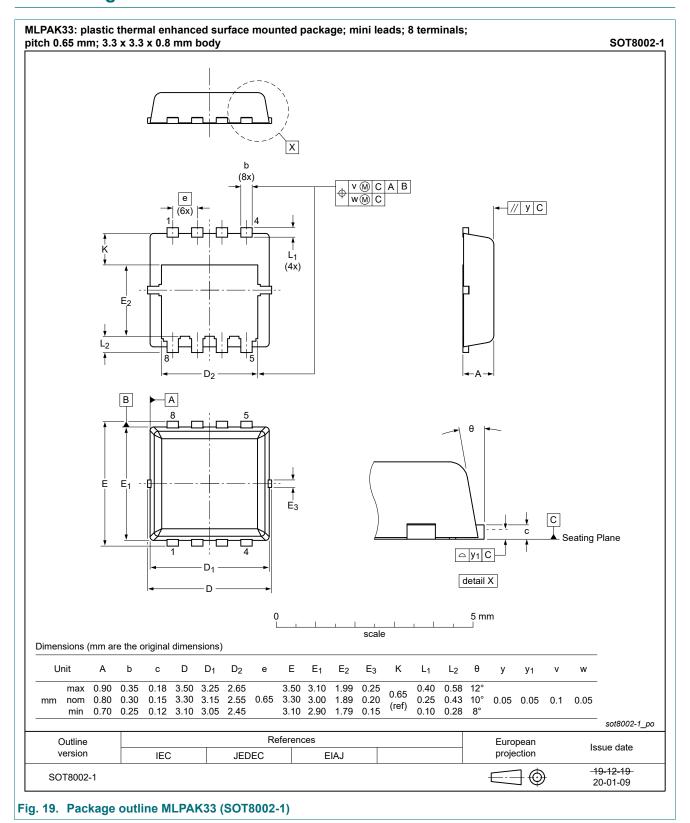
### 11. Test information



**Product data sheet** 

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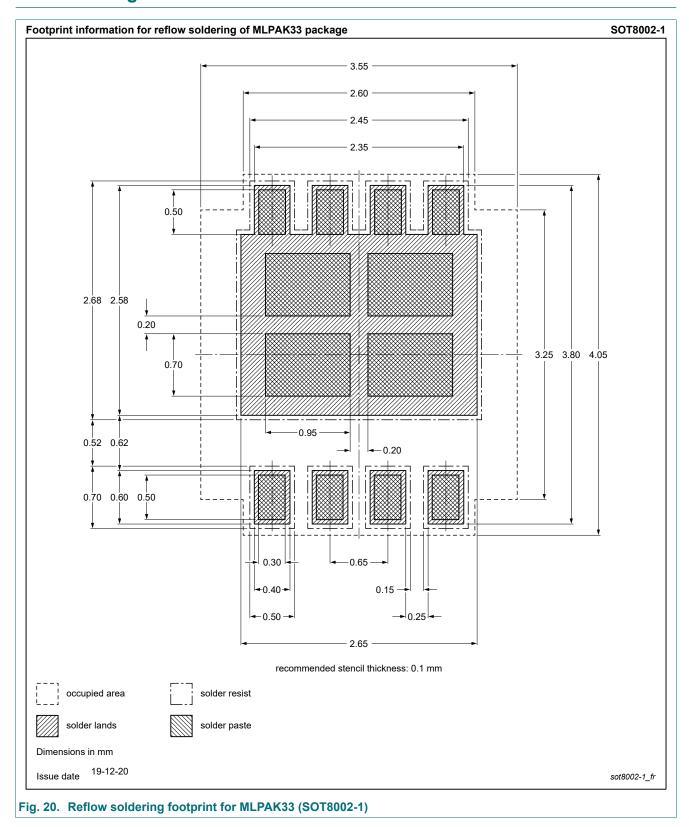
# 12. Package outline



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# 13. Soldering



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# 14. Revision history

### Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PXP012-30QL v.1	20220119	Product data sheet	-	-

#### 30 V, P-channel Trench MOSFET

### 15. Legal information

#### **Data sheet status**

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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PXP012-30QL

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