REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device type 02. - drw	03-11-10	Raymond Monnin
B	Correction to table I, I_{CCPD} test, change unit from µA to mA. - drw	08-12-22	Robert M. Heber
C	Add device type 03, case outline Y, and figure A-2. Add die bonding pad location table under Figure A-1. Delete device class M requirement references. - ro	16-09-02	Charles F. Saffle

REV																				
SHEET																				
REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C						
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28						
REV STATUS			REV			C	C	C	C	C	C	C	C	C	C	C	C	C	C	
OF SHEETS			SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A	PREPARED BY Dan Wonnell	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **http://www.landandmaritime.dla.mil**
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE	CHECKED BY Raymond Monnin	
	APPROVED BY Raymond Monnin	MICROCIRCUIT, LINEAR, DESERIALIZER, MONOLITHIC SILICON
	DRAWING APPROVAL DATE 02-10-07	
AMSC N/A	REVISION LEVEL C	SIZE A · CAGE CODE **67268** · **5962-01535**
		SHEET 1 OF 28

DSCC FORM 2233
APR 97

5962-E535-16

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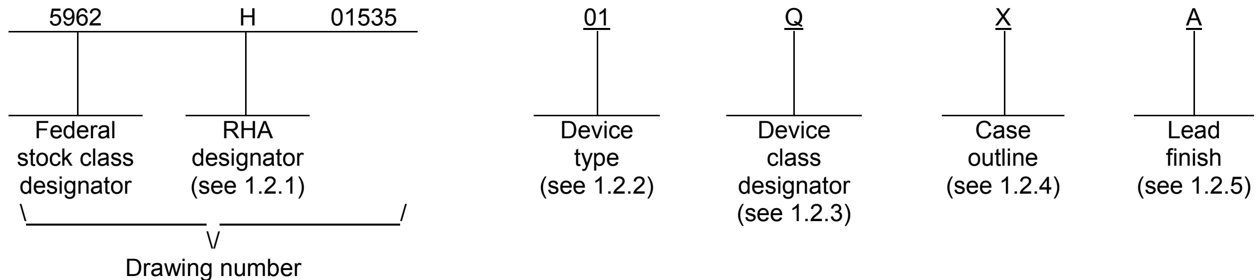
1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	UT54LVDS218	50 MHz Deserializer
02	UT54LVDS218	75 MHz Deserializer
03	RHFLVDS218	75 MHz Deserializer

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	48	Flat pack
Y	See figure 1	48	Flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

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1.3 Absolute maximum ratings. 1/

Supply voltage (V_{DD}):
- Device types 01 and 02 .... -0.3 V dc to 4.0 V dc
- Device type 03 .... 4.8 dc 2/

Output voltage (R_{XOUT}) :
- Device type 03 .... -0.3 V to 4.8 V

Voltage on any pin ($V_{I/O}$):
- Device types 01 and 02 .... -0.3 V dc to (V_{DD} + 0.3 V dc) 3/

DC input current (I_I):
- Device types 01 and 02 .... ±10 mA

TTL inputs (operating or cold spare) (V_I) :
- Device type 03 .... -0.3 V to 4.8 V

LVDS input common mode (V_{CM}) (operating or cold spare):
- Device type 03 .... -5 V to 6 V

Storage temperature (T_{STG}) .... -65°C to +150°C

Power dissipation (P_D) :
- Case outline X .... 1.25 W
- Case outline Y .... 1.25 W

Junction temperature (T_J) 4/ .... +150°C

Thermal resistance, junction-to-case (θ_{JC}) :
- Case outline X .... 10°C/W 5/
- Case outline Y .... 10°C/W 5/

Electrostatic discharge (ESD) for device type 03:
- Human body model (HBM):
  - All pins except LVDS outputs .... 2 kV
  - LVDS outputs versus GND .... 8 kV
- Charge device model (CDM) .... 500 V

1.4 Recommended operating conditions.

Supply voltage (V_{DD}) :
- Device types 01, 02, and 03 .... 3.0 V dc to 3.6 V dc

Input voltage (V_{IN}) :
- Device type 01 and 02 .... 0 V dc to V_{DD}

Static common mode on the receiver (V_{CM}):
- Device type 03 .... -4 V to 5 V

Case temperature range (T_C) .... -55°C to +125°C

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ All voltages, except the differential I/O bus voltage, are with respect to the network ground terminal.
3/ For cold spare mode (V_{DD} = V_{SS}), $V_{I/O}$ may be –0.3 V to the maximum recommended operating V_{DD} + 0.3 V.
4/ Maximum junction temperature may be increased to +175°C during burn-in and life test.
5/ Test per MIL-STD-883, method 1012.

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1.5 Radiation features.

Maximum total dose available (dose rate = 1 rad(Si)/s):
Device types 01 and 02 .... 1 Mrad(Si) 7/
Maximum total dose available (dose rate = 55 mrad(Si)/s) :
Device type 03 .... 300 krad(Si) 8/
Single event effects (SEE):
Device types 01 and 02 only
No Single event latchup (SEL) occurs at effective LET (see 4.4.4.4) .... ≤ 100 MeV/(mg/cm^2) 9/
Device type 03 only
No Single event latchup (SEL) occurs at effective LET (see 4.4.4.4) .... ≤ 120 MeV/(mg/cm^2) 9/
Neutron irradiation:
Device types 01 and 02 only .... 1 X 10^{13} neutrons/cm^2 10/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

7/ Device types 01 and 02 radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition C (dose rate = 1 rad/s) as agreed by the users and manufacturers. Where the final user is not known, the test conditions and results shall be made available in the test report with each purchase order.
8/ Device type 03 radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition C (dose rate = 55 mrad/s) as agreed by the users and manufacturers. Where the final user is not known, the test conditions and results shall be made available in the test report with each purchase order.
9/ Limits are guaranteed by design or process, but not production tested unless specified by the customer through the purchase order or contract.
10/ Limits are guaranteed, but not production tested.

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2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

ASTM INTERNATIONAL (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of semiconductor Devices.

(Copies of these documents are available online at http://www.astm.org or from ASTM International, 100 Barr Harbor Drive, P.O. Box C700, West Conshohocken, PA, 19428-2959).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.1.1 Microcircuit die. For the requirements of microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

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TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ -55°C ≤ TC ≤ +125°C VDD = 3.3 V to 3.6 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
CMOS/TTL DC SPECIFICATIONS ($\overline{\text{PWR DWN}}$, RXOUT)							
High-level input voltage	VIH		1, 2, 3	01, 02, 03	2.0	VDD	V
Low-level input voltage	VIL		1, 2, 3	01, 02, 03	GND	0.8	V
Low-level output voltage	VOL	IOL = 2 mA	1, 2, 3	01, 02		0.3	V
		IOL = 2 mA, VDD = 3 V to 3.6 V		03		0.25	
High-level output voltage	VOH	IOL = -0.4 mA	1, 2, 3	01, 02	2.7		V
		IOL = -0.4 mA, VDD = 3 V to 3.6 V		03	2.7		
High-level input current	IIH	VIN = 3.6 V, VDD = 3.6 V	1, 2, 3	01, 02, 03	-10	+10	µA
Low-level Input current	IIL	VIN = 0 V, VDD = 3.6 V	1, 2, 3	01, 02, 03	-10	+10	µA
Input clamp voltage	VCL	ICL = -18 mA	1, 2, 3	01, 02, 03		-1.5	V
Cold spare leakage current	ICS	VIN = 3.6 V, VDD = VSS	1, 2, 3	01, 02	-20	+20	µA
		VIN = 3.6 V, VDD = VSS		03	-10	10	
Output short circuit current	IOS	VOUT = 0 V 3/ 4/	1, 2, 3	01, 02	-15	-130	mA
		VOUT = 0 V 3/		03	-30	-90	
TTL/CMOS and clock output leakage current in powerdown	IOFF	PWRDWN low, VOUT = 0 V, and PWRDWN low, VOUT = VDD	1, 2, 3	03	-10	10	µA
LVDS RECEIVER SPECIFICATIONS (IN+, IN-)							
Differential input high threshold	VTH	VCM =+1.2 V 4/	1, 2, 3	01, 02		+100	mV
		VCM =+1.2 V 4/		03		+100	
		-4 V < VCM < 5 V 4/				+130	
Differential input low threshold	VTL	VCM =+1.2 V 4/	1, 2, 3	01, 02	-100		mV
		VCM =+1.2 V		03	-100		
		-4 V < VCM < 5 V			-130		
Common mode voltage range	VCMR	VID = 210 mV 5/	1, 2, 3	01, 02	0.2	2.0	V
		VID = 200 mVp-p 5/		03	-4	5	

See footnotes at end of table.

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TABLE IA. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ 2/ -55°C ≤ T_C ≤ +125°C V_{DD} = 3.3 V to 3.6 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
LVDS RECEIVER SPECIFICATIONS (IN+, IN-) – continued.							
Input current	I_{IN}	V_{IN} = 2.4 V, V_{DD} = 3.6 V	1, 2, 3	01, 02	-10	+10	µA
		V_{IN} = 0 V, V_{DD} = 3.6 V			-10	+10	
Differential input current	I_{ID}	V_{ID} = 400 mVpp	1,2,3	03	-10	10	µA
Common mode input current	I_{ICM}	V_{IC} = -4 V to 5 V	1,2,3	03	-70	70	µA
Cold spare leakage current	ICSIN	V_{IN} = 3.6 V, V_{DD} = V_{SS}	1, 2, 3	01, 02	-20	+20	µA
		V_{IN} = 3.6 V, V_{DD} = V_{SS}		03	-60	+60	
SUPPLY CURRENT							
Active supply current	I_{CC}	C_L = 8 pF, see figure 3 4/	1, 2, 3	01, 02		105	mA
		C_L = 8 pF, see figure 3		03		65	
Power down supply current	I_{CCPD}	$\overline{\text{PWRDWN}}$ = low, LVDS inputs = low logic, V_{DD} = 3.6 V	1, 2, 3	01, 02, 03		2.0	mA

See footnotes at end of table.

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TABLE IA. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ 2/ -55°C ≤ T_C ≤ +125°C V_{DD} = 3.0 V dc to 3.6 V dc unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
RECEIVER SWITCHING CHARACTERISTICS – continued. 6/								
CMOS/TTL low-to-high transition time	CLHT	See figure 4, 4/		9, 10, 11	01, 03		3.5	ns
CMOS/TTL high-to-low transition time	CHLT	See figure 4, 4/		9, 10, 11	01, 03		3.5	ns
Receiver input strobe position for bit 0	RSPos0	See figure 9, 4/	f = 50 MHz	9, 10, 11	01	0.59	1.33	ns
			f = 75 MHz		02, 03	0.50	1.24	
Receiver input strobe position for bit 1	RSPos1	See figure 9, 4/	f = 50 MHz	9, 10, 11	01	3.45	4.19	ns
			f = 75 MHz		02, 03	2.41	3.15	
Receiver input strobe position for bit 2	RSPos2	See figure 9, 4/	f = 50 MHz	9, 10, 11	01	6.30	7.04	ns
			f = 75 MHz		02, 03	4.31	5.05	
Receiver input strobe position for bit 3	RSPos3	See figure 9, 4/	f = 50 MHz	9, 10, 11	01	9.16	9.90	ns
			f = 75 MHz		02, 03	6.22	6.96	
Receiver input strobe position for bit 4	RSPos4		f = 50 MHz	9, 10, 11	01	12.02	12.76	ns
			f = 75 MHz		02, 03	8.12	8.86	
Receiver input strobe position for bit 5	RSPos5		f = 50 MHz	9, 10, 11	01	14.88	15.62	ns
			f = 75 MHz		02, 03	10.03	10.77	
Receiver input strobe position for bit 6	RSPos6		f = 50 MHz	9, 10, 11	01	17.73	18.47	ns
			f = 75 MHz		02, 03	11.93	12.67	
RxCLK OUT period	RCOP		f = 50 MHz	9, 10, 11	01	20.00	66.7	ns
			f = 75 MHz		02, 03	13.3	66.7	
RxCLK OUT high time	RCOH		f = 50 MHz,	9, 10, 11	01	3.6		ns
			f = 75 MHz		02, 03	3.6		
RxCLK OUT low time	RCOL		f = 50 MHz	9, 10, 11	01	3.6		ns
			f = 75 MHz		02, 03	3.6		
RxOUT setup to RxCLK OUT	RSRC		f = 50 MHz	9, 10, 11	01	3.5		ns
			f = 75 MHz		02, 03	3.5		
RxOUT hold to RxCLK OUT	RHRC		f = 50 MHz	9, 10, 11	01	3.5		ns
			f = 75 MHz		02, 03	3.5		

See footnotes at end of table.

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TABLE IA. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ 2/ -55°C ≤ T_C ≤ +125°C V_{DD} = 3.0 V dc to 3.6 V dc unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
RECEIVER SWITCHING CHARACTERISTICS – continued. 6/								
RxCLK IN to RxCLK OUT delay	RCCD	See figure 6, 8/	f = 50 MHz	9, 10, 11	01	3.4	8.3	ns
			f = 75 MHz		02	3.4	8.3	
			f = 75 MHz		03	3.4	8.3	
Receiver phase lock loop set	RPLLS	See figure 7 5/		9, 10,11	01, 02, 03		10	ms
Receiver powerdown delay	RPDD	See figure 8		9, 10,11	01, 02, 03		2	μs

1/ Pre and Post irradiation values are identical unless otherwise specified in table I. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C (see 1.5 herein).
2/ Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except differential voltages.
3/ Output short current (I_{OS}) is specified as magnitude only, minus sign indicates direction only. Only one output should be shorted at a time for a maximum duration of one second.
4/ Guaranteed by characterization.
5/ Functionally tested.
6/ Receiver skew margin is defined as the valid data sampling region at the receiver inputs. This margin takes into account the transmitter pulse positions (min and max) and the receiver input setup and hold time (internal data sampling window). This margin allows LVDS interconnect skew, inter-symbol interface (both dependent on type/length of cable), and source clock jitter less than 250 ps (calculated from T_{POS} to R_{POS}).
7/ Guaranteed by design.
8/ Total latency for the channel link chipset is a function of clock period and gate delays through the transmitter (TCCD) and receiver (RCCD). The total latency for LVDS217 Serializer and the LVDS218 Deserializer is (T + TCCD) + 2*T + RCCD), where T = clock period.

TABLE IB. SEP test limits. 1/ 2/ 3/

Device types	Bias V_{DD} = 3.6 V for Single event latch-up (SEL) test No SEL occurs at effective LET
01, 02	LET ≤ 100 MeV/(mg/cm^2)
03	LET ≤ 120 MeV/(mg/cm^2)

1/ For SEP test conditions, see 4.4.4.4 herein.
2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.
3/ Limits are guaranteed by design or process, but not production tested unless specified by the customer through the purchase order or contract. For details SEE report, please contact device manufactures.

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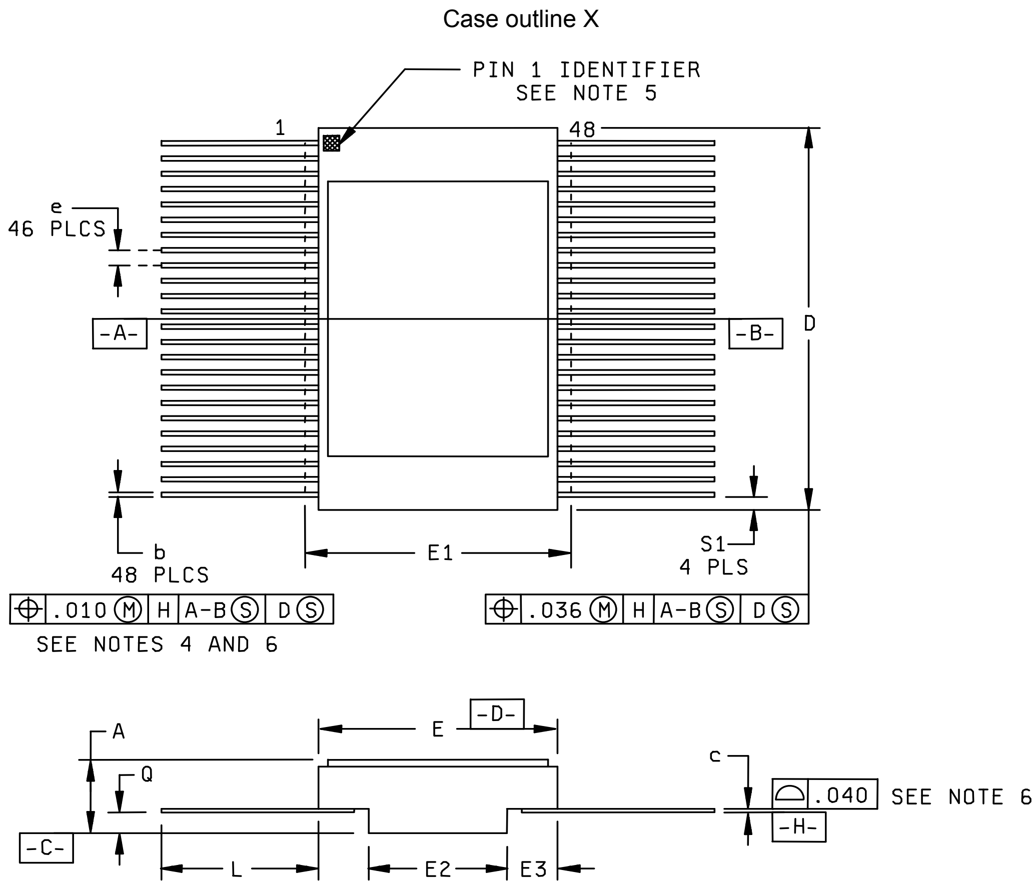
Case outline X



Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A	.093	.115	2.362	2.921
b	.006	.010	0.152	0.254
c	.004	.007	0.102	0.178
D	.622	.638	15.799	16.205
E	.374	.386	9.500	9.804
E1		.415		10.541
E2	.274	.286	6.960	7.264
E3	.030		0.762	
e	.025 BSC		0.635 BSC	
L	.300	.320	7.620	8.128
Q	.011	REF	0.279	REF
S1	.005		0.127	

NOTES:
1. The U.S. Government preferred system of measurement is the metric SI system. However, since this item originally designed using inch-pound units of measurement, in the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.
2. All exposed metalized areas are gold plated over electroplated nickel per MIL-PRF-38535. Lead finishes are in accordance with MIL-PRF-38535.
3. The lid is electrically connected to V_{SS}.
4. Lead position and coplanarity are not measured.
5. ID mark symbol is vendor option.
6. With solder, increase maximum by 0.003 inches.

FIGURE 1. Case outline.

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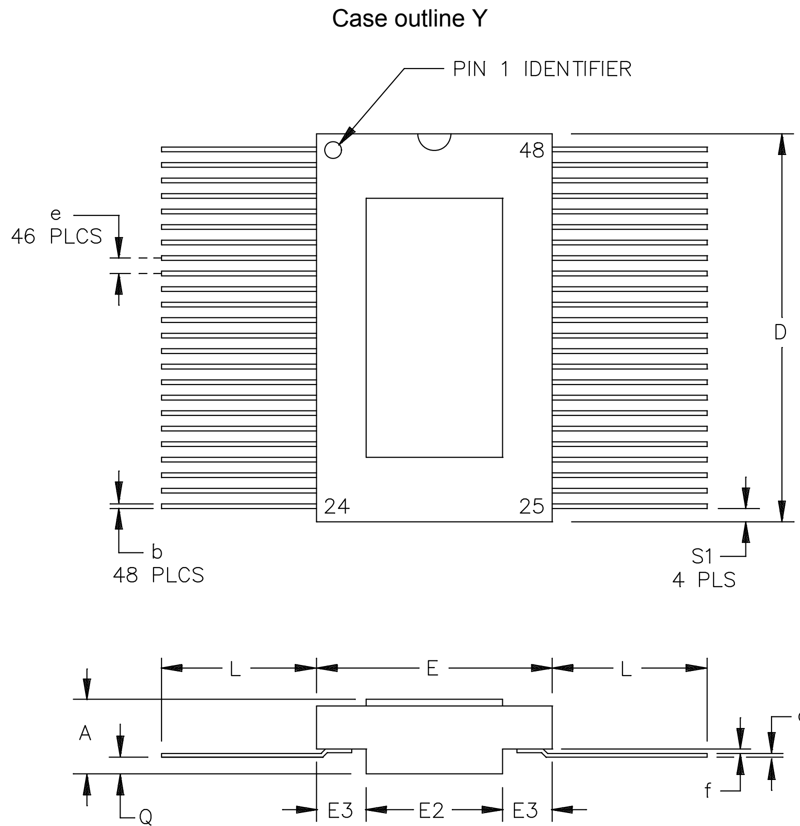
Case outline Y



Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A	.086	.107	2.18	2.72
b	.008	.012	0.20	0.30
c	.005	.007	0.12	0.18
D	.613	.627	15.57	15.92
E	.375	.385	9.52	9.78
E2	.245	.255	6.22	6.48
E3	.060	.070	1.52	1.78
e	.025 BSC		0.635 BSC	
f	.008 BSC		0.20 BSC	
L	.270	.370	6.85	9.40
Q	.026	.036	0.66	0.92
S1	.010	.024	0.25	0.61

NOTES:

1. The U.S. Government preferred system of measurement is the metric SI system. However, since this item originally designed using inch-pound units of measurement, in the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.
2. All exposed metalized areas are gold plated over electroplated nickel per MIL-PRF-38535. Lead finishes are in accordance with MIL-PRF-38535.
3. The lid is electrically connected to V_{SS}.
4. Lead position and coplanarity are not measured.
5. ID mark symbol is vendor option.

FIGURE 1. Case outlines - continued.

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Device types	01, 02, 03
Case outlines	X, Y
Terminal number	Terminal symbol
1	RxOUT 17
2	RxOUT 18
3	GND
4	RxOUT 19
5	RxOUT 20
6	N/C
7	LVDS GND
8	RxIN 0-
9	RxIN 0+
10	RxIN 1-
11	RxIN 1+
12	LVDS V_{DD}
13	LVDS GND
14	RxIN 2-
15	RxIN 2+
16	RxCLK IN-
17	RxCLK IN+
18	LVDS GND
19	PLL GND
20	PLL V_{DD}
21	PLL GND
22	$\overline{\text{POWER DWN}}$
23	RxCLK OUT
24	RxOUT 0

Device types	01, 02, 03
Case outlines	X, Y
Terminal number	Terminal symbol
25	GND
26	RxOUT 1
27	RxOUT 2
28	V_{DD}
29	RxOUT 3
30	RxOUT 4
31	RxOUT 5
32	GND
33	RxOUT 6
34	RxOUT 7
35	RxOUT 8
36	V_{DD}
37	RxOUT 9
38	GND
39	RxOUT 10
40	RxOUT 11
41	RxOUT 12
42	V_{DD}
43	RxOUT 13
44	GND
45	RxOUT 14
46	RxOUT 15
47	RxOUT 16
48	V_{DD}

FIGURE 2. Terminal connections.

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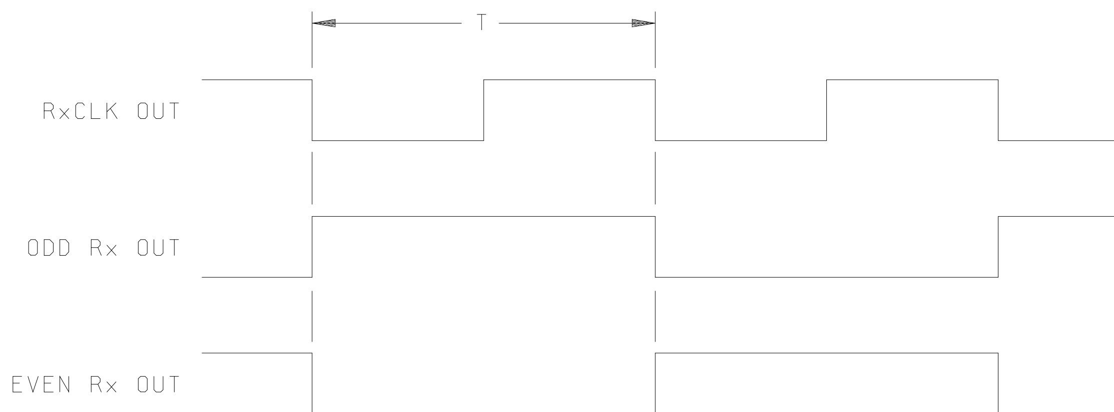

FIGURE 3. Test Pattern.

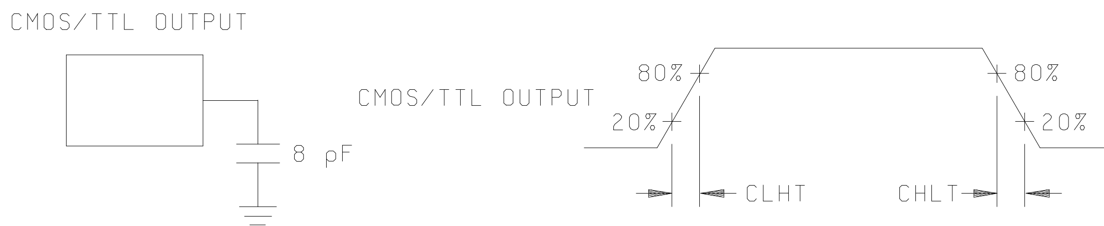

FIGURE 4. Output Load and Transition Times.

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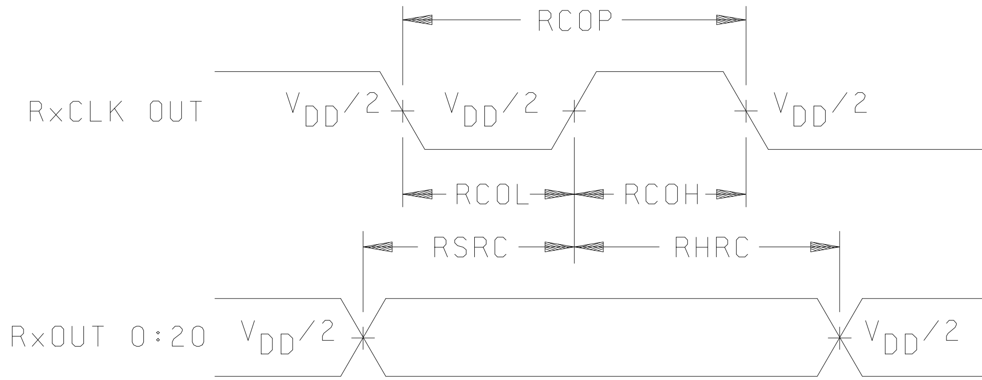

FIGURE 5. Setup/Hold and High/Low Times.

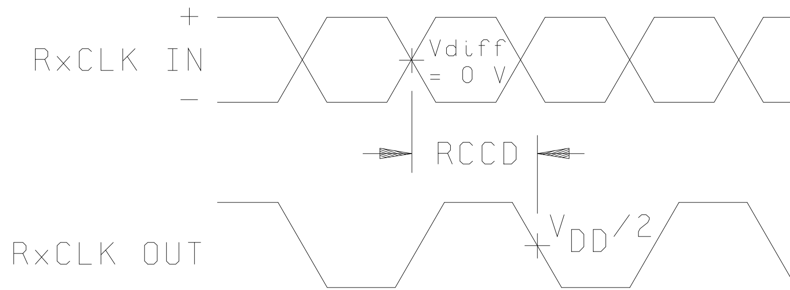

FIGURE 6. Clock-to-Clock Out Delay.

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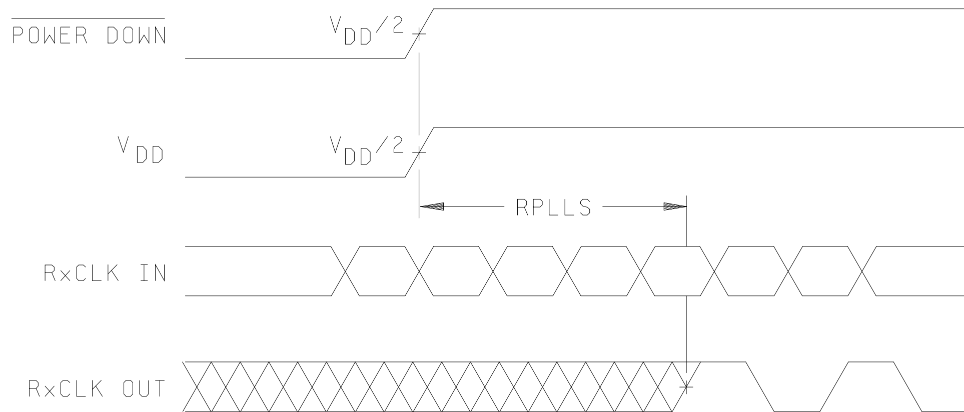

FIGURE 7. Phase Lock Loop Set Time.

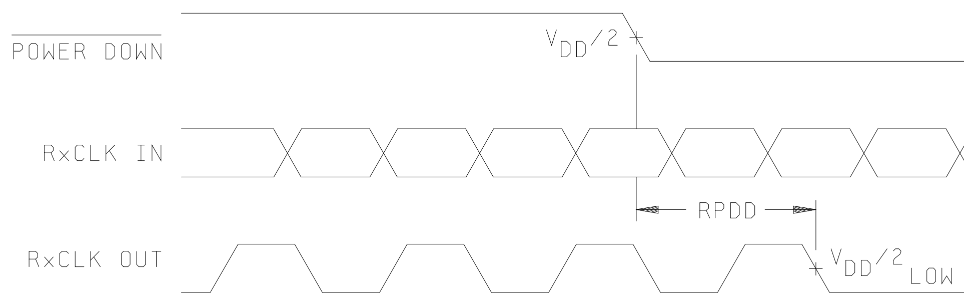

FIGURE 8. Receiver Powerdown Delay.

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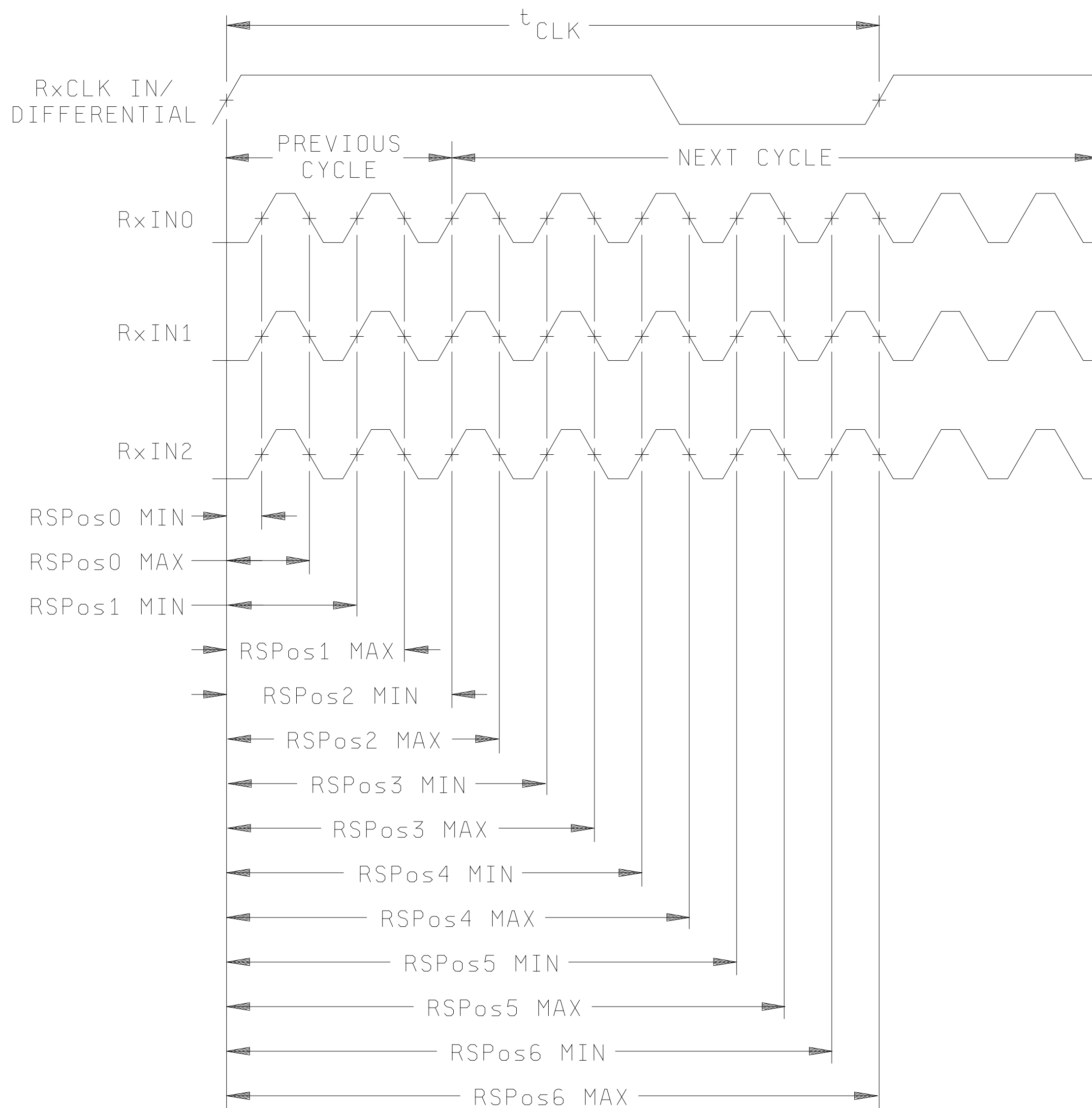

FIGURE 9. Receiver LVDS Input Strobe Position.

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4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 4, 5, 6, 7 and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

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TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1	1
Final electrical parameters (see 4.2)	1, 2, 3, 1/ 9, 10, 11	1, 2, 3, 1/ 2/ 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 9, 10, 11	1, 2, 3, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3 2/
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)	1, 9	1, 9

1/ PDA applies to subgroup 1.
2/ Delta limits as specified in table IIB shall be required where specified, and the delta limits shall be computed with reference to the previous electrical parameters.

TABLE IIB. Burn-in and operating life test delta parameters. T_A = +25°C.

Parameters	Symbol	Conditions	Device types	Limit
Active supply current	I_{CC}	C_L = 8 pF, see figure 3	03	±0.5 mA
Low level output voltage	V_{OL}	I_{OL} = 2 mA, V_{DD} = 3 V to 3.6 V	03	±0.02 V
High level output voltage	V_{OH}	I_{OL} = 0.4 mA, V_{DD} = 3 V to 3.6 V	03	±0.02 V

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4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total irradiation dose testing. Total irradiation dose testing shall be performed in accordance with MIL-STD-883 method 1019, condition C (dose rate = 1 rad/s) for device types 01 and 02, and for device type 03 condition C (dose rate = 55 mrad/s) as specified herein.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5 krads(Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Dose rate latchup testing. Dose rate induced latchup testing shall be performed in accordance with test method 1020 of MIL-STD-883 and as specified herein (see 1.5 herein). Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may effect the RHA capability of the process.

4.4.4.3 Dose rate burnout. When required by the customer test shall be performed on devices, SEC, or approved test structures at technology qualifications and after any design or process changes which may effect the RHA capability of the process. Dose rate burnout shall be performed in accordance with test method 1023 of MIL-STD-883 and as specified herein.

4.4.4.4 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be performed on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^7 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 micron in silicon. However, the particle range shall be adequate to detect latch-up, because the relevant junction is often buried deep below the active chip volume. In order to detect latch-up the ion range shall be sufficient to penetrate well beyond the deepest part of the sensitive volume of the devices.

e. The test temperature shall be +25°C and the maximum rated operating temperature ±10°C.

f. Bias conditions shall be defined by the manufacturer for the latchup measurements.

g. For SEL test limits, see Table IB herein.

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5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Additional information. When applicable, a copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA test conditions (SEP).

b. Number of latch-up (SEL).

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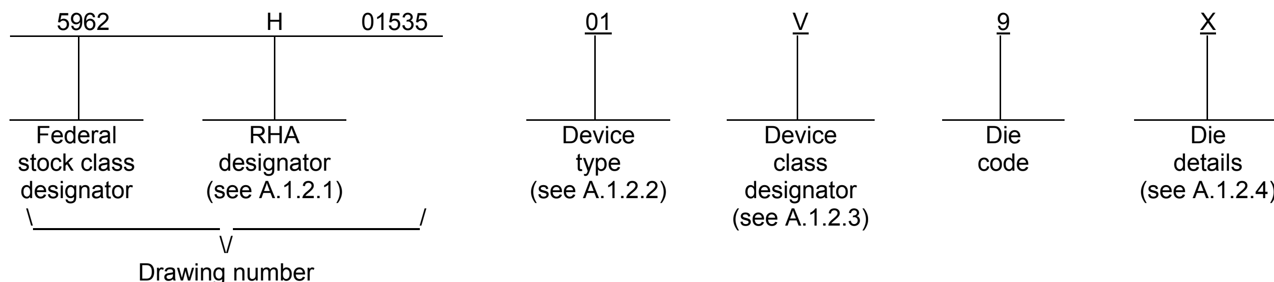
APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-01535

A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multi-chip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device class V) are reflected in the Part or Identification Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

A.1.2 PIN. The PIN is as shown in the following example:



A.1.2.1 RHA designator. Device classes Q and V RHA identified die meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	UT54LVDS218	50 MHz Deserializer
02	UT54LVDS218	75 MHz Deserializer
03	RHFLVDS218	75 MHz Deserializer

A.1.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

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A.1.2.4 Die details. The die details designation is a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die physical dimensions.

Die type	Figure number
01, 02	A-1
03	A-2

A.1.2.4.2 Die bonding pad locations and electrical functions.

Die type	Figure number
01, 02	A-1
03	A-2

A.1.2.4.3 Interface materials.

Die type	Figure number
01, 02	A-1
03	A-2

A.1.2.4.4 Assembly related information.

Die type	Figure number
01, 02	A-1
03	A-2

A.1.3 Absolute maximum ratings. See paragraph 1.3 herein for details.

A.1.4 Recommended operating conditions. See paragraph 1.4 herein for details.

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A.2 APPLICABLE DOCUMENTS.

A.2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARD

MIL-STD-883 - Test Method Standard Microcircuits.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

A.3 REQUIREMENTS

A.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein and the manufacturer's QM plan for device classes Q and V.

A.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figure A-1.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figure A-1.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figure A-1.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and on figure A-1.

A.3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be as defined in paragraph 3.2.3 herein.

A.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table IA of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table IA.

A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

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A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

A.4 VERIFICATION

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not affect the form, fit, or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum, it shall consist of:

a. Wafer lot acceptance for class V product using the criteria defined in MIL-STD-883, method 5007.

b. 100% wafer probe (see paragraph A.3.4 herein).

c. 100% internal visual inspection to the applicable class Q or V criteria defined in MIL-STD-883, method 2010 or the alternate procedures allowed in MIL-STD-883, method 5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein. Group E tests and conditions are as specified in paragraphs 4.4.4, 4.4.4.1, 4.4.4.1.1, 4.4.4.2, 4.4.4.3, and 4.4.4.4 herein.

A.5 DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

A.6 NOTES

A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications, and logistics purposes.

A.6.2 Comments. Comments on this appendix should be directed to DLA Land and Maritime -VA, Columbus, Ohio, 43218-3990 or telephone (614)-692-0540.

A.6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see A.6.4 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

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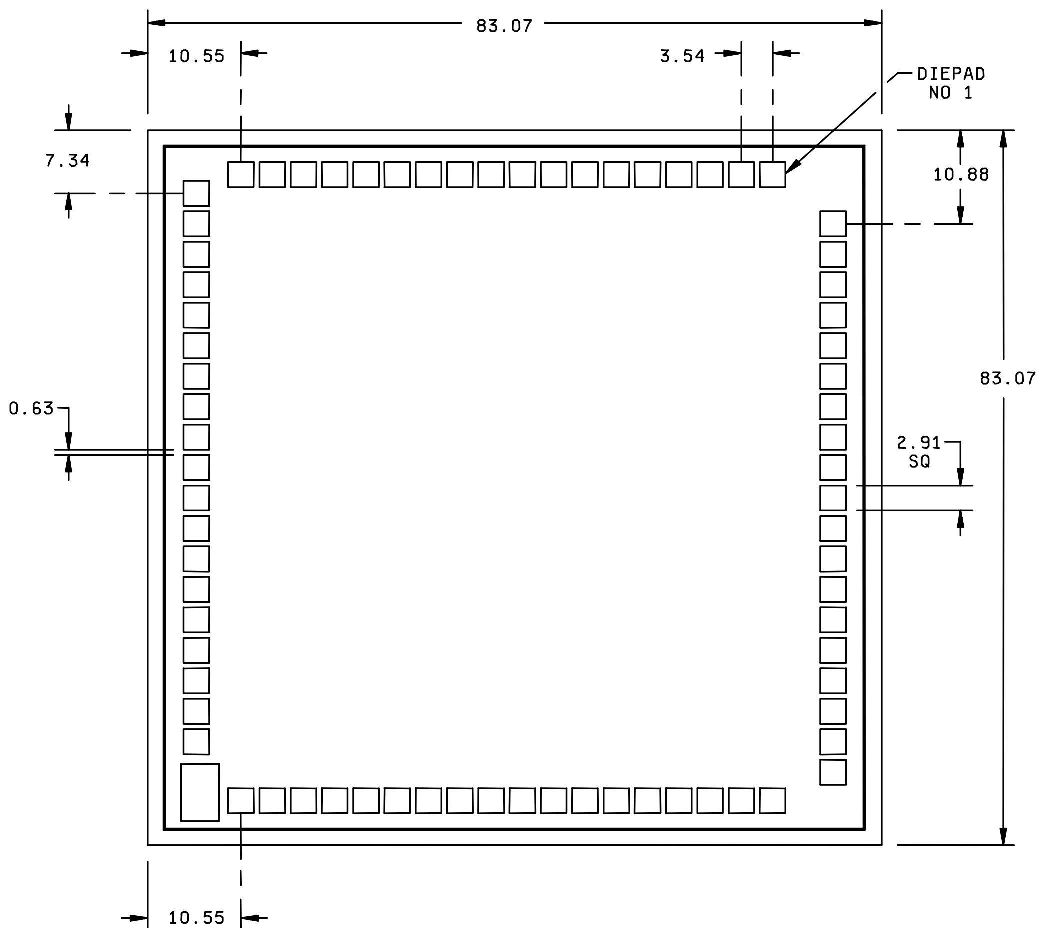
APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-01535



Die bonding pad locations and electrical functions

Die physical dimensions.
Die size: 83.07 mils X 83.07 mils
Die thickness: 17.5 mils ±1 mil

Interface materials.
Top metallization: Al, 0.5% CU
Backside metallization: None

Glassivation.
Type: SiO2/Si3N4
Thickness: 10.0kÅ

Substrate: Epitaxial layer on single crystal silicon

Assembly related information.
Substrate potential: Tied to VSS
Special assembly instructions: Contact manufacturer for bonding information on die pads 8-11 and 45-48.

FIGURE A-1. Die bonding pad locations and electrical functions.

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APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-01535

Die pad	X center	Y center	Pad symbol
1	29.3	35.9	N/C
2	25.7	35.9	N/C
3	22.2	35.9	N/C
4	18.6	35.9	N/C
5	15.1	35.9	RXOUT15
6	11.5	35.9	RXOUT16
7	8	35.9	V_{DD}
8	4.5	35.9	N/C
9	0.9	35.9	N/C
10	-2.6	35.9	N/C
11	-6.2	35.9	N/C
12	-9.7	35.9	RXOUT17
13	-13.3	35.9	RXOUT18
14	-16.8	35.9	V_{SS}
15	-20.4	35.9	N/C
16	-23.9	35.9	N/C
17	-27.4	35.9	N/C
18	-31	35.9	N/C
19	-35.9	34.2	N/C
20	-35.9	30.7	RXOUT19
21	-35.9	27.1	RXOUT20
22	-35.9	23.6	N/C
23	-35.9	20	LVDSGND
24	-35.9	16.5	RXIN0-
25	-35.9	12.9	RXIN0+
26	-35.9	9.4	RXIN1-
27	-35.9	5.9	RXIN1+
28	-35.9	2.3	LVDSVDD
29	-35.9	-1.2	LVDSGND
30	-35.9	-4.8	RXIN2-
31	-35.9	-8.3	RXIN2+
32	-35.9	-11.9	RXCLKIN-
33	-35.9	-15.4	RXCLKIN+
34	-35.9	-19	LVDSGND
35	-35.9	-22.5	PLLGND
36	-35.9	-26	PLLVDD
37	-35.9	-29.6	PLLGND

Die pad	X center	Y center	Pad symbol
38	-31	-35.9	N/C
39	-27.4	-35.9	N/C
40	-23.9	-35.9	N/C
41	-20.4	-35.9	N/C
42	-16.8	-35.9	PWRDWN_B
43	-13.3	-35.9	RXCLKOUT
44	-9.7	-35.9	RXOUT0
45	-6.2	-35.9	N/C
46	-2.6	-35.9	N/C
47	0.9	-35.9	N/C
48	4.5	-35.9	V_{SS}
49	8	-35.9	N/C
50	11.5	-35.9	RXOUT1
51	15.1	-35.9	RXOUT2
52	18.6	-35.9	N/C
53	22.2	-35.9	N/C
54	25.7	-35.9	N/C
55	29.3	-35.9	N/C
56	35.9	-33.1	N/C
57	35.9	-29.6	V_{DD}
58	35.9	-26	RXOUT3
59	35.9	-22.5	RXOUT4
60	35.9	-19	RXOUT5
61	35.9	-15.4	V_{SS}
62	35.9	-11.9	RXOUT6
63	35.9	-8.3	RXOUT7
64	35.9	-4.8	RXOUT8
65	35.9	-1.2	V_{DD}
66	35.9	2.3	RXOUT9
67	35.9	5.9	V_{SS}
68	35.9	9.4	RXOUT10
69	35.9	12.9	RXOUT11
70	35.9	16.5	RXOUT12
71	35.9	20	V_{DD}
72	35.9	23.6	RXOUT13
73	35.9	27.1	V_{SS}
74	35.9	30.7	RXOUT14

NOTES:
1. Contact manufacturer for bonding information on these pads.
2. Units are in mils.
3. Origin (0,0) = die center

FIGURE A-1. Die bonding pad locations and electrical functions.

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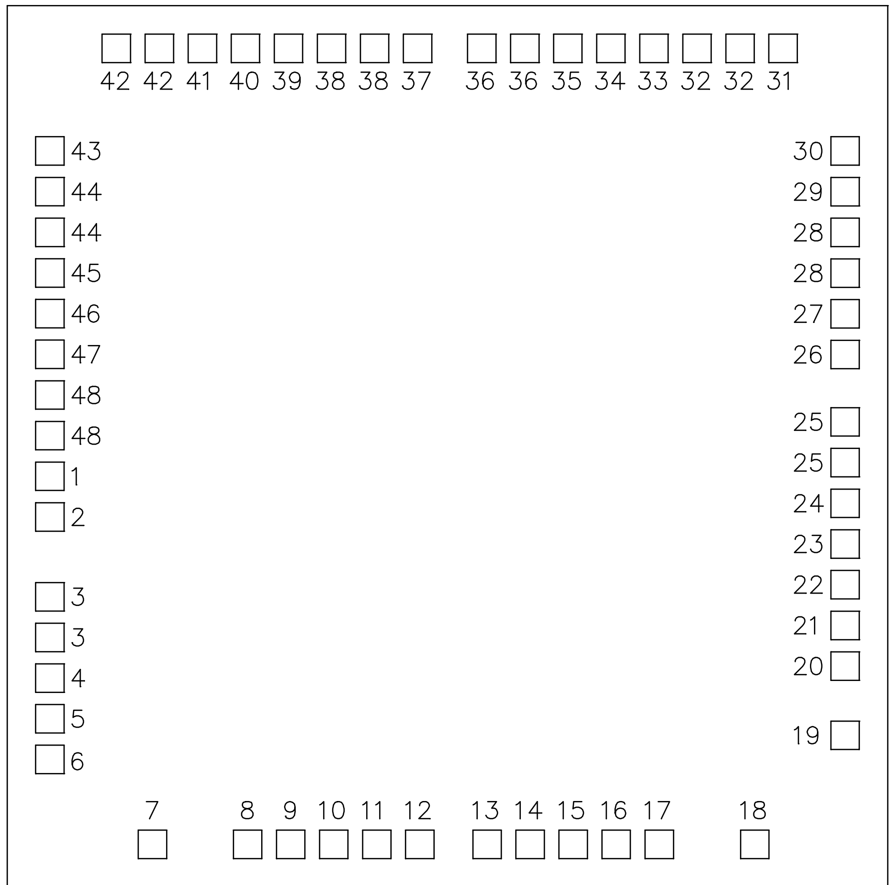

Die bonding pad locations and electrical functions

Die physical dimensions.
Die size: 100.8 mils x 100.8 mils
Die thickness: 112 mils ±0.4 mil

Interface materials.
Top metallization: Metal 1: TaN/Ta/Cu = 0.250 μm
Metal 2: TaN/Ta/Cu = 0.350 μm
Metal 3: TaN/Ta/Cu = 0.350 μm
Metal 4: TaN/Ta/Cu = 0.900 μm
Metal 5: Al/Cu = 1.2 μm (Top)
Backside metallization: raw silicon – back grinding

Glassivation.
Type: PSG + Nitride
Thickness: 0.044 mil

Substrate: Single crystal silicon

Assembly related information.
Substrate potential: Tied to V_{SS}.

FIGURE A-2. Die bonding pad locations and electrical functions.

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APPENDIX A

APPENDIX A FORMS A PART OF SMD 5962-01535

Die pad	X center	Y center	Pad symbol	Die pad	X center	Y center	Pad symbol
42	-915.5	1155.01	V_{DD}	20	1155.0	-690.88	PLL V_{DD}
42	-798.5	1155.01	V_{DD}	19	1155.0	-880.88	PLL GND
41	-681.5	1155.01	RXOUT12	18	855.03	-1155.0	LVDS GND
40	-564.5	1155.01	RXOUT11	17	591.0	-1155.0	RXCLKINP
39	-447.5	1155.01	RXOUT10	16	467.0	-1155.0	RXCLKINN
38	-330.5	1155.01	GND	15	343.0	-1155.0	RxIN2P
38	-213.5	1155.01	GND	14	219.0	-1155.0	RxIN2N
37	-96.6	1155.01	RXOUT9	13	95.0	-1155.0	LVDS GND
36	93.5	1155.01	V_{DD}	12	-95.0	-1155.0	LVDS V_{DD}
36	210.5	1155.01	V_{DD}	11	-219.0	-1155.0	RxIN1P
35	327.5	1155.01	RXOUT8	10	-343.0	-1155.0	RxIN1N
34	444.5	1155.01	RXOUT7	9	-467.0	-1155.0	RxIN0P
33	561.5	1155.01	RXOUT6	8	-591.0	-1155.0	RxIN0N
32	678.5	1155.01	GND	7	-855.03	-1155.0	LVDS GND
32	795.5	1155.01	GND	6	-1155.0	-880.88	NC
31	912.5	1155.01	RXOUT5	5	-1155.0	-765.88	RXOUT20
30	1155.0	797.96	RXOUT4	4	-1155.0	-650.88	RXOUT19
29	1155.0	682.96	RXOUT3	3	-1155.0	-535.88	GND
28	1155.0	567.96	V_{DD}	3	-1155.0	-420.88	GND
28	1155.0	452.95	V_{DD}	2	-1155.0	-230.88	RXOUT18
27	1155.0	337.95	RXOUT2	1	-1155.0	-115.88	RXOUT17
26	1155.0	222.95	RXOUT1	48	-1155.0	-0.88	V_{DD}
25	1155.0	32.95	GND	48	-1155.0	114.13	V_{DD}
25	1155.0	-82.0	GND	47	-1155.0	229.13	RXOUT16
24	1155.0	-199.59	RXOUT0	46	-1155.0	344.13	RXOUT15
23	1155.0	-314.6	RXCLKOUT	45	-1155.0	459.13	RXOUT14
22	1155.0	-429.6	PWN DWN	44	-1155.0	574.13	GND
21	1155.0	-564.6	PLL GND	44	-1155.0	689.13	GND
				43	-1155.0	804.13	RXOUT13

All X and Y pad dimensions are the same at 80.0.

NOTES:
1. Units are in μm.
2. Origin (0,0) = die center.

FIGURE A-2. Die bonding pad locations and electrical functions - continued.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 16-09-02

Approved sources of supply for SMD 5962-01535 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962H0153501QXA	65342	UT54LVDS218UCA
5962H0153501QXC	65342	UT54LVDS218UCC
5962H0153501VXA	65342	UT54LVDS218UCA
5962H0153501VXC	65342	UT54LVDS218UCC
5962H0153501Q9A	65342	UT54LVDS218-QDIE
5962H0153501V9A	65342	UT54LVDS218-VDIE
5962H0153502QXA	65342	UT54LVDS218UCA
5962H0153502QXC	65342	UT54LVDS218UCC
5962H0153502VXA	65342	UT54LVDS218UCA
5962H0153502VXC	65342	UT54LVDS218UCC
5962H0153502Q9A	65342	UT54LVDS218-QDIE
5962H0153502V9A	65342	UT54LVDS218-VDIE
5962F0153503VYC	F8859	RHFLVDS218K01V
5962F0153503V9A	F8859	RHFLVDS218D2V

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
65342	Aeroflex, UTMC Microelectronic Systems, Inc. 4350 Centennial Blvd. Colorado Springs, CO 80907-3486
F8859	ST Microelectronics 3 rue de Suisse CS 60816 35208 RENNES cedex2-FRANCE

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