



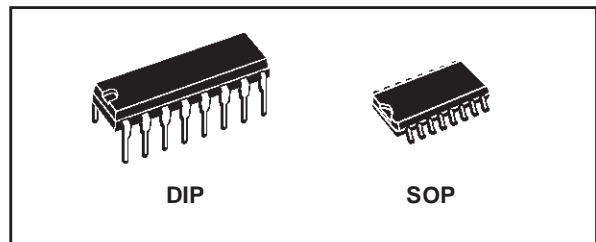
HCF4040B

RIPPLE-CARRY BINARY COUNTER/DIVIDERS 12 STAGE

- MEDIUM SPEED OPERATION :
 $t_{PD} = 80\text{ns}$ (TYP.) at $V_{DD} = 10\text{V}$
- FULLY STATIC OPERATION
- COMMON RESET
- BUFFERED INPUTS AND OUTPUTS
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT SPECIFIED UP TO 20V
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT LEAKAGE CURRENT
 $I_I = 100\text{nA}$ (MAX) AT $V_{DD} = 18\text{V}$ $T_A = 25^\circ\text{C}$
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC JESD13B "STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES"

DESCRIPTION

The HCF4040B is a monolithic integrated circuit fabricated in Metal Oxide Semiconductor technology available in DIP and SOP packages.



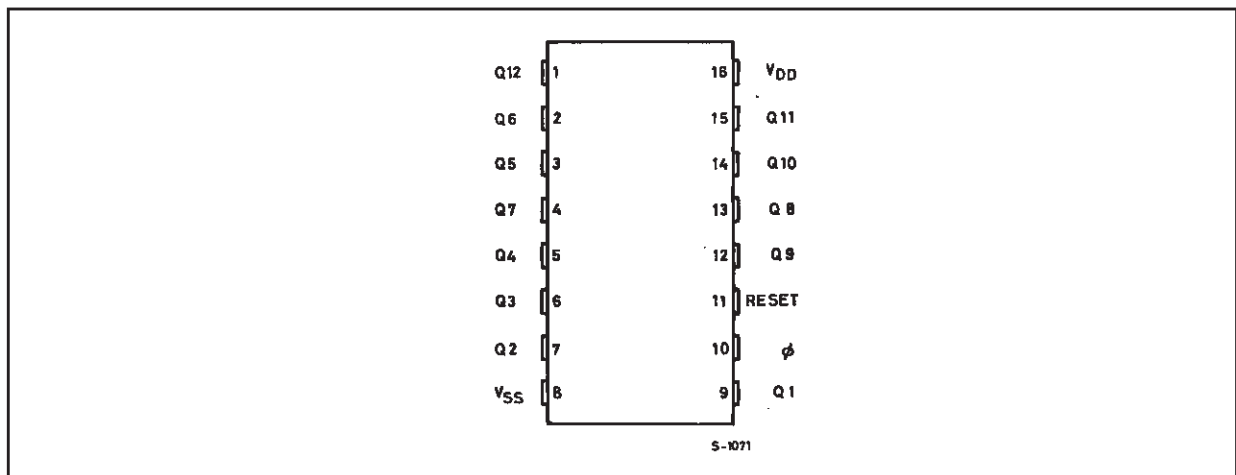
ORDER CODES

PACKAGE	TUBE	T & R
DIP	HCF4040BEY	
SOP	HCF4040BM1	HCF4040M013TR

The HCF4040B is a ripple carry binary counter. All counter stages are master-slave flip-flops. The state of a counter advances one count on the negative transition of each input pulse; a high level on the RESET line resets the counter to its all zeros stage. Schmitt trigger action on the input pulse line permits unlimited clock rise and fall times.

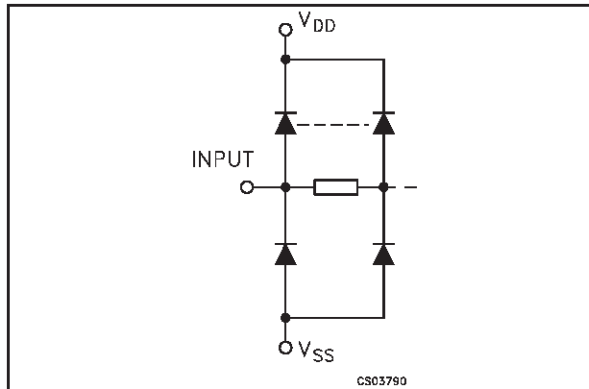
All inputs and outputs are buffered

PIN CONNECTION



HCF4040B

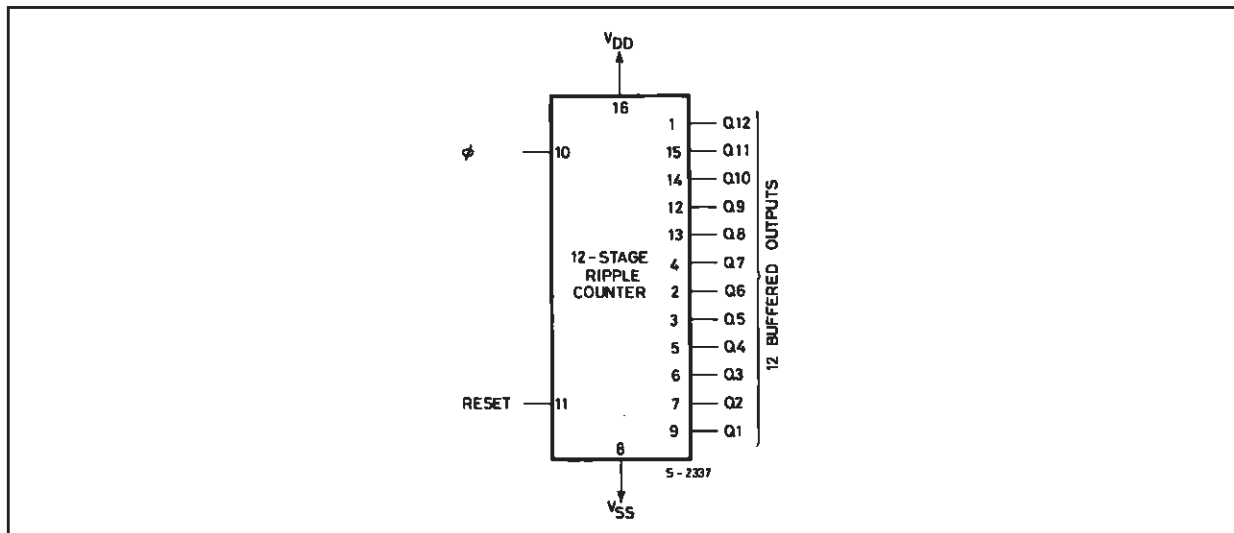
INPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
9, 7, 5, 4, 6, 13, 12, 14, 15, 1, 2, 3	Q1 to Q12	12 Buffered Outputs
11	RESET	Reset Input
10	Φ	Input Pulses
8	V_{SS}	Negative Supply Voltage
16	V_{DD}	Positive Supply Voltage

FUNCTIONAL DIAGRAM

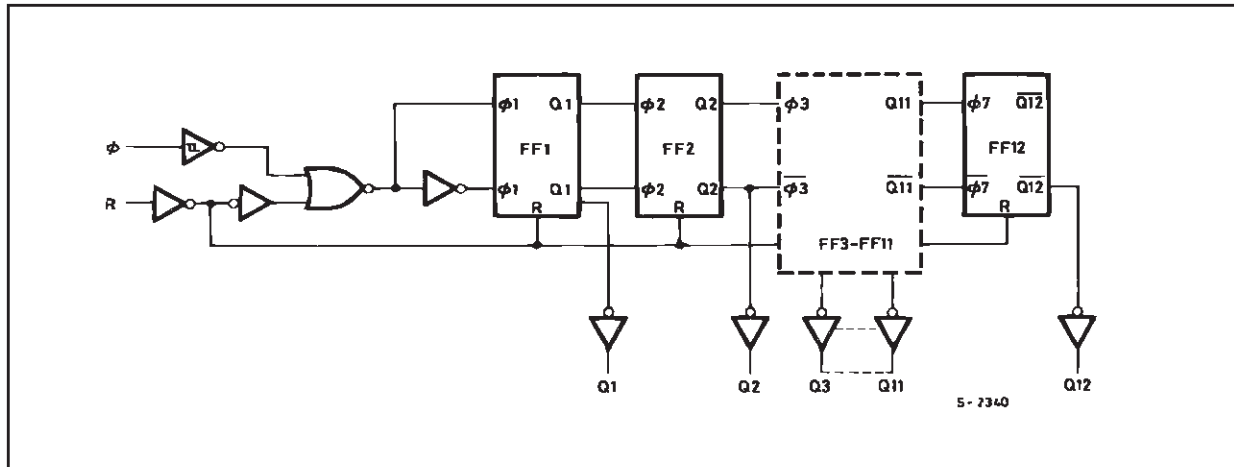


TRUTH TABLE

Φ	RESET	OUTPUT STATE
X	H	ALL OUTPUTS = "L"
	L	NO CHANGE
	L	ADVANCE TO NEXT STATE

X : Don't Care

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.5 to +22	V
V_I	DC Input Voltage	-0.5 to $V_{DD} + 0.5$	V
I_I	DC Input Current	± 10	mA
P_D	Power Dissipation per Package	200	mW
	Power Dissipation per Output Transistor	100	mW
T_{op}	Operating Temperature	-55 to +125	$^{\circ}\text{C}$
T_{stg}	Storage Temperature	-65 to +150	$^{\circ}\text{C}$

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

All voltage values are referred to V_{SS} pin voltage.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	3 to 20	V
V_I	Input Voltage	0 to V_{DD}	V
T_{op}	Operating Temperature	-55 to 125	$^{\circ}\text{C}$

DC SPECIFICATIONS

Symbol	Parameter	Test Condition				Value						Unit	
		V _I (V)	V _O (V)	I _O (μ A)	V _{DD} (V)	T _A = 25°C			-40 to 85°C		-55 to 125°C		
						Min.	Typ.	Max.	Min.	Max.	Min.		Max.
I _L	Quiescent Current	0/5			5		0.04	5		150		150	μ A
		0/10			10		0.04	10		300		300	
		0/15			15		0.04	20		600		600	
		0/20			20		0.08	100		3000		3000	
V _{OH}	High Level Output Voltage	0/5		<1	5	4.95			4.95		4.95		V
		0/10		<1	10	9.95			9.95		9.95		
		0/15		<1	15	14.95			14.95		14.95		
V _{OL}	Low Level Output Voltage	5/0		<1	5		0.05			0.05		0.05	V
		10/0		<1	10		0.05			0.05		0.05	
		15/0		<1	15		0.05			0.05		0.05	
V _{IH}	High Level Input Voltage		0.5/4.5	<1	5	3.5			3.5		3.5		V
			1/9	<1	10	7			7		7		
			1.5/13.5	<1	15	11			11		11		
V _{IL}	Low Level Input Voltage		4.5/0.5	<1	5			1.5		1.5		1.5	V
			9/1	<1	10			3		3		3	
			13.5/1.5	<1	15			4		4		4	
I _{OH}	Output Drive Current	0/5	2.5	<1	5	-1.36	-3.2		-1.1		-1.1		mA
		0/5	4.6	<1	5	-0.44	-1		-0.36		-0.36		
		0/10	9.5	<1	10	-1.1	-2.6		-0.9		-0.9		
		0/15	13.5	<1	15	-3.0	-6.8		-2.4		-2.4		
I _{OL}	Output Sink Current	0/5	0.4	<1	5	0.44	1		0.36		0.36		mA
		0/10	0.5	<1	10	1.1	2.6		0.9		0.9		
		0/15	1.5	<1	15	3.0	6.8		2.4		2.4		
I _I	Input Leakage Current	0/18	Any Input		18		$\pm 10^{-5}$	± 0.1		± 1		± 1	μ A
C _I	Input Capacitance		Any Input				5	7.5					pF

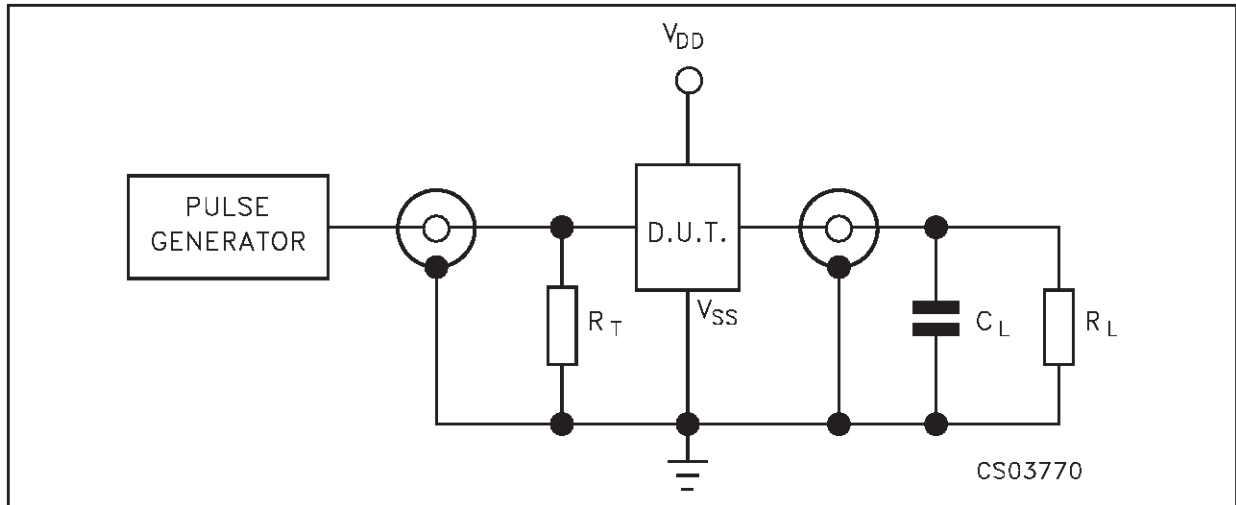
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD}=5V, 2V min. with V_{DD}=10V, 2.5V min. with V_{DD}=15V

DYNAMIC ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^{\circ}\text{C}$, $C_L = 50\text{pF}$, $R_L = 200\text{K}\Omega$, $t_r = t_f = 20\text{ ns}$)

Symbol	Parameter	Test Condition		Value (*)			Unit
		V_{DD} (V)		Min.	Typ.	Max.	
INPUT-PULSE OPERATION							
t_{PLH} t_{PHL}	Propagation Delay Time (\emptyset to Q1 Out)	5			180	360	ns
		10			80	160	
		15			65	130	
t_{PLH} t_{PHL}	Propagation Delay Time (Q_n to Q_{n+1})	5			100	200	ns
		10			40	80	
		15			30	60	
t_{THL} t_{TLH}	Transition Time	5			100	200	ns
		10			50	100	
		15			40	80	
t_W	Minimum Input Pulse Width	5			70	140	ns
		10			30	60	
		15			20	40	
t_r , t_f	Input Pulse Rise and Fall Time	5		unlimited			μs
		10					
		15					
f_{max}	Maximum Clock Input Frequency	5		3.5	7		MHz
		10		8	16		
		15		12	24		
RESET OPERATION							
t_{PHL}	Propagation Delay Time	5			140	280	ns
		10			60	120	
		15			50	100	
t_W	Minimum Reset Pulse Width	5			100	200	ns
		10			40	80	
		15			30	60	
t_{REM}	Reset Removal Time	5			175	350	ns
		10			75	150	
		15			50	100	

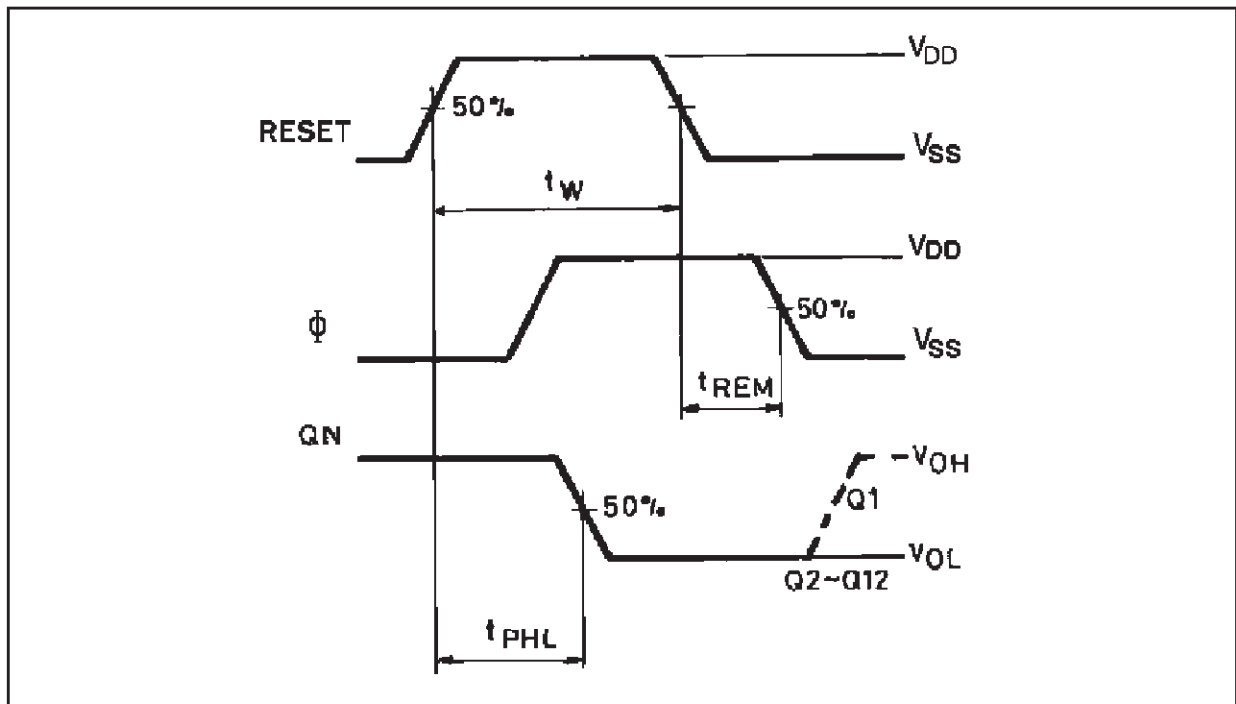
(*) Typical temperature coefficient for all V_{DD} value is 0.3 %/°C.

TEST CIRCUIT

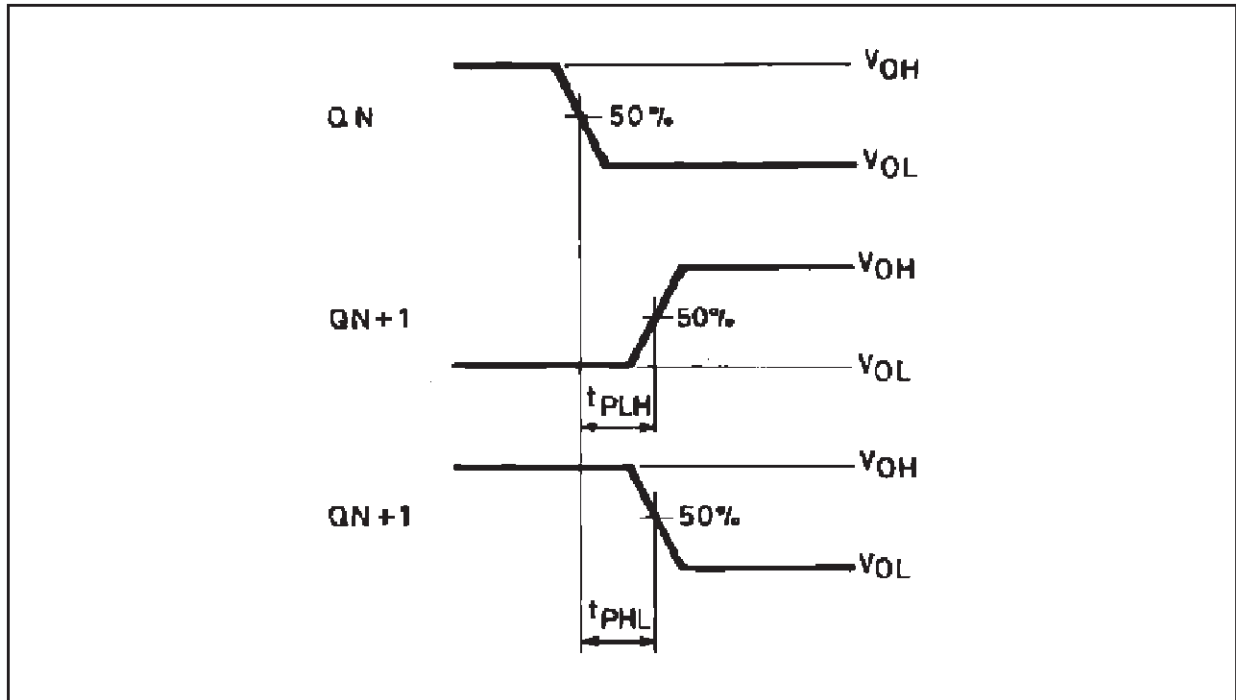
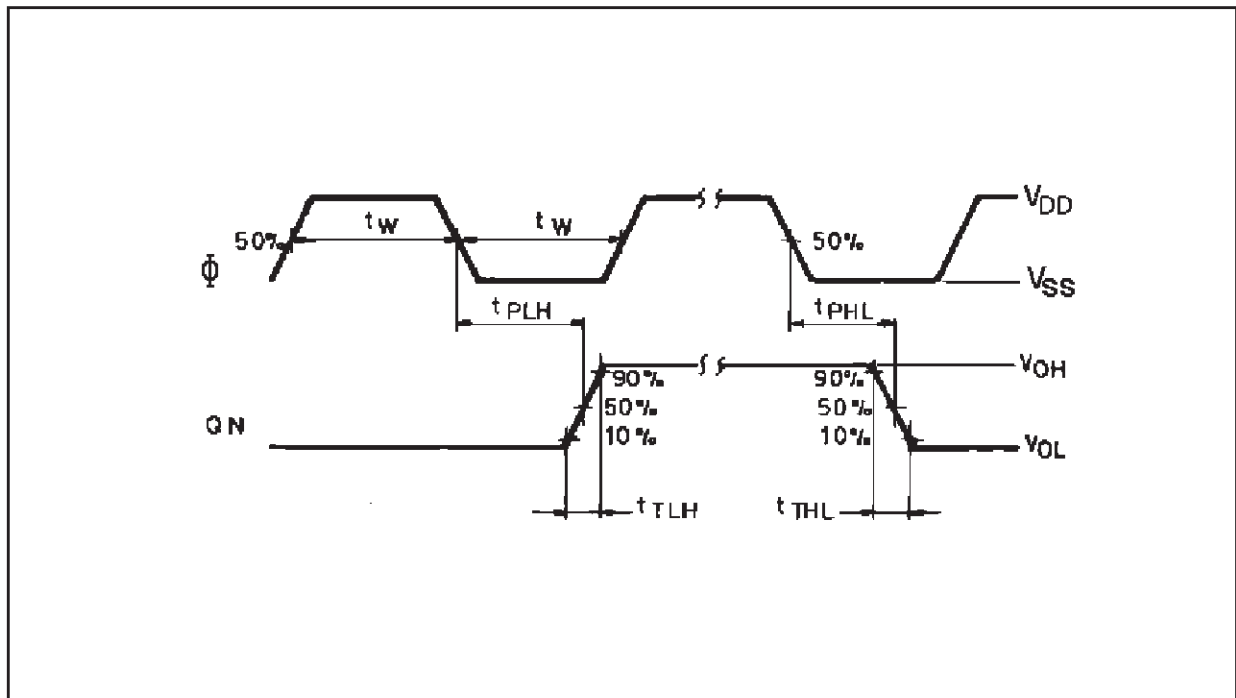


$C_L = 50\text{pF}$ or equivalent (includes jig and probe capacitance)
 $R_L = 200\text{K}\Omega$
 $R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

WAVEFORM 1 : MINIMUM PULSE WIDTH (RESET) AND REMOVAL TIME (RESET TO Φ) ($f=1\text{MHz}$; 50% duty cycle)

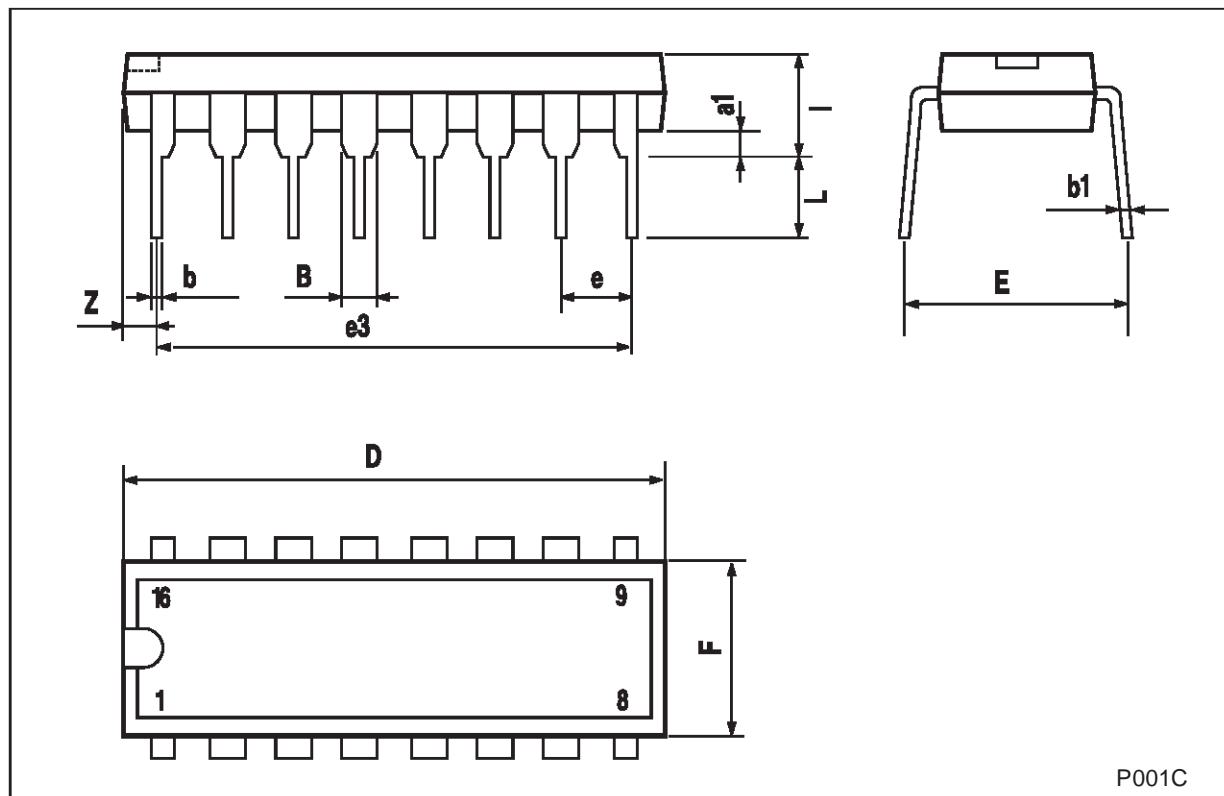


WAVEFORM 2 : PROPAGATION DELAY TIME (f=1MHz; 50% duty cycle)

WAVEFORM 3 : PROPAGATION DELAY TIME, MINIMUM PULSE WIDTH (Φ) (f=1MHz; 50% duty cycle)

Plastic DIP-16 (0.25) MECHANICAL DATA

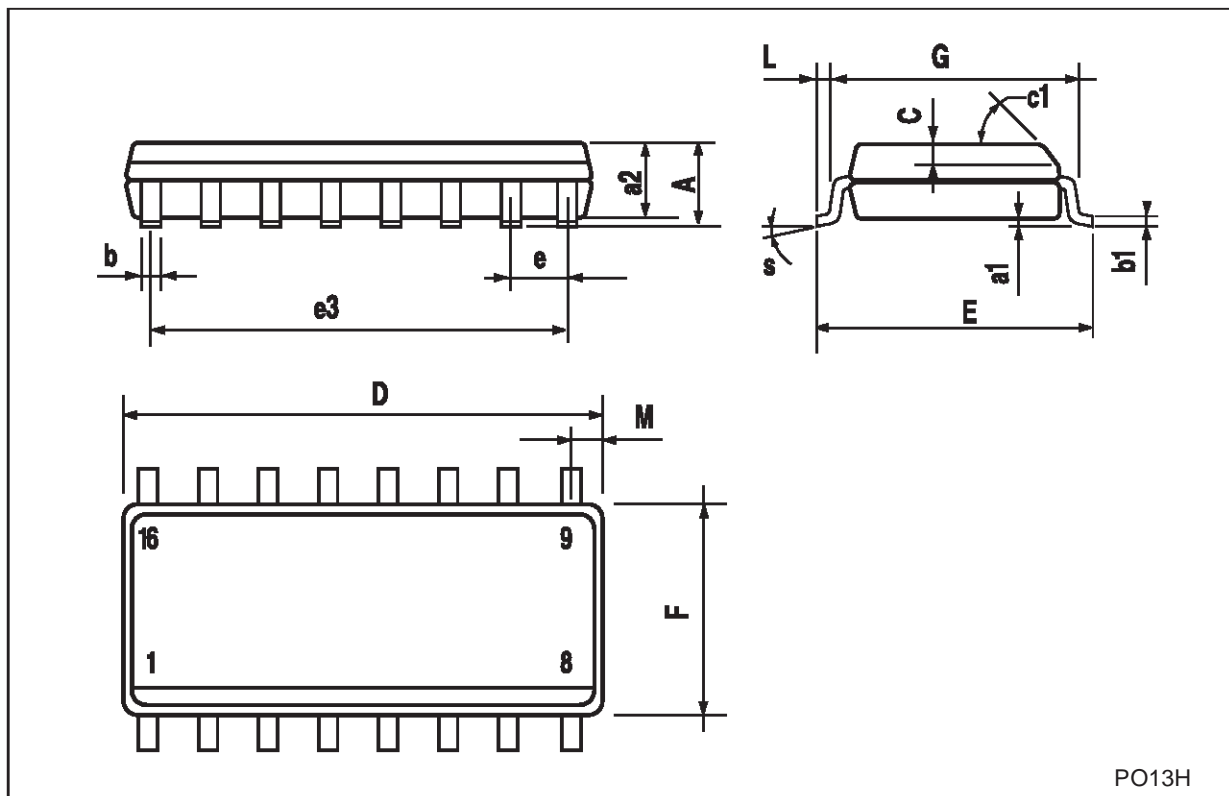
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



P001C

SO-16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



PO13H

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

© The ST logo is a registered trademark of STMicroelectronics

© 2001 STMicroelectronics - Printed in Italy - All Rights Reserved
STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - China - Finland - France - Germany - Hong Kong - India - Italy - Japan - Malaysia - Malta - Morocco
Singapore - Spain - Sweden - Switzerland - United Kingdom

© <http://www.st.com>