



2N7002HS

60 V, dual N-channel Trench MOSFET

15 December 2021

Product data sheet

1. General description

Dual N-channel enhancement mode Field-Effect Transistor (FET) in a very small SOT363 (SC-88) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Logic-level compatible
- Very fast switching
- Trench MOSFET technology
- AEC-Q101 qualified

3. Applications

- Relay driver
- High-speed line driver
- Low-side load switch
- Switching circuits

4. Quick reference data

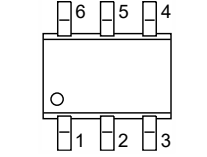
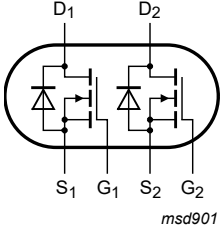
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor						
V_{DS}	drain-source voltage	$T_{amb} = 25\text{ °C}$	-	-	60	V
V_{GS}	gate-source voltage		-20	-	20	V
I_D	drain current	$V_{GS} = 10\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	320	mA
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 500\text{ mA}; T_J = 25\text{ °C}$	-	1	1.6	Ω

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 1 cm^2 .

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source 1	 <p>TSSOP6 (SOT363)</p>	 <p>msd901</p>
2	G1	gate 1		
3	D2	drain 2		
4	S2	source 2		
5	G2	gate 2		
6	D1	drain 1		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
2N7002HS	TSSOP6	plastic, surface-mounted package; 6 leads; 0.65 mm pitch; 2.1 mm x 1.25 mm x 0.95 mm body	SOT363

7. Marking

Table 4. Marking codes

Type number	Marking code ^[1]
2N7002HS	C7%

[1] % = placeholder for manufacturing site code

8. Limiting values

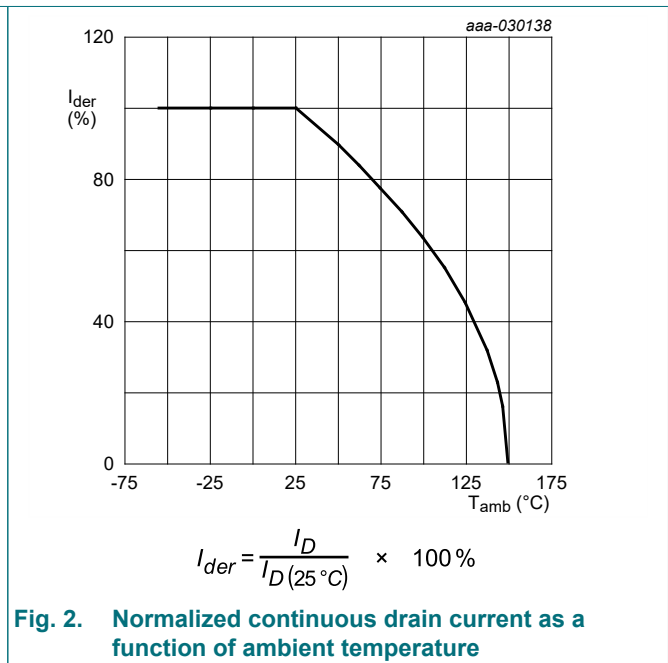
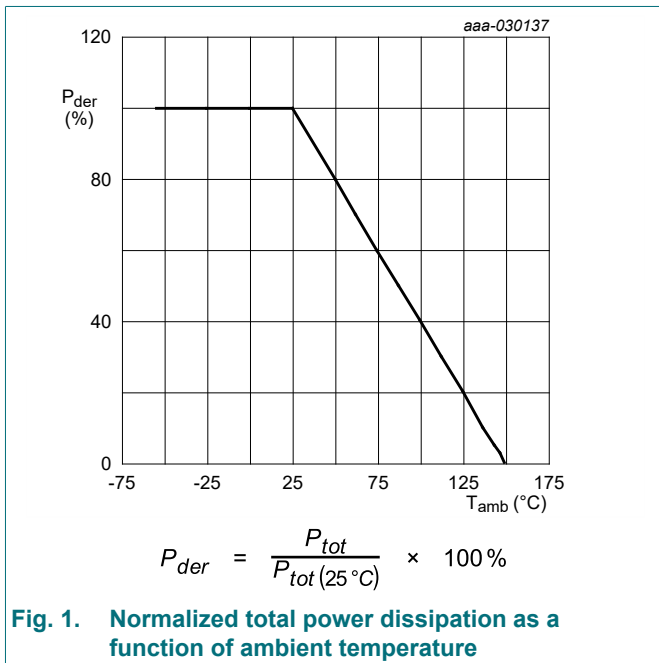
Table 5. Limiting values

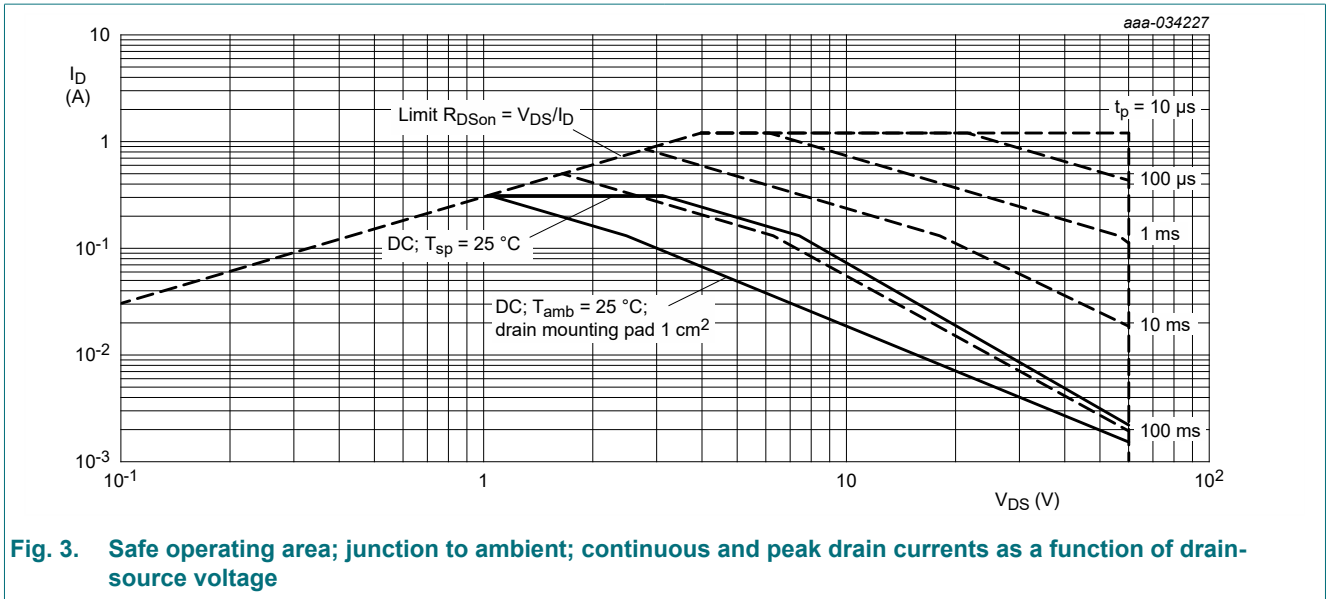
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per transistor						
V _{DS}	drain-source voltage	T _{amb} = 25 °C		-	60	V
V _{GS}	gate-source voltage			-20	20	V
I _D	drain current	V _{GS} = 10 V; T _{amb} = 25 °C	[1]	-	320	mA
		V _{GS} = 10 V; T _{amb} = 100 °C	[1]	-	200	mA
I _{DM}	peak drain current	T _{amb} = 25 °C; single pulse; t _p ≤ 10 μs		-	1.2	A
P _{tot}	total power dissipation	T _{amb} = 25 °C	[2]	-	280	mW
			[1]	-	320	mW
		T _{sp} = 25 °C		-	960	mW
Per device						
P _{tot}	total power dissipation	T _{amb} = 25 °C	[2]	-	420	mW
T _j	junction temperature			-55	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C
Source-drain diode						
I _S	source current	T _{amb} = 25 °C	[1]	-	320	mA

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 1 cm².

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.





9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per device						
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	300	K/W
Per transistor						
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	390	445	K/W
			[2]	340	390	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point		-	-	130	K/W

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 1 cm².

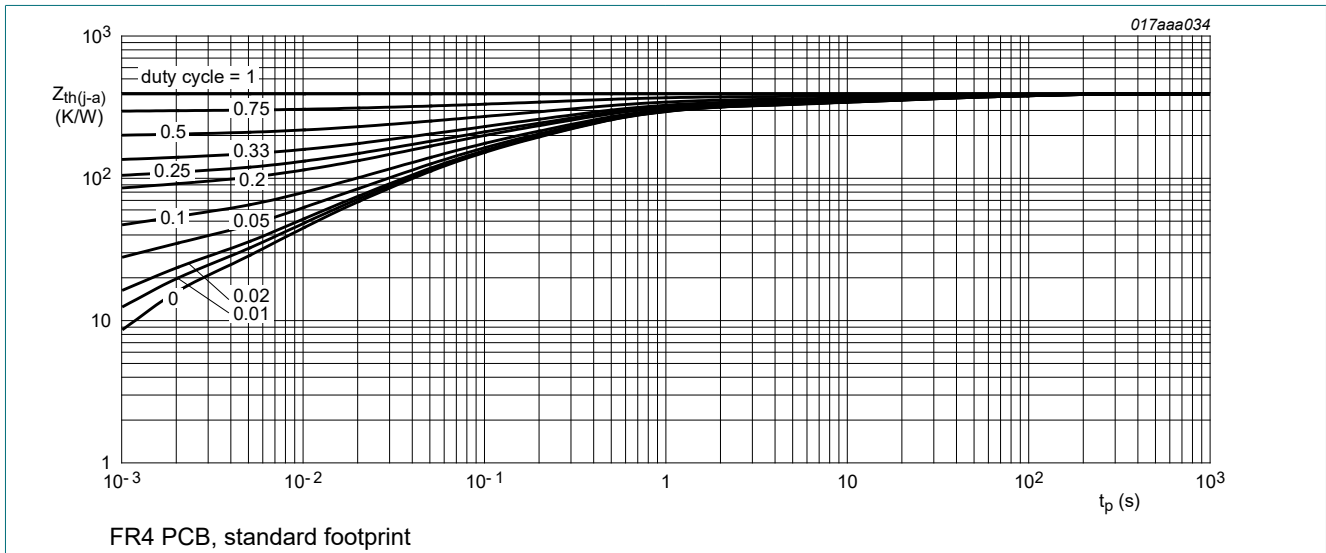


Fig. 4. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

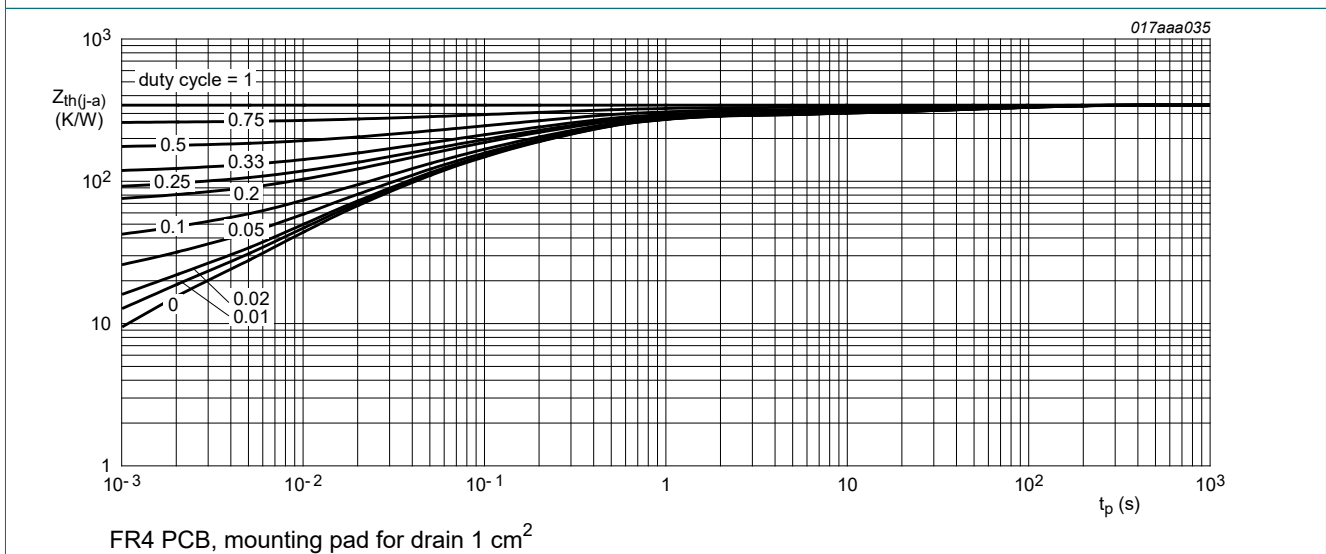


Fig. 5. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 10 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	60	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = 250 \mu A; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$	1.1	1.75	2.4	V
I_{DSS}	drain leakage current	$V_{DS} = 60 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	1	μA
		$V_{DS} = 60 V; V_{GS} = 0 V; T_j = 150 \text{ }^\circ C$	-	-	10	μA
I_{GSS}	gate leakage current	$V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	100	nA
		$V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	-100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10 V; I_D = 500 \text{ mA}; T_j = 25 \text{ }^\circ C$	-	1	1.6	Ω
		$V_{GS} = 10 V; I_D = 500 \text{ mA}; T_j = 150 \text{ }^\circ C$	-	2.1	3.3	Ω
		$V_{GS} = 5 V; I_D = 50 \text{ mA}; T_j = 25 \text{ }^\circ C$	-	1.3	2	Ω
g_{fs}	forward transconductance	$V_{DS} = 10 V; I_D = 200 \text{ mA}; T_j = 25 \text{ }^\circ C$	-	400	-	mS
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$V_{DS} = 30 V; I_D = 300 \text{ mA}; V_{GS} = 4.5 V; T_j = 25 \text{ }^\circ C$	-	0.3	0.5	nC
Q_{GS}	gate-source charge		-	0.1	-	nC
Q_{GD}	gate-drain charge		-	0.1	-	nC
C_{iss}	input capacitance	$V_{DS} = 10 V; f = 1 \text{ MHz}; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	34	-	pF
C_{oss}	output capacitance		-	7	-	pF
C_{rss}	reverse transfer capacitance		-	4	-	pF
$t_{d(on)}$	turn-on delay time		$V_{DS} = 50 V; R_L = 250 \Omega; V_{GS} = 10 V; R_{G(ext)} = 6 \Omega; T_j = 25 \text{ }^\circ C$	-	2	-
t_r	rise time	-		3	-	ns
$t_{d(off)}$	turn-off delay time	-		6	-	ns
t_f	fall time	-		4	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 115 \text{ mA}; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	0.47	0.75	1.1	V

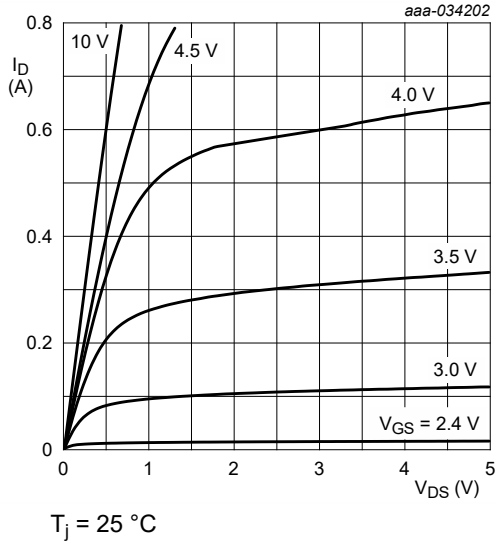


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

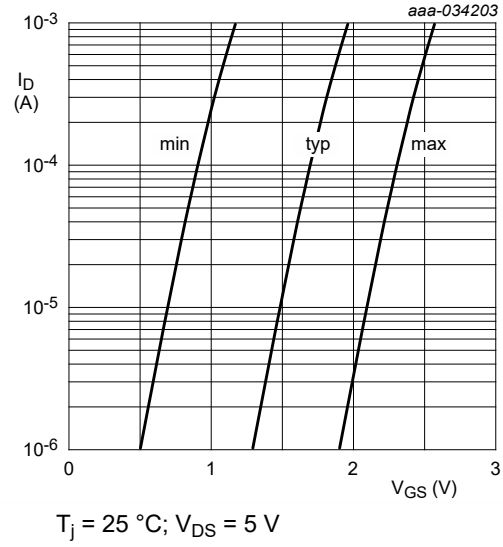


Fig. 7. Sub-threshold drain current as a function of gate-source voltage

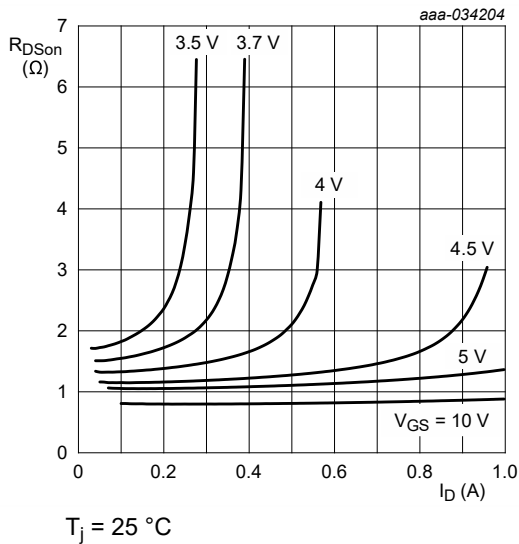


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

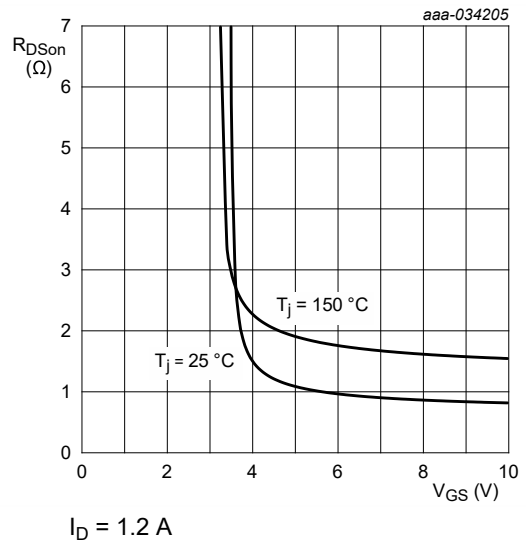


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

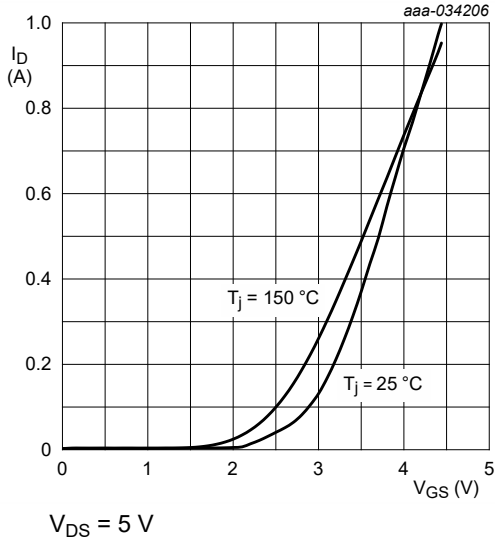


Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

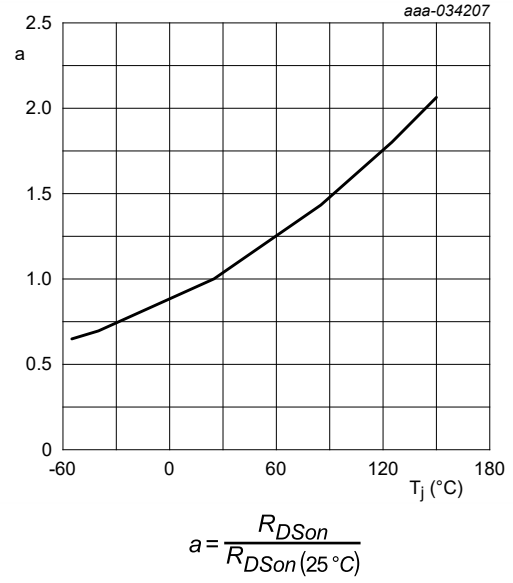


Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

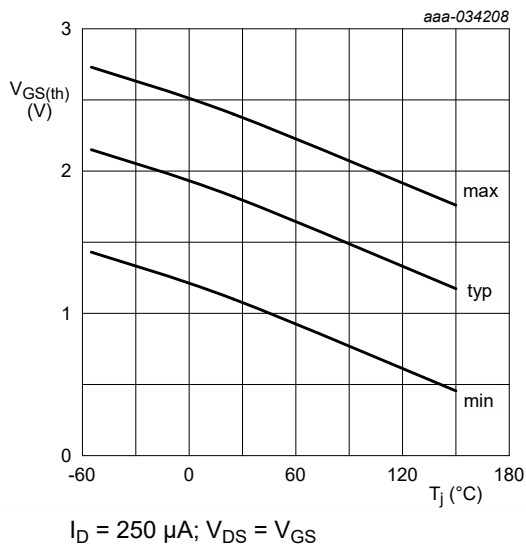


Fig. 12. Gate-source threshold voltage as a function of junction temperature

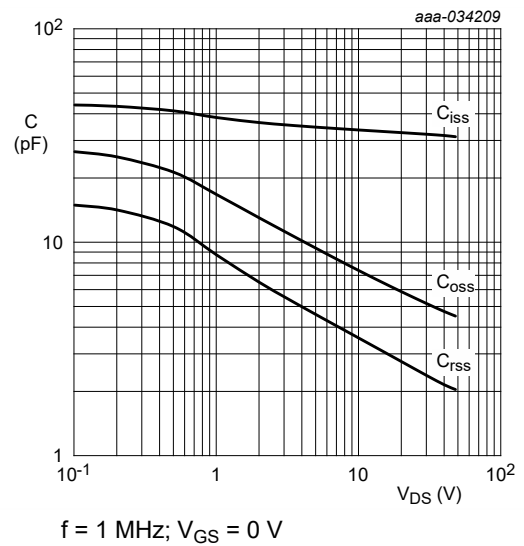
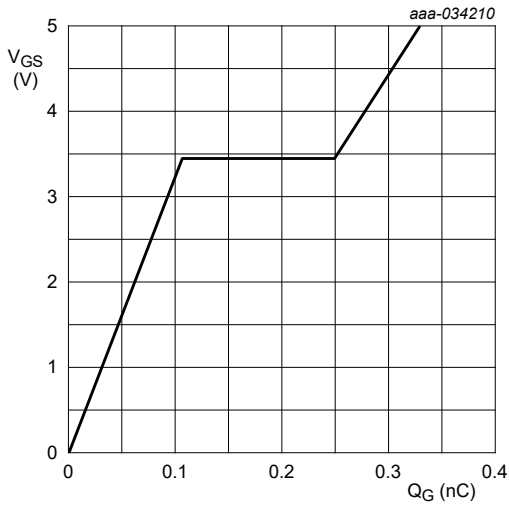


Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$I_D = 300 \text{ mA}$; $V_{DS} = 30 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$

Fig. 14. Gate-source voltage as a function of gate charge; typical values

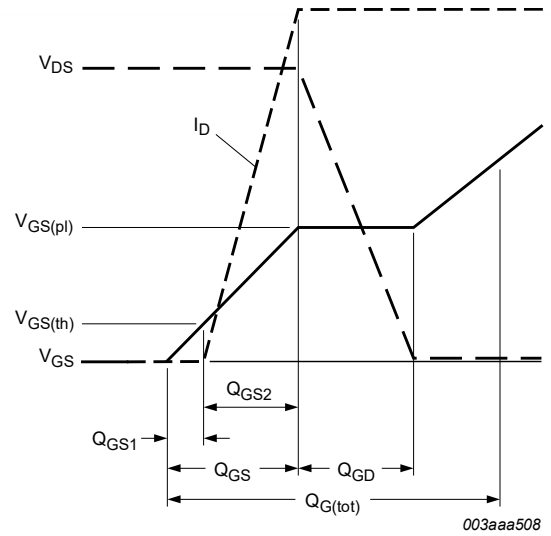
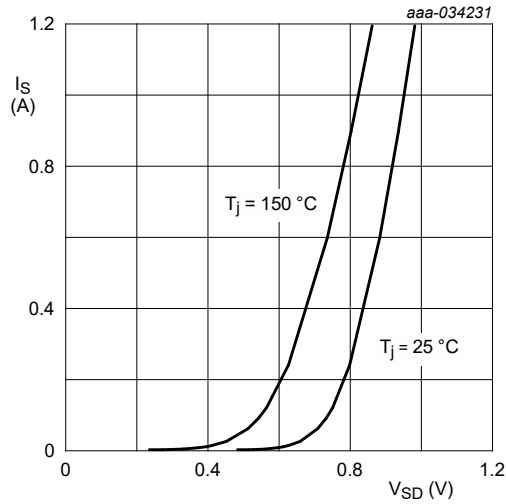


Fig. 15. Gate charge waveform definitions



$V_{GS} = 0 \text{ V}$

Fig. 16. Source current as a function of source-drain voltage; typical values

11. Test information

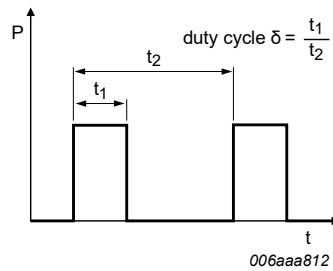


Fig. 17. Duty cycle definition

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

12. Package outline

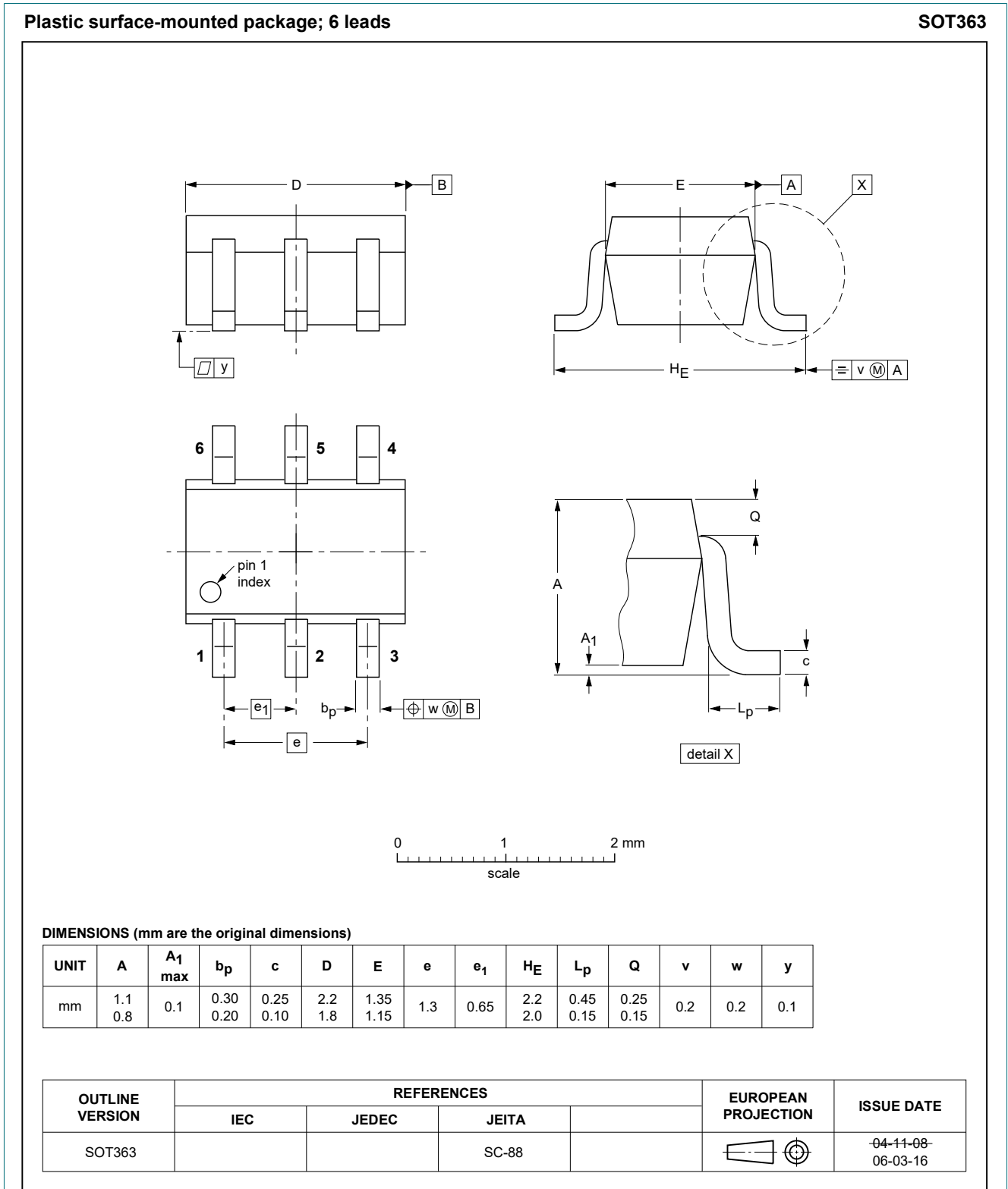


Fig. 18. Package outline TSSOP6 (SOT363)

13. Soldering

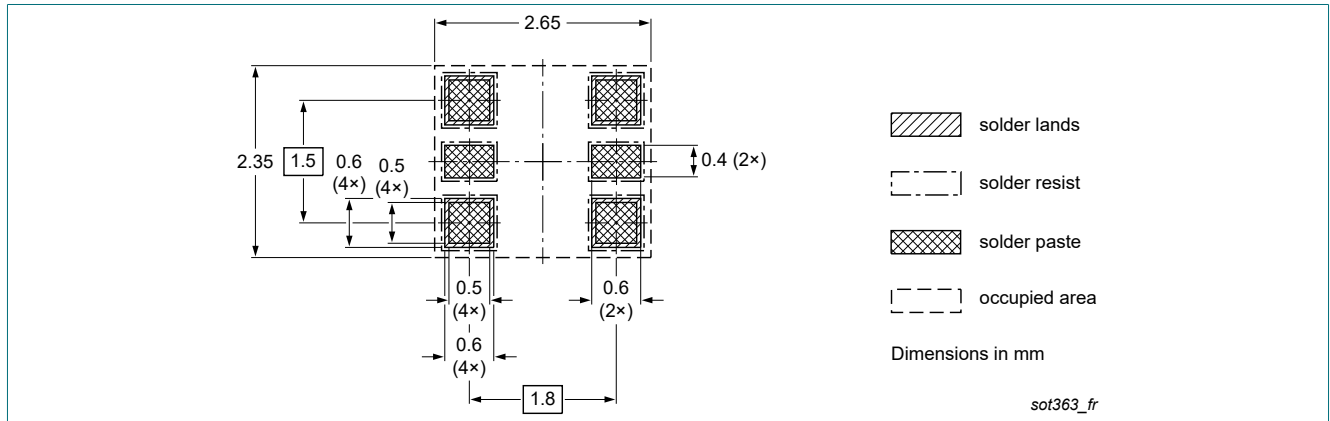


Fig. 19. Reflow soldering footprint for TSSOP6 (SOT363)

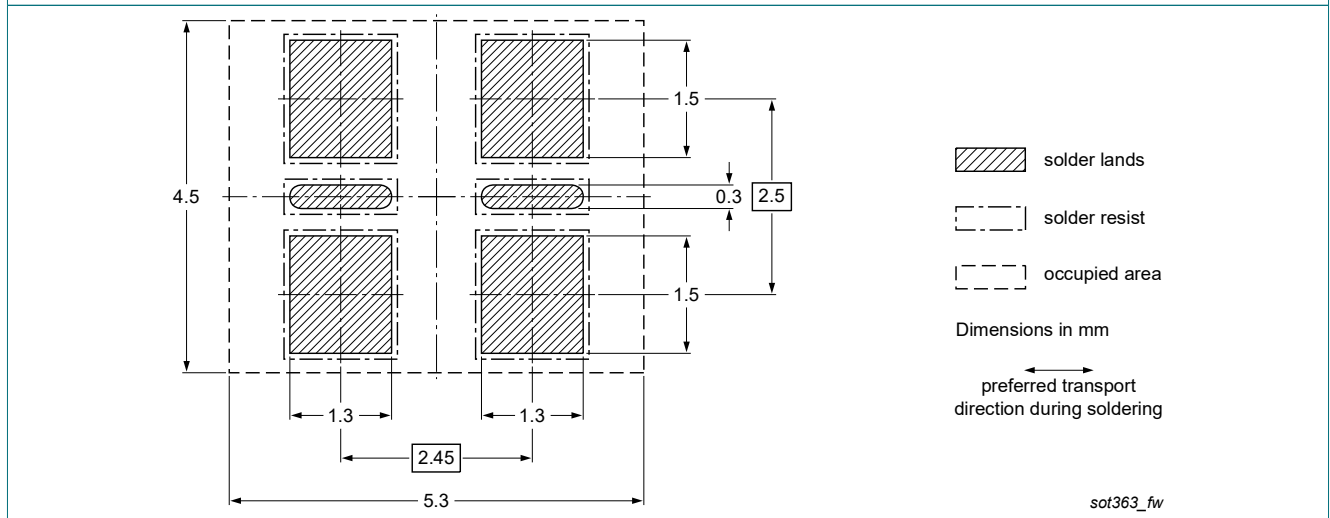


Fig. 20. Wave soldering footprint for TSSOP6 (SOT363)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
2N7002HS v.3	20211215	Product data sheet	-	2N7002HS v.2
Modifications:	• Changed values for parameters I_D and I_S			
2N7002HS v.2	20211201	Product data sheet	-	2N7002HS v.1
2N7002HS v.1	20211119	Preliminary data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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