EVBUM2281/D

KAI-11002 Imager Board User's Manual

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EVAL BOARD USER'S MANUAL

Description

The KAI−11002 Imager Evaluation Board, referred to in this document as the Imager Board, is designed to be used as part of a two−board set, in conjunction with a Timing Generator Board. ON Semiconductor offers an Imager Board / Timing Generator Board package that has been designed and configured to operate with the KAI−11002 Image Sensor.

The Timing Generator Board generates the timing signals necessary to operate the CCD, and provides the power required by the Imager Board. The timing signals, in LVDS format, and the power, are provided to the Imager Board via the interface connector (J1). In addition, the Timing Generator Board performs the processing and digitization of the analog video output of the Imager Board.

The KAI−11002 Imager Board has been designed to operate the KAI−11002 with the specified performance at 30 MHz pixel clocking rate and nominal operating conditions. (See the KAI−11002 performance specifications for details).

For testing and characterization purposes, the KAI−11002 Imager Board provides the ability to adjust many of the CCD bias voltages and CCD clock level voltages by adjusting potentiometers on the board. The Imager Board provides the means to modify other device operating parameters (CCD reset clock pulse width, VSS bias voltage) by populating components differently on the board.

INPUT REQUIREMENTS

Table 1. POWER REQUIREMENTS

Power Supplies	Minimum	Typical	Maximum	Units
+5 V_MTR Supply	4.9	5.0	5.1	V
		1400		mA
−5 V_MTR Supply	−5.1	−5.0	−4.9	V
		200		mA
VPLUS Supply	18	20	21	V
		175		mA
VMINUS Supply	−21	−20	−18	V
		150		mA

Table 2. SIGNAL LEVEL REQUIREMENTS

Input Signals (LVDS)	V_{min}	$V_{threshold}$	V_{max}	Units	Comments
H1A (±)	0	±0.1	2.4	V	H1A clock
H1B (±)	0	±0.1	2.4	V	H1B clock
H2A (±)	0	±0.1	2.4	V	H2A clock
H2B (±)	0	±0.1	2.4	V	H2B clock
FDG	0	±0.1	2.4	V	Fast Dump clock
R (±)	0	±0.1	2.4	V	Reset clock
V1 (±)	0	±0.1	2.4	V	V1 clock
V2 (±)	0	±0.1	2.4	V	V2 clock
V2B (±)	0	±0.1	2.4	V	V2B clock
V3RD (±)	0	±0.1	2.4	V	V2 Clock 3rd level
VES (±)	0	±0.1	2.4	V	Electronic Shutter
AMP_ENABLE (±)	0	±0.1	2.4	V	Output Amplifier Enable

ARCHITECTURE OVERVIEW

The following sections describe the functional blocks of the KAI−11002 Imager Board (Refer to Figure 1).

Power Filtering and Regulation

Power is supplied to the Imager Board via the J1 interface connector. The power supplies are de−coupled and filtered with ferrite beads and capacitors to suppress noise. Voltage regulators are used to create the +15 V and –15 V supplies from the VPLUS and VMINUS supplies.

LVDS Receivers / TTL Buffers

LVDS timing signals are input to the Imager Board via the J1 interface connector. These signals are shifted to TTL levels before being sent to the CCD clock drivers.

CCD Pixel−Rate Clock Drivers (H1, H2 & Reset Clocks)

The pixel rate CCD clock drivers utilize two fast switching transistors that are designed to translate TTL−level input clock signals to the voltage levels required by the CCD. The high and low voltage levels of the CCD clocks are set by potentiometers buffered by operational amplifiers configured as voltage followers.

For the H1A and H2A clock drivers, which require larger amounts of drive current due to the larger capacitive load presented by the CCD, the current source of the high and low voltage levels is a high current (up to 600 mA) transistor configured as an emitter follower. For better current drive capability, an extra pair of transistors may be populated in parallel. For the other clock drivers (H1L, RESET) that have much smaller loads, the drive current is supplied by the buffer op−amp itself.

Because the H1 and H2 clock rails are adjusted independently, the H1B and H2B clock driver voltage rails are selected by using four jumpers (E1−E4). In single output mode, the H1B and H2B rails are connected to the H1A and H2A rails, respectively. In dual output mode, the H1B and H2B rails should be connected to the H2A and H1A rails, respectively. See Table 5 for details.

H1L CCD Timing Adjustment Potentiometers

Minor timing adjustments can be made to the H1L CCD right and left clock positions using the delay adjust potentiometers R180 and R181. Each potentiometer, along with a capacitor, forms an RC network that acts to delay the position of the H1L clock with respect to the H1A clock.

Reset Clock One−Shot

The pulse width of the RESET_CCD clock is set by a programmable One−Shot. The One−Shot can be configured to provide a RESET_CCD clock signal with a pulse width from 5 ns to 15 ns.

CCD VCLK Drivers

The vertical clock (VCLK) drivers consist of MOSFET driver IC's. These drivers are designed to translate the TTL−level clock signals to the voltage levels required by the CCD. The high, middle, and low voltage levels of the vertical clocks are set by potentiometers buffered by operational amplifiers configured as voltage followers. The current sources for these voltage levels are high current (up to 600 mA) transistors. The V2_CCD high level clock voltage is switched from V_MID to V_HIGH once per frame to transfer the charge from the photodiodes to the vertical CCDs. See Table 6 and Table 7 for vertical clocking voltage level options.

CCD FDG Voltages

The Fast Dump Gate (FDG) driver is a transistor that will switch the voltage on the FDG pin of the CCD from FDG_LOW to FDG_HIGH during Fast Dump Gate operation. When not in operation, or when the Fast Dump Gate feature is not being utilized, the FDG pin of the CCD is held at FDG_LOW. The FDG_HIGH and FDG_LOW voltage levels of the FDG driver are set by resistor divider circuits, and are buffered by operational amplifiers configured as voltage followers.

VES Circuit

The quiescent CCD substrate voltage (VSUB) is set by a potentiometer. For electronic shutter operation, the VES signal drives a transistor amplifier circuit which AC−couples the voltage difference between the VPLUS and VMINUS supplies onto the Substrate voltage. This creates the necessary potential to clear all charge from the photodiodes, thereby acting as an electronic shutter to control exposure.

CCD Bias Voltages

The CCD bias voltages are set by potentiometers, buffered by operational amplifiers configured as voltage followers. The bias voltages are de−coupled at the CCD pin.

Emitter−Follower

The VOUT_CCD signals are buffered using bipolar junction transistors in the emitter−follower configuration. These circuits also provide the necessary 5 mA current sink for the CCD output circuits.

CCD Image Sensor

This evaluation board supports the KAI−11002 Image Sensor.

Line Drivers

The buffered VOUT_CCD signals are AC−coupled and driven from the Imager Board by operational amplifiers in a non−inverting configuration. The operational amplifiers are configured to have a gain of 2, to correctly drive 75 Ω video coaxial cabling from the SMB connectors.

OPERATIONAL SETTINGS

The Imager board is configured to operate the KAI−11002 Image Sensors under the following operating conditions:

DC Bias Voltages

The following voltages are fixed, or adjusted with a potentiometer as noted. The nominal values listed in Table 3 were correct at the time of this document's publication, but may be subject to change; refer to the KAI−11002 device specification.

Table 3. DC BIAS VOLTAGES

Description	Symbol	Min	Nominal	Max	Units	Potentiometer	Notes
Left Output Amplifier Supply	VDDL		15.0		V		
Right Output Amplifier Supply	VDDR		15.0		V		1
Reset Drain	VRD	6.7	12.0	13.5	V	R15	3
ESD Protection	ESD		−9.0		V		
Substrate	VSUB	8.5	TBD	15.0	V	R18	3
Output Gate Left	VOGL	−7.5	−2.5	−0.4	V	R11	2, 3
Output Gate Right	VOGR	−7.5	−2.5	−0.4	V	R7	2, 3
Ground, P−well	GND		0.0		V		

1. If the CCD is to be operated in single output mode only (VOUT_LEFT) the unused output amplifier supply can be tied to ground to conserve power by not populating R71, R72 and C76 and by replacing C75 with a 0 Ω resistor.
2. The Output Gate signals VOGL and VOGR may be controlled independently, or, by installing R28 and R33 and removing R29, may be set to the same potential, controlled by R11.
3. The Min and Max voltages in the table indicate the imager board potentiometer adjustable voltage range. These values may exceed the specified CCD operating conditions. See the KAI−11002 device specification for details.

Clock Voltages

The following clock voltage levels are fixed, or adjusted with a potentiometer as noted. The nominal values listed in Table 4 were correct at the time of this document's publication, but may be subject to change; refer to the KAI−4011 / KAI−4021 /KAI−04022 device specification.

Table 4. CLOCK VOLTAGES

Description	Symbol	Level	Min	Nom	Max	Unit	Potentiometer	Notes
Horizontal CCD Clock − Phase 1A	H1A_CCD	Low	−7.5	−4	−0.8	V	R121	4
		High	0.4	2	7.5	V	R140	4
Horizontal CCD Clock − Phase 1B	H1B_CCD	Low	−7.5	−4	−0.8	V	R121	5, 10
		High	0.4	2	7.5	V	R140	5, 10
HCCD Last Gate Clock − Phase 1L	H1L_CCD	Low	−7.5	−4	−0.8	V	R95	6
		High	0.4	2	7.5	V	R80	6
Horizontal CCD Clock − Phase 2A	H2A_CCD	Low	−7.5	−4	−0.8	V	R121	7
		High	0.4	2	7.5	V	R140	7
Horizontal CCD Clock − Phase 2B	H2B_CCD	Low	−7.5	−4	−0.8	V	R121	8, 10
		High	0.4	2	7.5	V	R140	8, 10

4. Connected to CCD pins 8, 9, and 13 (H1SL, H1BL and H1SR)
5. Connected to CCD pin 12 (H1BR)
6. H1L Left connected to CCD pin 5 (H1BINL). H1L Right connected to CCD pin 16 (H1BINR)
7. Connected to CCD pins 7, 10, and 14 (H2SL, H2BL and H2SR)
8. Connected to CCD pin 11 (H2BR)
9. Four level vertical clocking mode only. See Table 6 and Table 7 Vertical Clocking Modes. Not applicable for all devices; see KAI−11002 device specifications.
10. H1B and H2B high and low clock voltages are connected either to H1A High and Low or H2A high and low depending on the output mode of operation. See Table 5.

Table 4. CLOCK VOLTAGES

Description	Symbol	Level	Min	Nom	Max	Unit	Potentiometer	Notes
Vertical CCD Clock − Phase 1	V1_CCD	−15 V		−15.0		V		9
		Low	−14	−9	−1	V	R40	
		Mid	−2.5	0	0	V	R66	
Vertical CCD Clock − Phase 2	V2_CCD	−15 V		−15.0				9
		Low	−14	−9	−1	V	R40	
		Mid	−2.5	0	0	V	R66	
		High	4	8	11	V	R48	
Reset Clock	RESET_CCD	Low	−7	−3.5	−1	V	R166	
		High	1	1.5	7	V	R154	
Fast Dump Clock	FDG_CCD	Low		−9		V		
		High		5		V		

4. Connected to CCD pins 8, 9, and 13 (H1SL, H1BL and H1SR)
5. Connected to CCD pin 12 (H1BR)
6. H1L Left connected to CCD pin 5 (H1BINL). H1L Right connected to CCD pin 16 (H1BINR)
7. Connected to CCD pins 7, 10, and 14 (H2SL, H2BL and H2SR)
8. Connected to CCD pin 11 (H2BR)
9. Four level vertical clocking mode only. See Table 6 and Table 7 Vertical Clocking Modes. Not applicable for all devices; see KAI−11002 device specifications.
10. H1B and H2B high and low clock voltages are connected either to H1A High and Low or H2A high and low depending on the output mode of operation. See Table 5.

Table 5. HCLK JUMPER SETTINGS

Jumper	Setting	Clock Level	Voltage Set To	Notes
E1	1OUT	H2B_LOW	H1A LOW	Default
E1	2OUT	H2B_LOW	H2A LOW	
E2	1OUT	H1B_HIGH	H2A HIGH	Default
E2	2OUT	H1B_HIGH	H1A HIGH	
E3	1OUT	H2B_HIGH	H1A HIGH	Default
E3	2OUT	H2B_HIGH	H2A HIGH	
E4	1OUT	H1B_LOW	H2A LOW	Default
E4	2OUT	H1B_LOW	H1A LOW	

Table 6. V1 VERTICAL CLOCKING MODES

V1_CCD Voltage	V1_TTL	V2B_TTL	Notes
V_MID	0	0	
V_MID	0	1	
V_LOW	1	0	
−15 V	1	1	Four level vertical clocking mode only. Not applicable for all devices, see device specifications.

Table 7. V2 VERTICAL CLOCKING MODES

V2_CCD Voltage	V3RD_TTL	V2_TTL	V2B_TTL	Notes
V_MID	0	0	0	
V_HIGH	1	0	0	
V_LOW	0	1	0	
V_LOW	1	1	0	
V_MID	0	0	1	
V_HIGH	1	0	1	
−15 V	0	1	1	Four level vertical clocking mode only. Not applicable for all devices, see device specifications.
−15 V	1	1	1	Four level vertical clocking mode only. Not applicable for all devices, see device specifications.

Reset Clock Pulse Width

The pulse width of RESET_CCD is set by configuring P[2..0], the inputs to the programmable one−shot. P[2..0] can be tied high or low to achieve the desired pulse width by populating the resistors R161−164 accordingly.

Table 8. RESET CLOCK PULSE WIDTH

Pulse Width	P0	P1	P2	R161	R162	R163	R164	Notes
15 ns	0	0	0	IN	IN	OUT	OUT	
5 ns	1	0	0	IN	OUT	IN	OUT	Default Setting
7.5 ns	0	1	0	OUT	IN	OUT	IN	
10 ns	1	1	0	OUT	OUT	IN	IN	

BLOCK DIAGRAM AND PERFORMANCE DATA

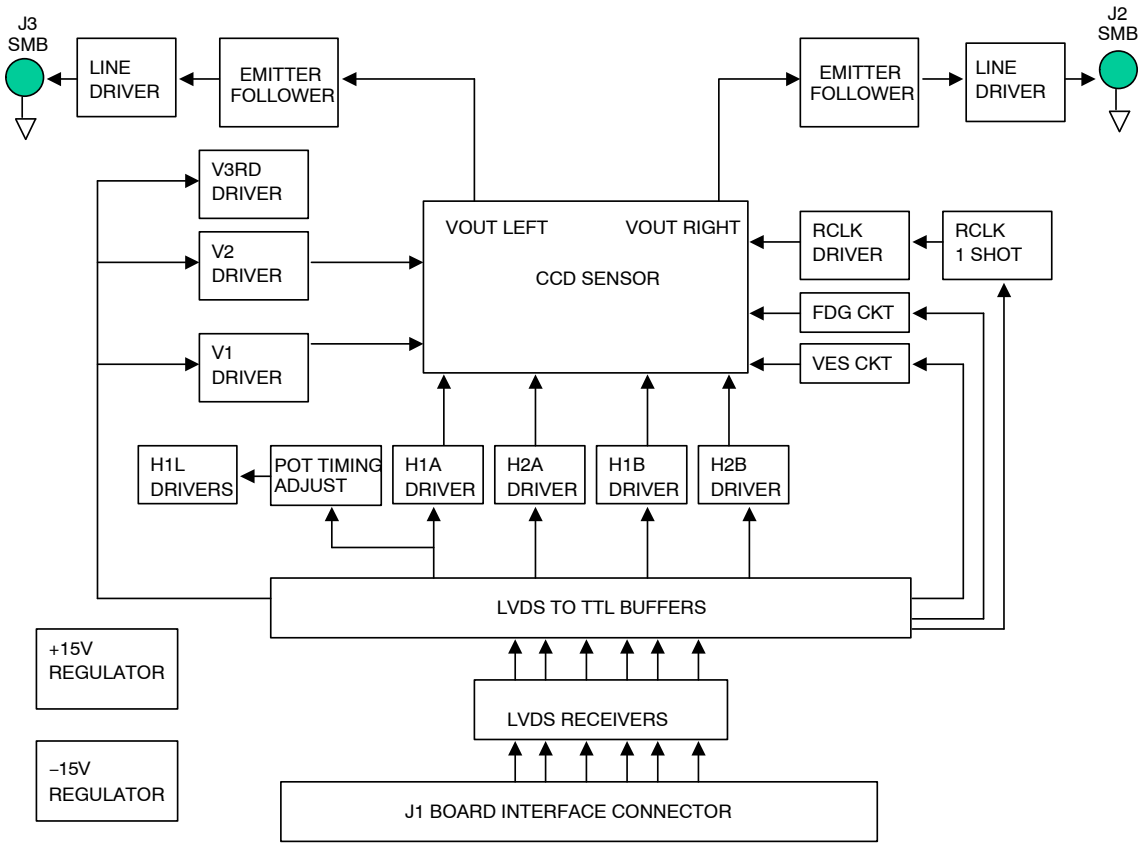

Figure 1. KAI−11002 Imager Board Block Diagram

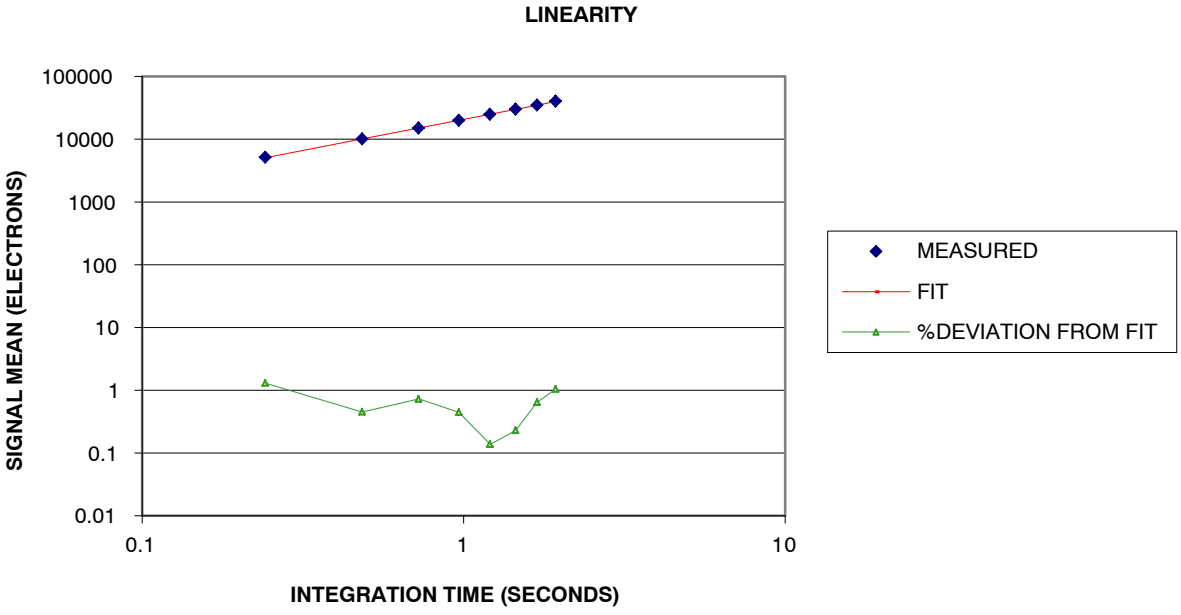

Figure 2. Measured Performance − Linearity

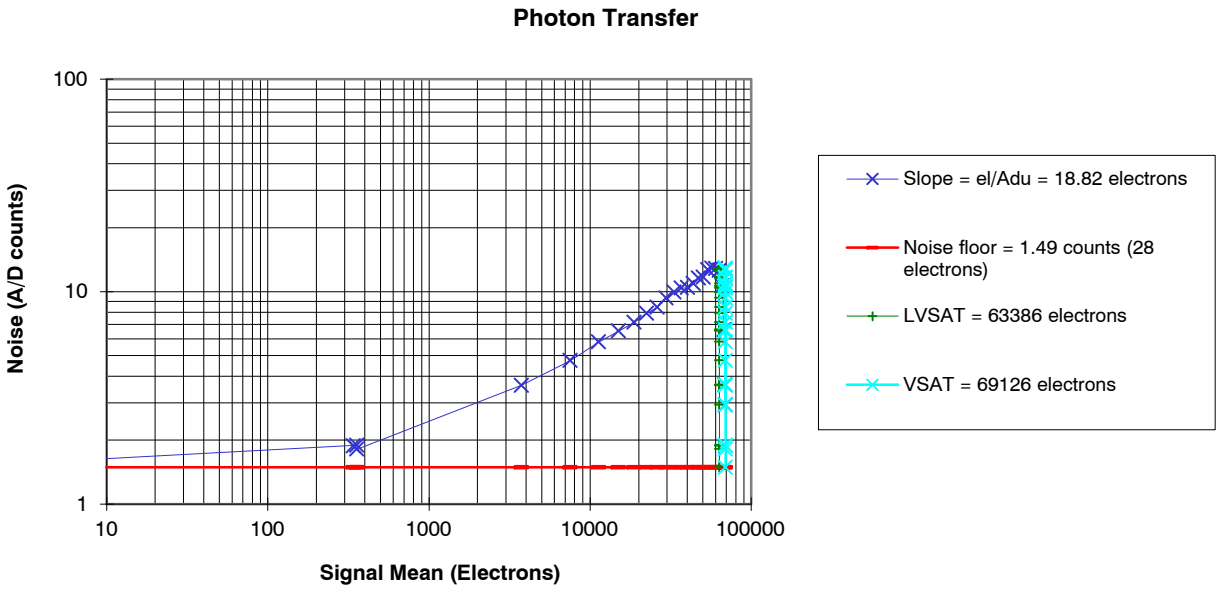

Figure 3. Measured Performance – Dynamic Range and Noise Floor

CONNECTOR ASSIGNMENTS AND PINOUTS

SMB Connectors J2 and J3

The emitter−follower buffered CCD_VOUT signals are driven from the Imager Board via the SMB connectors J2 and J3. Coaxial cable with a characteristic impedance of 75 Ω should be used to connect the imager board to the Timing Generator Board to match the series and terminating resistors used on these boards.

Table 9. J1 INTERFACE CONNECTOR PIN ASSIGNMENTS

Pin	Signal	Pin	Signal
1	N.C.	2	N.C.
3	AGND	4	AGND
5	VES+	6	VES−
7	AGND	8	AGND
9	FDG+	10	FDG−
11	AGND	12	AGND
13	V3RD+	14	V3RD−
15	AGND	16	AGND
17	V2B+	18	V2B−
19	AGND	20	AGND
21	V2+	22	V2−
23	AGND	24	AGND
25	V1+	26	V1−
27	AGND	28	AGND
29	R+	30	R−
31	AGND	32	AGND
33	H2B+	34	H2B−
35	AGND	36	AGND
37	H2A+	38	H2A−
39	AGND	40	AGND
41	H1B+	42	H1B−
43	AGND	44	AGND
45	H1A+	46	H1A−
47	N.C.	48	N.C.
49	AGND	50	AGND
51	N.C.	52	N.C.
53	VMINUS_MTR	54	VMINUS_MTR
55	N.C.	56	N.C.
57	AGND	58	AGND
59	AMP_ENABLE+	60	AMP_ENABLE−
61	−5 V_MTR	62	−5 V_MTR
63	N.C.	64	N.C.
65	AGND	66	AGND
67	N.C.	68	N.C.
69	+5 V_MTR	70	+5 V_MTR
71	N.C.	72	N.C.
73	AGND	74	AGND
75	N.C.	76	N.C.
77	VPLUS_MTR	78	VPLUS_MTR
79	N.C.	80	N.C.

Warnings and Advisories

ON Semiconductor is not responsible for customer damage to the Imager Board or Imager Board electronics. The customer assumes responsibility and care must be taken when probing, modifying, or integrating the ON Semiconductor Evaluation Board Kits.

When programming the Timing Board, the Imager Board must be disconnected from the Timing Board before power is applied. If the Imager Board is connected to the Timing Board during the reprogramming of the Altera PLD, damage to the Imager Board will occur.

Purchasers of an Evaluation Board Kit may, at their discretion, make changes to the Timing Generator Board firmware. ON Semiconductor can only support firmware developed by, and supplied by, ON Semiconductor. Changes to the firmware are at the risk of the customer.

Ordering Information

Please address all inquiries and purchase orders to:

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