

M74HC40103

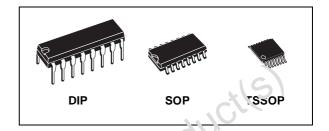
8 STAGE PRESETTABLE SYNCHRONOUS DOWN COUNTER

- HIGH SPEED : f_{MAX} = 38MHz (TYP.) at V_{CC} = 6V
- LOW POWER DISSIPATION: $I_{CC} = 4\mu A(MAX.)$ at $T_A = 25^{\circ}C$
- HIGH NOISE IMMUNITY: V_{NIH} = V_{NIL} = 28 % V_{CC} (MIN.)
- SYMMETRICAL OUTPUT IMPEDANCE: |I_{OH}| = I_{OL} = 4mA (MIN)
- BALANCED PROPAGATION DELAYS:
 t_{PLH} ≅ t_{PHL}
- WIDE OPERATING VOLTAGE RANGE: V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 40103



The M74HC40103 is an high speed CMOS 8-STAGE PRESETTABLE SYNCHRONOUS DOWN COUNTER fabricated with silicon gate C^2 MOS technology.

The HC40103 consists of an 8 stage synchronous down counter with a single output which is active when the internal count is zero. The HC40103 contains a single 8-bit binary counter. This device has control inputs for enabling or disabling the clock, for clearing the counter to its maximum count, and for presetting the counter either synchronously or asynchronously. All control inputs and the CARRY-OUT / ZERO DETECT output are active low logic. In normal operation the counter is decremented by one count on each positive transition of the CLOCK. Counting is



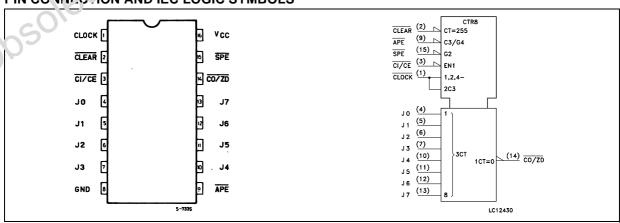
ORDER CODES

PACKAG E	TUSE	7.5.7
DIP	∿74¦ íC40103B1R	
SOP	M74HC40103M1R	N 74HC40103RM13TR
73500	240	M74HC40103TTR

inhibited when the CARRY-IN / COUNTER ENABLE (CLCE) input is high. The CARRY-OUT / ZERO-L'ETECT (CO/ZD) output goes low when the count reaches zero if the CI/CE input is low, and remains low for one full clock period. When the SYNCHRONOUS PRESET-ENABLE (SPE) input is low, data at the J input is clocked into the counter on the next positive clock transition regardless of the state of the CI/CE input.

When the ASYNCHRONOUS PRESET-ENABLE (APE) input is low, data at the J inputs is asynchronously forced into the counter regardless of the state of the SPE CI/CE or CLOCK inputs. J input J0-J7 represent a singular 8-bit binary word. When the CLEAR, CLR input is low, the counter is asynchronously cleared to its maximum count

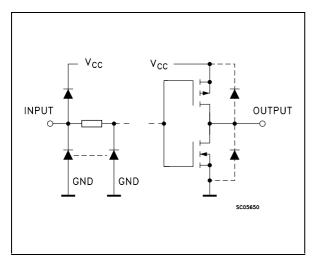
PIN CONNECTION AND IEC LOGIC SYMBOLS



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(255₁₀) regardless of the state of any other input. The precedence relationship between control input is indicated in the truth table. If all control inputs are high at the time of zero count, the counters will jump to the maximum count giving a

INPUT AND OUTPUT EQUIVALENT CIRCUIT



counting sequence of 256 clock pulses long. The HC40103 may be cascaded using the CI/CE input and the CO/ZD output, in either a synchronous or ripple mode. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

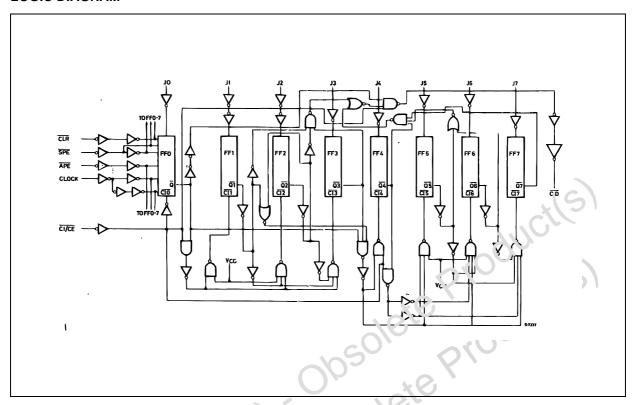
PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	CLOCK	Clock Input (LOW to HIGH edge triggered)
2	CLEAR	Asynchronous Macter Reset Input (Active Low)
3	CI/CE	Terminal Exacte input
4, 5, 6, 7, 10, 11, 12, 13	J0 to J9	Jam Inputs
9	ĀPĒ	Prachronous Preset Enable Inputs(Active Low)
14	CO / Z D	Terminal Count Output (Active Low)
15	SPE	Synchronous Preset Enable Input (Active Low)
٩	GND	Ground (0V)
16	Vcc	Positive Supply Voltage

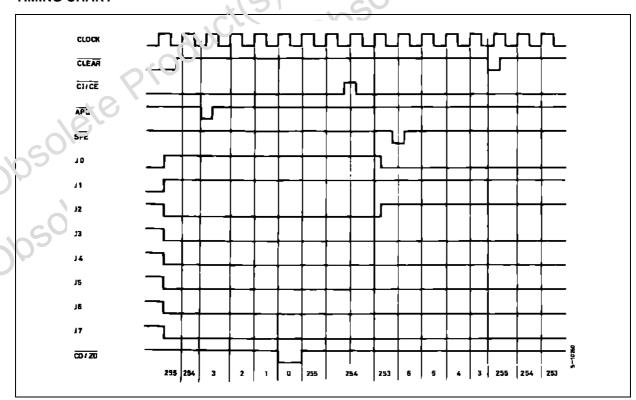
TRUTH TABLE

	C	ONTRO	_ INPUTS	3	MODE	FUNCTIONAL DESCRIPTION
	CLEAR	APE	SPE	CI/CE	C MODE	FUNCTIONAL DESCRIPTION
	Н	Н	Н	ή .	COUNT INHIBIT	EVEN IF CLOCK IS GIVEN, NO COUNT IS MADE
	Н	Н	Н		REGULAR COUNT	DOWN COUNT AT RISING EDGE OF CLOCK
	Н	Н		Х	SYNCHRONOUS PRESET	DATA OF PI TERMINAL IS PRESET AT RISING EDGE OF CLOCK
	Н		X	X	ASYNCHRONOUS PRESET	DATA OF PI TERMINAL IS ASYNCHRONOUSLY PRESET TO CLOCK
	L	Χ	Χ	X	CLEAR	COUNTER IS SET TO MAXIMUM COUNT
0	Y: Doi't C Maximum (55"			
O'	osc)`				

LOGIC DIAGRAM



TIMING CHART



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	-0.5 to +7	V
V _I	DC Input Voltage	-0.5 to V _{CC} + 0.5	V
V _O	DC Output Voltage	-0.5 to V _{CC} + 0.5	V
I _{IK}	DC Input Diode Current	± 20	mA
I _{OK}	DC Output Diode Current	± 20	mA
Io	DC Output Current	± 25	mA
I _{CC} or I _{GND}	DC V _{CC} or Ground Current	± 50	mA
P_{D}	Power Dissipation	500(*)	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation uniterviese conditions is not implied
(*) 500mW at 65 °C; derate to 300mW by 10mW/°C from 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

	Symbol	Parameter	1018	Value	Unit
	V _{CC}	Supply Voltage		2 to 6	V
	VI	Input Voltage	1250	0 to V _{CC}	V
	Vo	Output Voltage		0 to V _{CC}	V
	T _{op}	Operating Temperature	7	-55 to 125	°C
		Input Rise and Fall Time	$V_{CC} = 2.0V$	0 to 1000	ns
	t _r , t _f	,(5)	$V_{CC} = 4.5V$	0 to 500	ns
		, Cil	$V_{CC} = 6.0V$	0 to 400	ns
0	osoli osoli	ate Product(s)			

DC SPECIFICATIONS

		7	Test Condition				Value				
Symbol	Parameter	V _{CC}		T _A = 25°C -40 to			-40 to	o 85°C -55 to 125°C			Unit
		(V)		Min.	Тур.	Max.	Min.	Max.	Min.	Max.	
V _{IH}	High Level Input	2.0		1.5			1.5		1.5		
	Voltage	4.5		3.15			3.15		3.15		V
		6.0		4.2			4.2		4.2		
V_{IL}	Low Level Input	2.0				0.5		0.5		0.5	
	Voltage	4.5				1.35		1.35		1.35	V
		6.0				1.8		1.8		1.8	
V_{OH}	High Level Output	2.0	I _O =-20 μA	1.9	2.0		1.9		1.9	15	1
	Voltage	4.5	I _O =-20 μA	4.4	4.5		4.4		4.4		1
		6.0	I _O =-20 μA	5.9	6.0		5.9		5.3		V
		4.5	I _O =-4.0 mA	4.18	4.31		4.13	A 0	4.10		
		6.0	I _O =-5.2 mA	5.68	5.8		5.93	0.	5.60	16	
V _{OL}	Low Level Output	2.0	I _O =20 μA		0.0	0.1		0.1		0.1	1
	Voltage	4.5	I _O =20 μA		0.0	0.7		0.1	. 10	0.1	
		6.0	I _O =20 μA		0.0	0.1		0.1	O	0.1	V
		4.5	I _O =4.0 mA	C	0. 7	0.26	01	0.33		0.40	
		6.0	I _O =5.2 mA	10	0.18	0.26		0.33		0.40	
I _I	Input Leakage Current	6.0	$V_I = V_{CC} \text{ or } GND$. (± 0.1		± 1		± 1	μΑ
I _{CC}	Quiescent Supply Current	6.0	V = VCC or GND	G	$O_{J_{i}}$	4		40		80	μΑ

AC ELECTRICAL CHARACTER'STICS ($C_L = 50 \text{ pF}$, Input $t_r = t_f = 6 \text{ns}$)

	A(0)	7	est Condition				Value				
Symbol	Paran eter	V _{CC}	*(3)	Т	A = 25°	С	-40 to	85°C	-55 to	125°C	Unit
	a to	(V)		Min.	Тур.	Max.	Min.	Max.	Min.	Max.	
t _{TLH} t _{TE} '.	Output Transition	2.0			30	75		95		110	
50	Time	4.5			8	15		19		22	ns
O_{P}		6.0			7	13		16		19	
t _{PLH} t _{PHL}	Propagation Delay	2.0			96	185		230		280	
	Time OO (7TP)	4.5			24	37		46		56	ns
- 0	(CK - CO/ZD)	6.0			20	31		39		47	
t _{PLH} t _{PHL}	Propagation Delay	2.0			116	225		280		340	
O	T <u>ime</u> (APE - CO/ZD)	4.5			29	45		56		68	ns
	(APE - CO/ZD)	6.0			25	38		48		57	
t _{PLH} t _{PHL}	Propagation Delay	2.0			104	200		250		300	
	Time	4.5			26	40		50		60	ns
	(CL - CO/ZD)	6.0			22	34		43		51	
t _{PLH} t _{PHL}	Propagation Delay	2.0			48	95		120		145	
	Time (CL/CF)	4.5			12	19		24		29	ns
	(CI/CE - CO/ZD)	6.0			10	16		20		24	

		1	est Condition				Value				
Symbol	Parameter	v _{cc}		т	A = 25°	С	-40 to	85°C	-55 to	125°C	Unit
		(V)		Min.	Тур.	Max.	Min.	Max.	Min.	Max.	
f _{MAX}	Maximum Clock	2.0		4	8		3		2.6		
	Frequency	4.5		20	32		16		13		MHz
		6.0		24	38		19		15		
t _W	Clock Pulse Width	2.0		150	20		195		235		
	HIGH or LOW	4.5		30	7		36		45		ns
		6.0		25	5		32		40		
t _W	CLEAR Pulse	2.0		115	35		140		175		
	Width LOW	4.5		20	12		28		35		ns
		6.0		19	10		24		30	1/2	1
t _W	Preset Enable	2.0		115	31		140		175		
	Pulse Width APE,	4.5		20	11		28	- 21	:5		ns
	LOW	6.0		19	9		24	70	30		
t _{REM}	Removal time	2.0		47	12		ν?		70	16	
	CLEAR to CLOCK	4.5		9	4		12	ì	13	1/2	ns
	or APE to CLOCK	6.0		8	3	40	10		11		
t _{SETUP}	Set Up Time SPE	2.0		70	20	7	90	7	110		
	to CLOCK	4.5		13	7		16	0	20		ns
		6.0		11	5		15		16		
t _{SETUP}	Set Up Time CI/CE	2.0		105	40		175		205		
	to CLOCK	4.5		27	14	XO	36		42		ns
		6.0		23	12		31		36		
t _{SETUP}	Set Up Time Jn to	2.0	16	72	20		92		105		
	CLOCK	4.5	4/5	14	8		18		20		ns
		6.0		12	6		15		18		
t _{hold}	Hold Time SPE to	7.0		-14	0		0		0		
1.0.0	CLOCK	4.5		-5	0		0		0		ns
	010	6.0	.151	-4	0		0		0		
t _{hold}	Hold Time CI/CE to	2.0		-30	0		0		0		
	CFOCK	4.5		-11	0		0		0		ns
	0	6.0		-9	0		0		0		
(hali	Hold Time Jn to	2.0		-17	0		0		0		
12	CLOCK	4.5		-6	0		0		0		ns
		6.0		-5	0		0		0		

CAPACITIVE CHARACTERISTICS

72		1	est Condition				Value				
Symbol	Parameter	v _{cc}		T,	_A = 25°	С	-40 to	85°C	-55 to	125°C	Unit
		(V)		Min.	Тур.	Max.	Min.	Max.	Min.	Max.	
C _{IN}	Input Capacitance	5.0			5	10		10		10	pF
C _{PD}	Power Dissipation Capacitance (note 1)	5.0			60						pF

¹⁾ C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}$

FUNCTIONAL DESCRIPTION

This device is an 8-stage presettable synchronous down counter. Carry Out/Zero Detect (CO/ZD) is output at the "L" level for the period of 1 bit when the readout becomes "0". This device adopts 8-bit-binary counter decimal notation, making setting up to 255 counts possible.

COUNT OPERATION

At the "H" level of control input of CLEAR, SPE and APE, the counter carriers out down count operation one by one at the rise of pulse given to CLOCK input. Count operation can be inhibited by setting Carry Input/Clock Enable CI/CE to the "H" level.

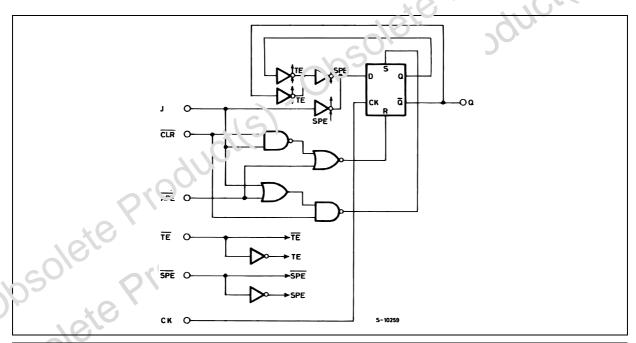
CO/ZD is output at the "L" level when the readout becomes "0" but is <u>not output</u> even if the readout becomes "0" when <u>CI/CE</u> is at the "H" level, thus maintaining the "H" level.

Synchronous cascade operation can be carried out by using CI/CE input and CO/ZD output.

The contents of count jump to maximum count (255) if clock is given when the readout is "0". Therefore, operation of 256-frequency division is carried out when clock input alone is given without various kinds of preset operation.

PRESET AND RESET OPERATION

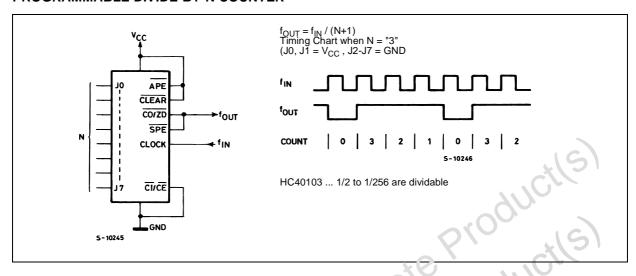
When Clear (CLEAR) input is set to the "L" level, the readout is set to the maximum count independently When of other inputs. Asynchronous Preset Enable (APE) input is set to the "L" level, readouts given on J0 to J7 can be asynchronously to the counter preset independently of inputs other than CLEAR input. When Synchronous Preset Enable (S.P.E) is set to the "L" level the readouts given on J0 to J7 can be preset to counter synchronously with the rise of clock. As to these operation mode, refer to the truth table.



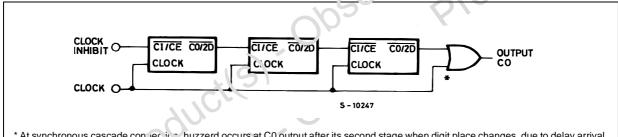
20,			INPUTS			OUTPUT
CLEAR	APE	SPE	J	TE	CLOCK	Q n + 1
L	Х	Х	Х	Х	Х	L
Н	L	Х	L	Х	Х	L
Н	L	X	Н	X	X	Н
Н	Н	L	L	Х	7	L
Н	Н	L	Н	Х		Н
Н	Н	L	Х	Х	Z	
Н	Н	Н	Х	L	L	Qn
Н	Н	Н	Х	Н	X	Qn

TYPICAL APPLICATIONS

PROGRAMMABLE DIVIDE-BY-N COUNTER

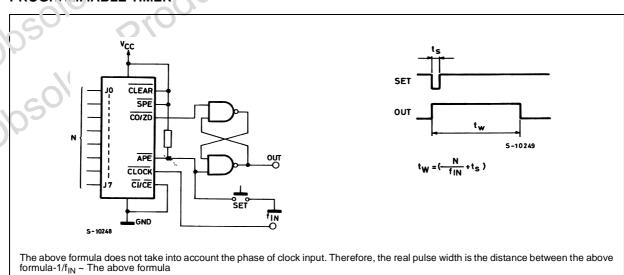


PARALLEL CARRY CASCADING



* At synchronous cascade con lec ic., huzzerd occurs at C0 output after its second stage when digit place changes, due to delay arrival. Therefore, take gate from high isal or the like, not from C0 output at the rear stage directly

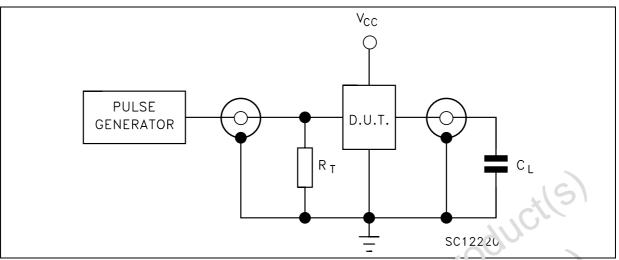
PROGRAMMABLE TIMER



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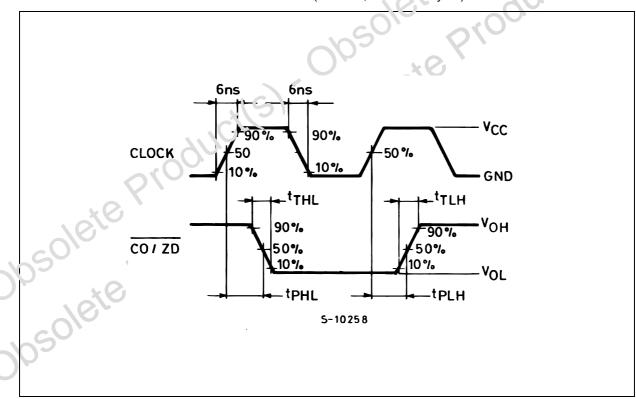
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TEST CIRCUIT

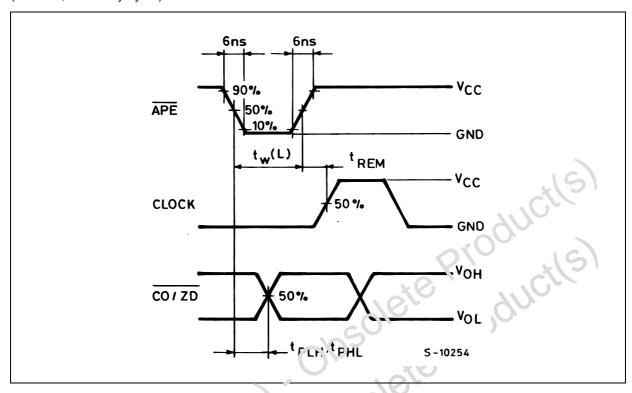


 C_L = 50pF or equivalent (includes jig and probe capacitance) R_T = Z_{OUT} of pulse generator (typically 50 Ω)

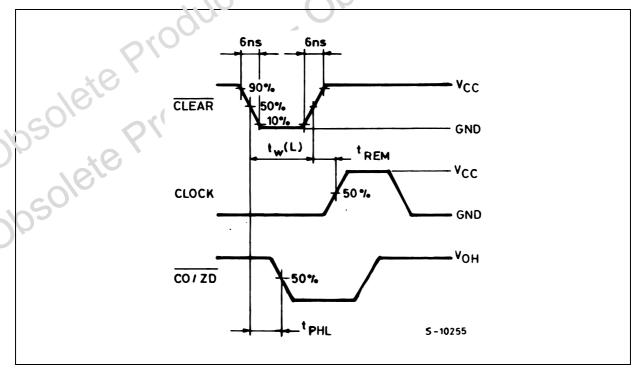
WAVEFORM 1: PROPAGATION DELAY TIME (f=1MHz; 50% duty cycle)



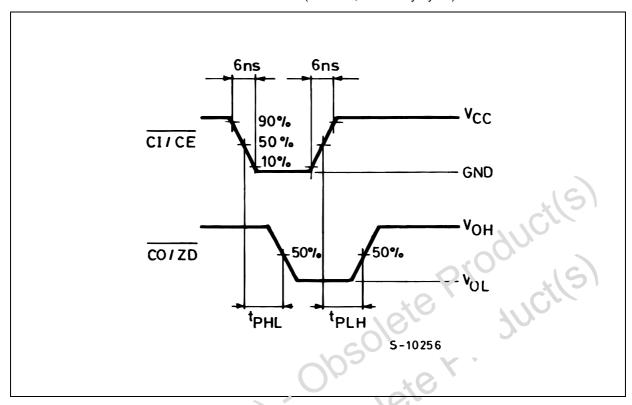
WAVEFORM 2: PROPAGATION DELAY, MINIMUM PULSE WIDTH AND REMOVAL TIME (f=1MHz; 50% duty cycle)



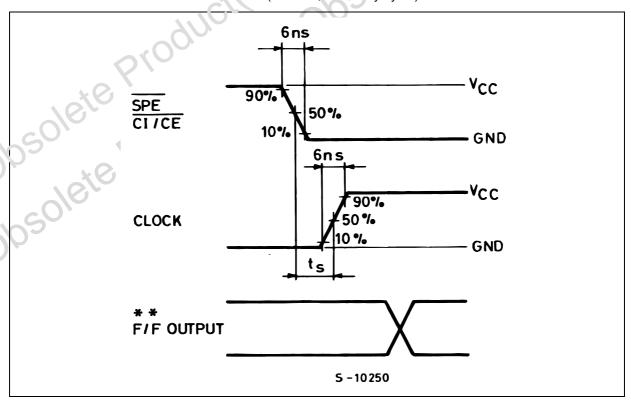
WAVEFORM 3: PROPAGATION DELAY, WINIMUM PULSE WIDTH AND REMOVAL TIME (f=1MHz; 50% duty cycle)



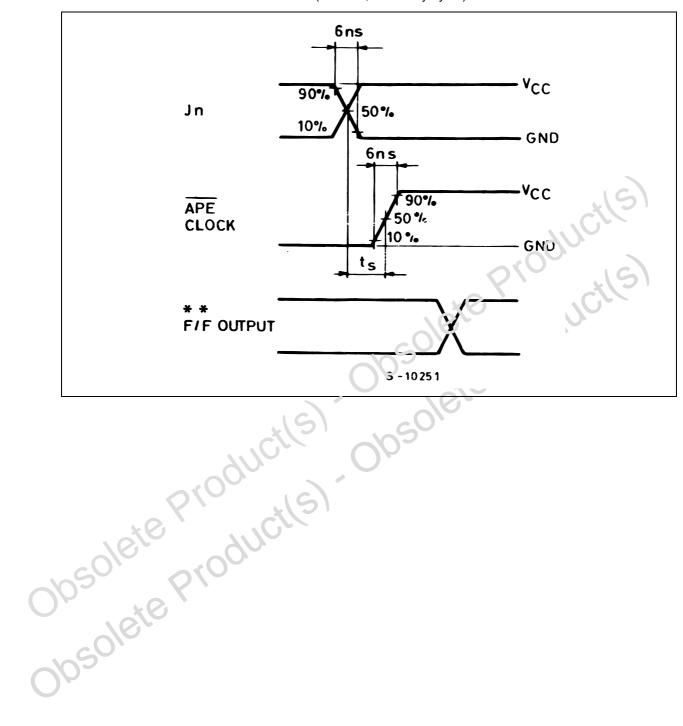
WAVEFORM 4: PROPAGATION DELAY TIME (f=1MHz; 50% duty cycle)



WAVEFORM 5: MINIMUM SETUP TIME (1=1MHz; 50% duty cycle)

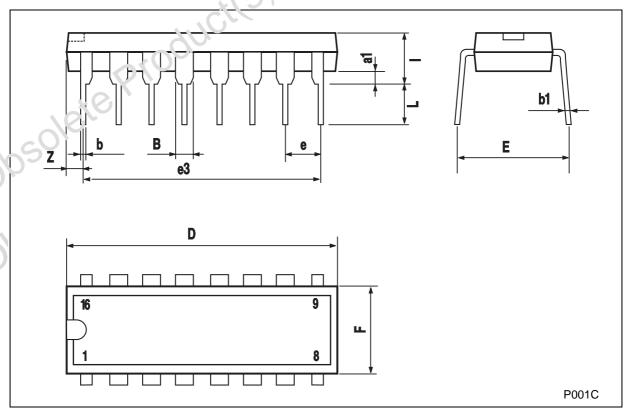


WAVEFORM 6: MINIMUM SETUP TIME (f=1MHz; 50% duty cycle)



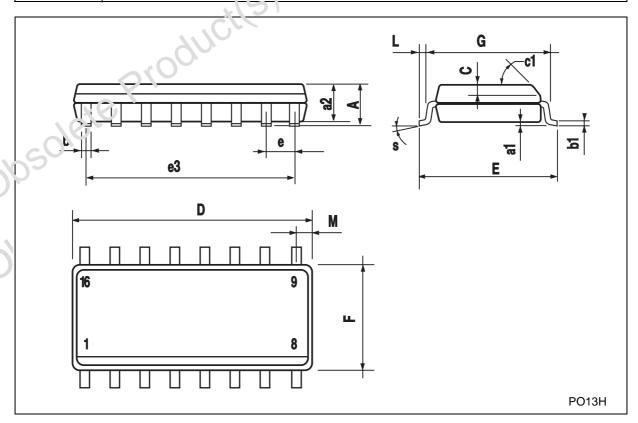
Plastic DIP-16 (0.25) MECHANICAL DATA

DIM		mm.			inch	
DIM.	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
В	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	16
D			20		.(ე.787
E		8.5			0.335	
е		2.54			2:100	
e3		17.78		×6	0.700	
F			7.1	18,		0.280
1			5.1	0		0.201
L		3.3	Ob		0.130	
Z			1.27			0.050



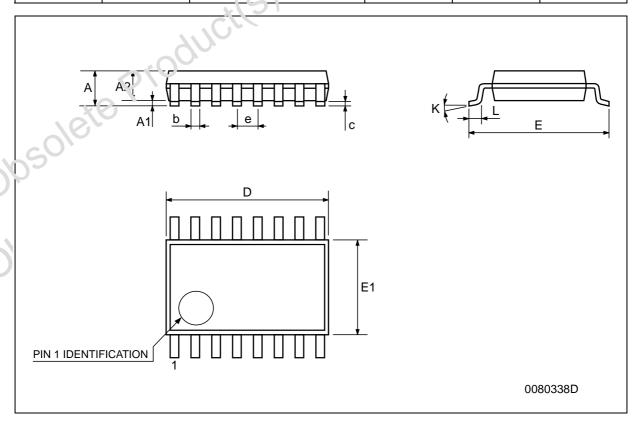
SO-16 MECHANICAL DATA

DIM.		mm.			inch	
DIIVI.	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
А			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
С		0.5			0.019	1191
c1			45° (t	yp.)	.(
D	9.8		10	0.385	40	0.393
E	5.8		6.2	0.228	100	0.244
е		1.27			0.050	
e3		8.89		48	0.350	
F	3.8		4.0	7.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
М			2.52			0.024
S			8° (m	ax.)	•	



TSSOP16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
А			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		v.012
С	0.09		0.20	0.004	401	0.0089
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.160	0.173	0.176
е		0.65 BSC	-100	0,	0.0256 BSC	
К	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030



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