

PSMN7R5-60YL

N-channel 60 V, 7.5 m Ω logic level MOSFET in LFPAK56 **20 November 2015** Product data sheet

1. **General description**

Logic level N-channel MOSFET in an LFPAK56 (Power SO8) package using TrenchMOS technology. This product is designed and qualified for use in a wide range of power supply & motor control equipment.

Features and benefits 2.

- Advanced TrenchMOS provides low R_{DSon}and low gate charge
- Logic level gate operation
- Avalanche rated, 100% tested
- LFPAK provides maximum power density in a Power SO8 package

Applications 3.

- Synchronous rectifier in LLC topology
- Chargers & adaptors with V_{out} < 10 V
- Fast charge & USB-PD applications
- Battery powered motor control
- LED lighting & TV backlight

Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V_{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C	-	-	60	V
I _D	drain current	V _{GS} = 5 V; T _{mb} = 25 °C; <u>Fig. 2</u>	-	-	86	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C; <u>Fig. 1</u>	-	-	147	W
Tj	junction temperature		-55	-	175	°C
Static chara	acteristics			'	'	'
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 20 A; T _j = 25 °C; Fig. 11	-	6	7.5	mΩ
Dynamic ch	naracteristics					
Q _{G(tot)}	total gate charge	V_{GS} = 10 V; I_D = 20 A; V_{DS} = 48 V; T_j = 25 °C; <u>Fig. 13</u> ; <u>Fig. 14</u>	-	60.6	-	nC
Q_{GD}	gate-drain charge	$V_{GS} = 5 \text{ V}; I_D = 20 \text{ A}; V_{DS} = 48 \text{ V};$ $T_j = 25 \text{ °C}; Fig. 13; Fig. 14$	-	9.7	-	nC



Symbol	Parameter	Conditions		Min	Тур	Max	Unit
Avalanche ruggedness							
E _{DS(AL)S}	non-repetitive drain- source avalanche energy	I_D = 86 A; $V_{sup} \le$ 60 V; R_{GS} = 50 Ω; V_{GS} = 5 V; $T_{j(init)}$ = 25 °C; unclamped; Fig. 4	[1][2]	-	-	76.5	mJ

- Single-pulse avalanche rating limited by maximum junction temperature of 175 $^{\circ}\text{C}.$ Refer to application note AN10273 for further information.

Pinning information

Table 2. **Pinning information**

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	mb	D
2	S	source		
3	S	source	d	G 4
4	G	gate	gggg	mbb076 S
mb	D	mounting base; connected to drain	1 2 3 4 LFPAK56; Power- SO8 (SOT669)	

Ordering information

Table 3. **Ordering information**

Type number	Package			
	Name	Description	Version	
PSMN7R5-60YL	LFPAK56; Power-SO8	Plastic single-ended surface-mounted package (LFPAK56; Power-SO8); 4 leads	SOT669	

Limiting values 7.

Table 4. **Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

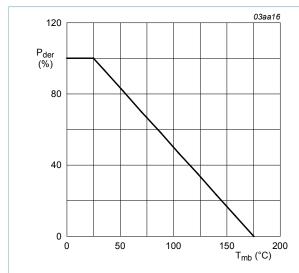
Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C	-	60	V
V_{DGR}	drain-gate voltage	R_{GS} = 20 k Ω	-	60	V
V _{GS}	gate-source voltage		-20	20	V
P _{tot}	total power dissipation	T _{mb} = 25 °C; <u>Fig. 1</u>	-	147	W
I _D	drain current	$T_{mb} = 25 ^{\circ}\text{C}; V_{GS} = 5 ^{\circ}\text{V}; Fig. 2$	-	86	Α
		T _{mb} = 100 °C; V _{GS} = 5 V; <u>Fig. 2</u>	-	61	Α
I _{DM}	peak drain current	T_{mb} = 25 °C; pulsed; $t_p \le 10 \mu s$; Fig. 3	-	346	Α

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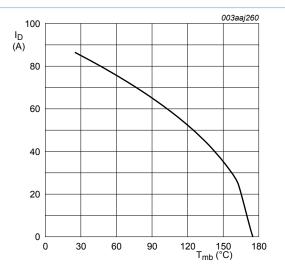
Symbol	Parameter	Conditions		Min	Max	Unit
T _{stg}	storage temperature			-55	175	°C
T _j	junction temperature			-55	175	°C
Source-drain	diode					
I _S	source current	T _{mb} = 25 °C		-	86	Α
I _{SM}	peak source current	pulsed; $t_p \le 10 \ \mu s$; $T_{mb} = 25 \ ^{\circ}C$		-	346	Α
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I_D = 86 A; $V_{sup} \le$ 60 V; R_{GS} = 50 Ω; V_{GS} = 5 V; $T_{j(init)}$ = 25 °C; unclamped; Fig. 4	[1][2]	-	76.5	mJ

- Single-pulse avalanche rating limited by maximum junction temperature of 175 $^{\circ}\text{C}.$ Refer to application note AN10273 for further information.



Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$



Continuous drain current as a function of mounting base temperature

$$V_{GS} \ge 5V$$

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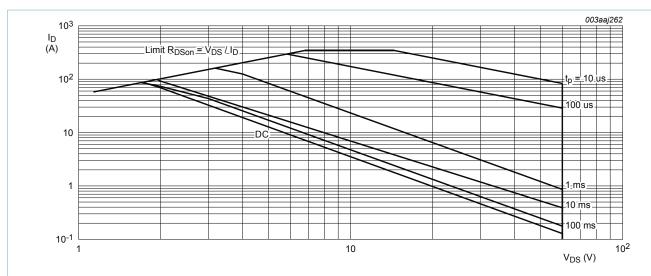
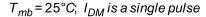


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage



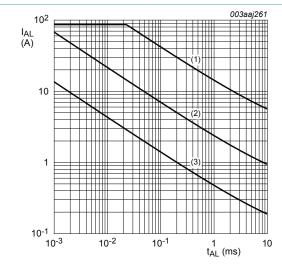


Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

(1)
$$T_{j(init)} = 25^{\circ}C$$
; (2) $T_{j(init)} = 150^{\circ}C$; (3) Repetitive Avalanche

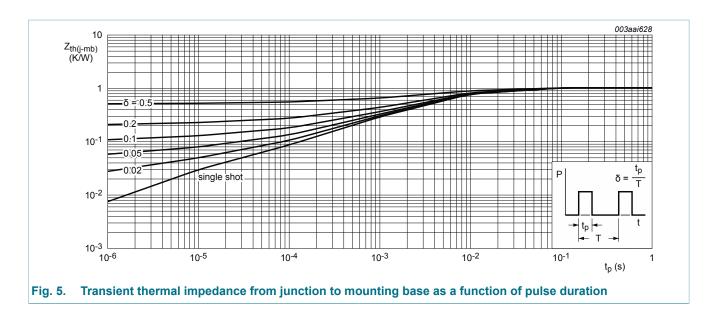
8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R _{th(j-mb)}	thermal resistance from junction to mounting base	Fig. 5	-	-	1.02	K/W

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9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	acteristics					
$V_{(BR)DSS}$	drain-source	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 °C$	60	-	-	V
	breakdown voltage	$I_D = 250 \ \mu A; \ V_{GS} = 0 \ V; \ T_j = -55 \ ^{\circ}C$	54	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ °C};$ Fig. 9; Fig. 10	1.4	1.7	2.1	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ °C};$ Fig. 9	-	-	2.45	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ °C};$ Fig. 9	0.5	-	-	V
I _{DSS}	drain leakage current	V _{DS} = 60 V; V _{GS} = 0 V; T _j = 175 °C	-	-	500	μA
		V _{DS} = 60 V; V _{GS} = 0 V; T _j = 25 °C	-	0.05	10	μA
I _{GSS} gate I	gate leakage current	V _{GS} = 16 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA
		V _{GS} = -16 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA
R _{DSon}	drain-source on-state	$V_{GS} = 5 \text{ V}; I_D = 20 \text{ A}; T_j = 25 ^{\circ}\text{C}; Fig. 11$	-	6.8	8.7	mΩ
resistance	resistance	V_{GS} = 10 V; I_{D} = 20 A; T_{j} = 25 °C; Fig. 11	-	6	7.5	mΩ
		$V_{GS} = 5 \text{ V}; I_D = 20 \text{ A}; T_j = 175 °C;$ Fig. 12; Fig. 11	-	-	19.7	mΩ
Dynamic ch	haracteristics		ı			
Q _{G(tot)}	total gate charge	I _D = 20 A; V _{DS} = 48 V; V _{GS} = 5 V; T _j = 25 °C; <u>Fig. 13</u> ; <u>Fig. 14</u>	-	31	-	nC

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N-channel 60 V, 7.5 m Ω logic level MOSFET in LFPAK56

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
		I _D = 20 A; V _{DS} = 48 V; V _{GS} = 10 V; T _j = 25 °C; <u>Fig. 13</u> ; <u>Fig. 14</u>	-	60.6	-	nC
Q_{GS}	gate-source charge	I _D = 20 A; V _{DS} = 48 V; V _{GS} = 5 V;	-	9	-	nC
Q_{GD}	gate-drain charge	T _j = 25 °C; <u>Fig. 13</u> ; <u>Fig. 14</u>	-	9.7	-	nC
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 25 V; f = 1 MHz;	-	3435	4570	pF
C _{oss}	output capacitance	T _j = 25 °C; <u>Fig. 15</u>	-	295	355	pF
C _{rss}	reverse transfer capacitance		-	150	205	pF
t _{d(on)}	turn-on delay time	$V_{DS} = 45 \text{ V}; R_L = 2 \Omega; V_{GS} = 5 \text{ V};$	-	17	-	ns
t _r	rise time	$R_{G(ext)} = 5 \Omega; T_j = 25 ^{\circ}C$	-	30	-	ns
t _{d(off)}	turn-off delay time		-	42	-	ns
t _f	fall time		-	26	-	ns
Source-dra	in diode					
V_{SD}	source-drain voltage	$I_S = 20 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 ^{\circ}\text{C}; Fig. 16$	-	0.82	1.2	V
t _{rr}	reverse recovery time	$I_S = 20 \text{ A}; dI_S/dt = -100 \text{ A/}\mu\text{s}; V_{GS} = 0 \text{ V};$	-	24	-	ns
Q _r	recovered charge	V _{DS} = 25 V; T _j = 25 °C	-	22.3	-	nC

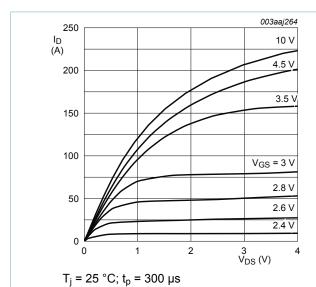


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

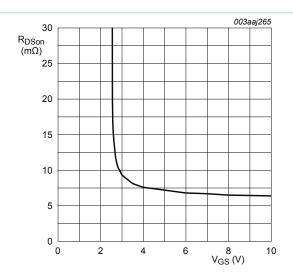


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

$$T_j = 25^{\circ}C; I_D = 20A$$

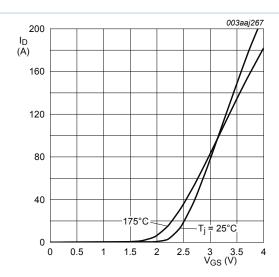


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values

$$V_{DS} = 10V$$

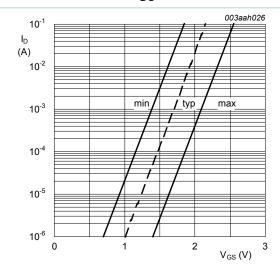


Fig. 10. Sub-threshold drain current as a function of gate-source voltage

$$T_j = 25^{\circ}C; \ V_{DS} = 5V$$

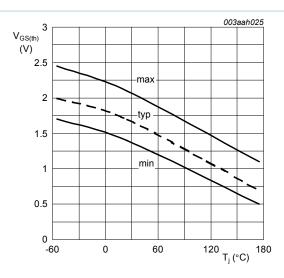
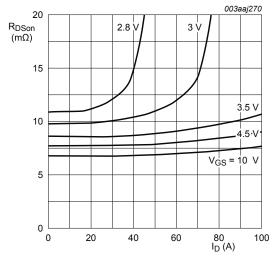


Fig. 9. Gate-source threshold voltage as a function of junction temperature

$$I_D$$
 = 1 mA; V_{DS} = V_{GS}



 $T_j = 25 \,^{\circ}\text{C}; t_p = 300 \,\mu\text{s}$

Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

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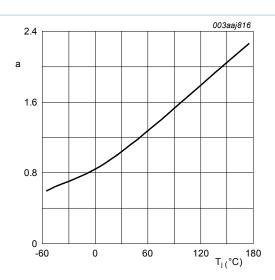


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon}(25^{\circ}C)}$$

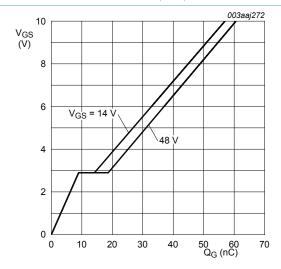


Fig. 14. Gate-source voltage as a function of gate charge; typical values

$$T_j = 25^{\circ}C; I_D = 20A$$

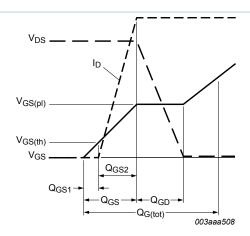


Fig. 13. Gate charge waveform definitions

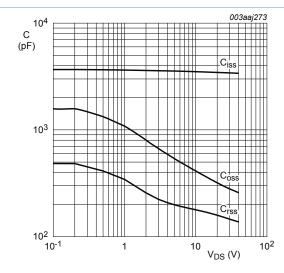


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$$V_{GS} = 0V$$
; $f = 1MHz$

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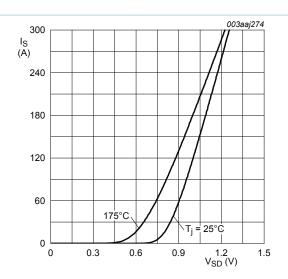


Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values $V_{\rm GS} = 0V$

10. Package outline

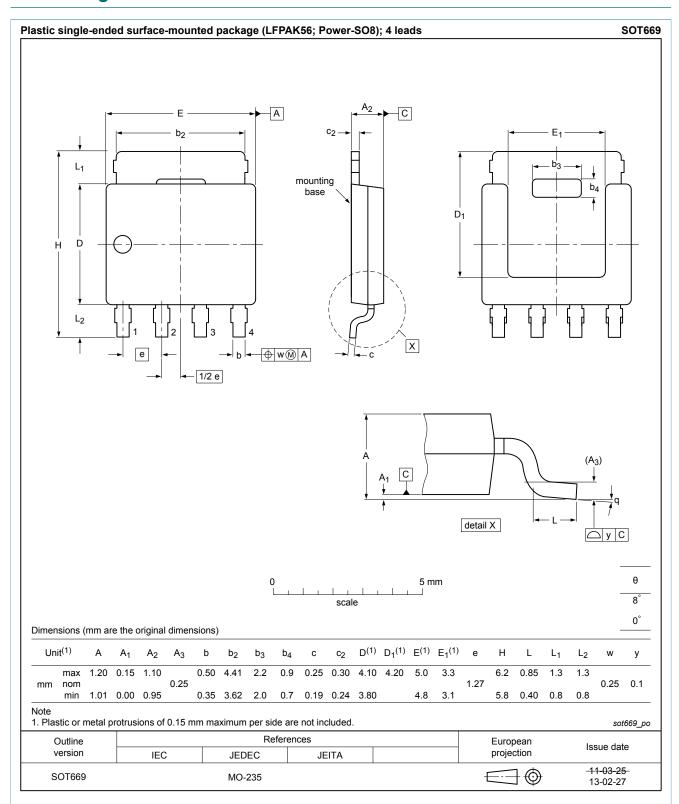


Fig. 17. Package outline LFPAK56; Power-SO8 (SOT669)

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