UM1522
User manual

EVALSP1340CPU evaluation board, revision 2.2

1 Introduction

This document applies to revision 2.2 evaluation boards.

This evaluation board is intended to be used to:

- enable quick evaluate and debugging of software for the SPEAr1340 embedded MPU
- act as a learning tool for rapid familiarity with the features of the SPEAr1340
- provide a reference design to use as a starting point for the development of a final application board

The EVALSP1340CPU board is equipped with interfaces to the high-speed peripherals embedded in SPEAr1340 device.

Figure 1. EVALSP1340CPU board rev. 2.2

Contents

List of tables

List of figures

2 Kit contents

- EVALSP1340CPU main board
- CLCD VGA plugboard
- AC power adapter (output voltage 12V 2A)

3 Features and block diagram

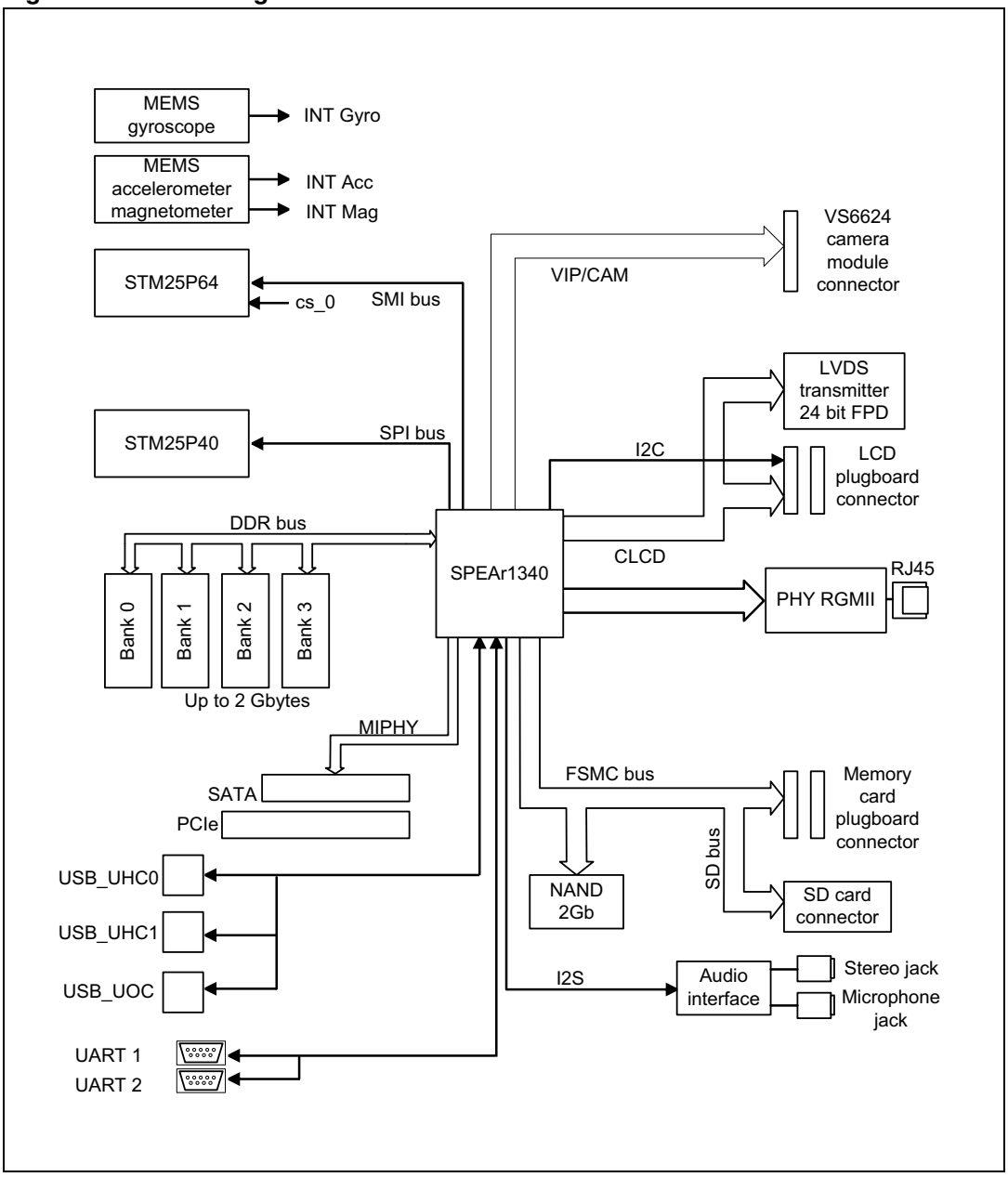
3.1 Board features

- SPEAr1340 embedded MPU
- 4 DDR3 chips (32-bit) 1 GB
- Serial NOR Flash, 8 MB
- 8-bit NAND Flash, 2 Gb
- 16-bit NAND Flash expansion connector
- Audio stereo jack and microphone
- Two USB 2.0 high speed host ports
- One OTG 2.0 high speed port (Micro USB-AB)
- One 10/100/1000 Ethernet port
- One PCIe X1 Root Complex connector
- One SATA connector
- One SDIO connector
- One UART serial port (up to 115 Kbaud)
- LCD connectors (LVDS bus - TFT panel)
- MEMS (accelerometer & magnetometer)
- Debug port (CPU JTAG connector)
- Camera module (1600x1200)

Optional

- 10" LCD kit - order code EVALSP1340LCD
- CLCD Video HDMI transmitter plugboard - order code EVALSP1340HDM

Figure 2. Block diagram



3.2 Implemented SPEAr1340 device features

The following table shows the device features, the primary and alternate functions as well as the specific plugboard used.

All IPs except Timer and MHY_debug are testable.

The XGPIO pins listed in the table can be set through software registers.

Legend:

X = available

= not available

Table 1. Summary of SPEAr1340 device features on the main board and plugboards

Feature	Main board	Dedicated pin/XGPIO	Shared function	Available on plugboard
DDR3 SDRAM	X	X		
2 x USB Host (USB_UHC0+USB_UHC1)	X	X		
USB OTG controller (USB_UOC)	X	X		
PCIe/SATA (PCIe+SATA+MiPHY)	X	X		
SMI	X	XGPIO		
SPI (SSP)	X	XGPIO	No	
SPI (SSP_SS3n)	X	XGPIO	No (1)	
2 x I2C (I2C0+I2C1)	X	XGPIO	No	
2 x UART(TX /RX only) (UART0+UART1)	X	XGPIO	No	
UART0	X	XGPIO	Timer (2)	
GMAC (GMAC+GMII)		XGPIO	No	
2 x CEC (CEC0+CEC1)		XGPIO	No(1)	CLCD
CLCD	X(3)	XGPIO	ARM ETM	CLCD
MCIF (SD/MMC)	X	XGPIO	No	
FSMC (NAND Flash)	X	XGPIO	No	
FSMC (NAND x16)	X (4)	XGPIO	Keyboard	
FSMC (NOR)	X (4)	XGPIO	MCIF	
PWM1		XGPIO	SSP_SS1n	
PWM2	Wake_up	XGPIO	Keyboard	
PWM3	DDR_SHUT_OFF	XGPIO	Timer (2)	
PWM4	DDR _SHUT_OFF	XGPIO	Timer (2)	

1. Shared with MPHY_debug
2. Timer not testable. Pins used for DDR_SHUT_OFF
3. Some CLCD pins are shared with MPHY_debug
4. Only strip connector on board

3.3 Plugboards

Plugboards allow you to adapt the evaluation board to interface with different hardware interfaces. They are connected to the main board through small high speed shielded connectors to avoid quality degradation of the signals. Each plugboard has the interface connectors in different positions to prevent insertion errors. Two video output plugboards are available: CLCD_VGA (included in the EVALSP1340CPU box) and CLCD_HDMI (EVALSP1340HDM can be ordered separately).

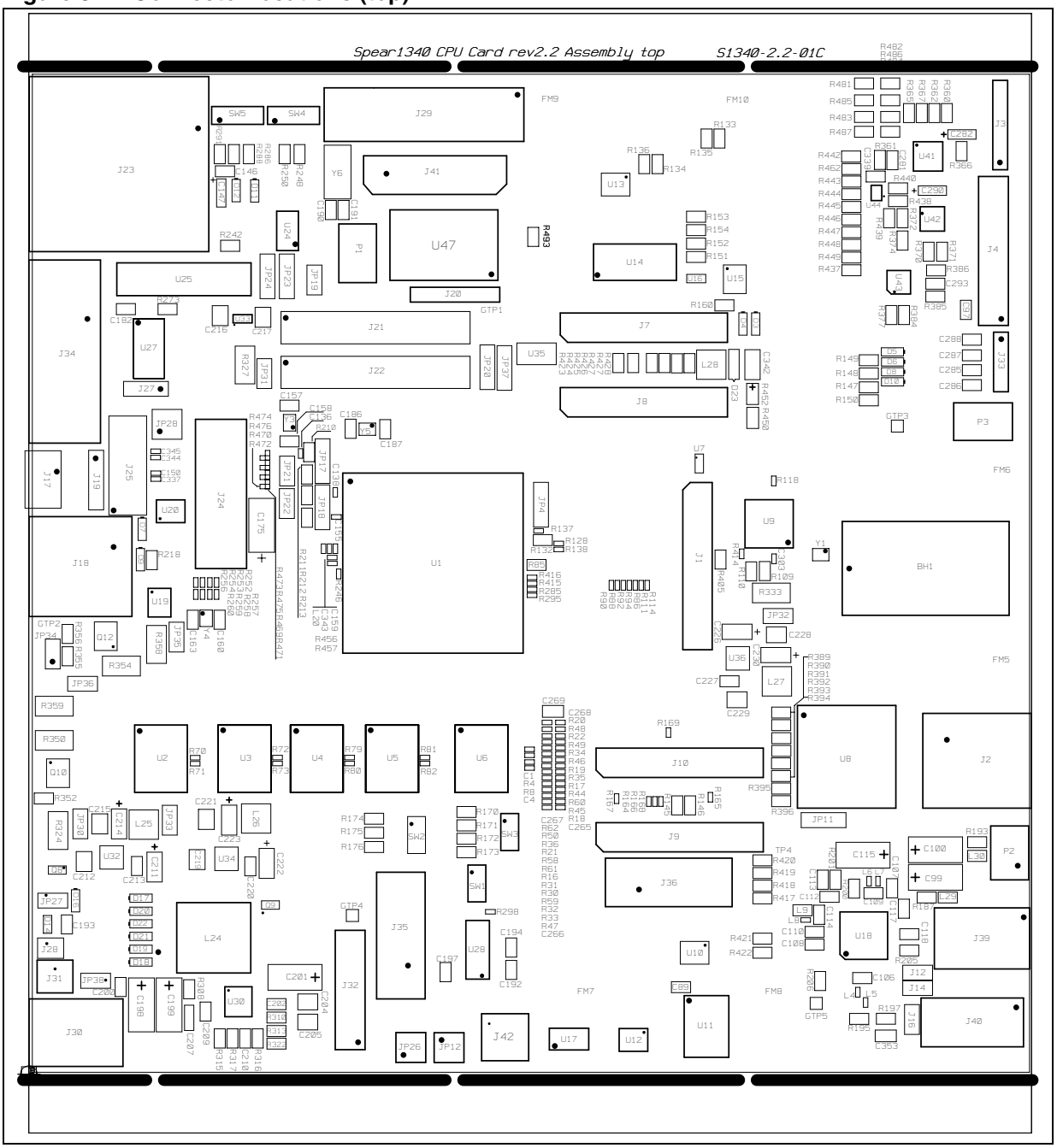
The CLCD plugboards support all the standards supported by the SPEAr1340 CLCD IP. Each plugboard contains a physical video chip interface, video connector, local power supply, and it implements all routing rules for standard requests.

- CLCD Video HDMI transmitter plugboard
  - A/V transmitter: Analog Device AD9889B
  - Supports HDMIv1.3 up to 1080p and UXGA@60Hz
  - Bandwidth: 165 MHz
  - HDCP v1.2 protocol
  - Supports both S/PDIF and I2S audio
  - Order code EVALSP1340HDM
- CLCD VGA plugboard
  - Analog Devices AD7125
  - 303 msps throughput rate
  - Triple 8-bit DAC

The VGA plugboard or the HDMI plugboard must be plugged into connectors J7 and J8.

3.4 Connectors, jumpers and pushbuttons

Figure 3. Connector locations (top)



4 Getting started

Caution: This board contains electrostatic-sensitive devices

The EVALSP1340CPU board is shipped in protective anti-static packaging. Do not submit the board to high electrostatic potentials, and follow good practices for working with static sensitive devices.

- Wear an anti-static wristband. Wearing a simple anti-static wristband can help to prevent ESD from damaging the board.
- Zero potential. Always touch a grounded conducting material before handling the board, and periodically while handling it.
- Use an anti-static mat. When configuring the board, place it on an anti-static mat to reduce the possibility of ESD damage.
- Handle only the edges. Handle the board by its edges only, and avoid touching board components.

4.1 Connecting

1. Connect a serial cable adapter (RS232 on J34) to a host PC (see Primary Serial cable setting).
2. On a host PC running Windows or Linux, start the Terminal program.
3. Connect the AC adapter to a power outlet.
4. Power on the board (plug the AC adapter jack into SW6). A sequence of boot messages displays, followed by the Linux console prompt.

4.2 Booting

The EVALSP1340CPU board can boot a Linux kernel pre-installed in the serial NOR Flash.

At power on, the serial port outputs a brief header message with some uBoot information (uBoot version, SDK version, and some internal hardware information). At this point, you can choose to:

- Stop the system directly in uBoot

  To do this, press the spacebar on the host computer keyboard before the boot delay time expires (default is 3 seconds).
- Boot Linux

  The system logs you in automatically as super user, and the Linux shell prompt displays on the screen.

4.3 Serial interface

A serial interface, which can typically be used to connect an operating system monitor console, is available on the J34 (primary, null modem connection). A secondary serial inference is available on J35 (optional).

- J34 is marked UART1 on the board and is connected to UART0 on the SPEAr1340 device
- J35 is marked UART2 on the board is connected to UART1 on the SPEAr1340 device

It is possible to simulate a cross cable by changing the position of the JP28 jumpers as shown below.

Refer to the schematic drawing (contact your local ST representative for availability), for the pin-out of the connectors.

Figure 4. Primary serial cable setting (J34)

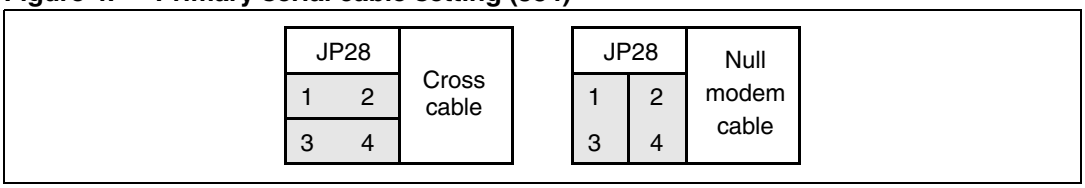
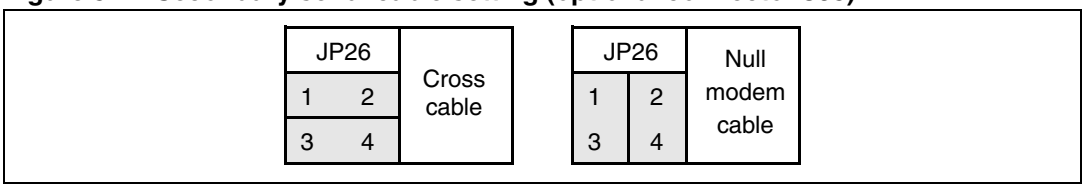


Figure 5. Secondary serial cable setting (optional connector J35)



4.4 Reset switch

A manual reset switch (P2) is available on the top side of the board.

5 Block descriptions

5.1 General power supply

The power supply block generates all the required voltages from a 12 V or a 5 V external AC/DC (plugged in J30). The generated voltages are:

- 5 V generated from 12 V with a step-down switching regulator (if 12 V ext. AC/DC is used)
- 5 V obtained from an over voltage protection device with thermal shutdown (if 5 V ext. AC/DC is used)
- 1.2 V, 1.5 V, 2.5 V, and 3.3 V generated from 5 V with a step-down switching regulator
- 1.8 V generated from 3.3 V with a low drop voltage regulator
- Up to 18.7 V generated from 12 V with a Step-up switching regulator (for LCD back light, default 12 V)

Table 2. Common power rails

Name	Use	Jumper for current measurement
+12V or +5V	J30: Power input connector	
VDD1V2	SPEAr core (SPEAr_VDD1V2) SPEAr DDR3 interface (SPEAr_DDR3_1V2)	JP30 JP35
VDD1V5	DDR3 chips SPEAr DDR I/O (SPEAr_DDR3_1V5) SPEAr RTC (RTC_VDD1V5)	 JP36 JP27
VDD1V8	SPEAr 1.8 V NAND8 Flash (JP20: Close 2&3 for 1.8V) SPEAr 1.8 V NAND16 Flash (JP37: Close 2&3 for 1.8V) Audio chip STA529 (U18)	
VDD2V5	Spear_VDD2V5: SPEAr_OTP antifuses (mounted R292 to supply) SPEAr GMII interface(JP4: Close 2-3 for 2.5V) MIPHY_VDD2V5_PLL SPEAr ADC_PLLs_VDD2V5 (JP17) SPEAr USB_VDD2V5 (JP18) A2D connector (J4)	JP31
VDD2V8	Camera Module (J42)	

Table 2. Common power rails (continued)

Name	Use	Jumper for current measurement
VDD3V3	SPEAr (SPEAr_VDD3V3) SPEAr GMII interface (JP4: Close 1-2 for 3.3 V) Audio chip STA529 (U18) PCIe Clock source PCIe Voltage JTAG MIPHY connector NAND Flash NAND8 Flash chip (Close 1&2 of JP20 for 3.3 V) NAND16 Flash chip (Close1&2 of JP37 for 3.3 V) CPU JTAG & trace connectors	JP32
+12V_HOST	PCIe x1 connectors	
LCD_BL	Back light voltage up to 18.7 V	

5.1.1 Power LEDs

Table 3. Power LEDs

Ref. Des.	Description
D16&D18 green	5 volt: +5V
D17 green	1.2 volt: VDD1V2
D20 green	1.5 volt: VDD1V5
D22 green	1.8 volt: VDD1V8
D21green	2.5 volt: VDD2V5
D19 green	3.3 volt: VDD3V3

5.2 Dynamic memory subsystem

5.2.1 Up to 2 GByte of DDR3 @533 MHz

Four 78-ball FPGA, x8 data interface components are present as follows:

- 4x 4 Gbit = 2 GByte (Micron MT41J512M8)

5.3 Static memory subsystem

5.3.1 Serial Flash

The following components are connected to the SMI interface:

- M25P64 (U11) ST serial Flash device: memory size = 8 MB
- M25P40 (U12) ST serial Flash device: memory size = 512 KB (optional, the device is not installed on the board)

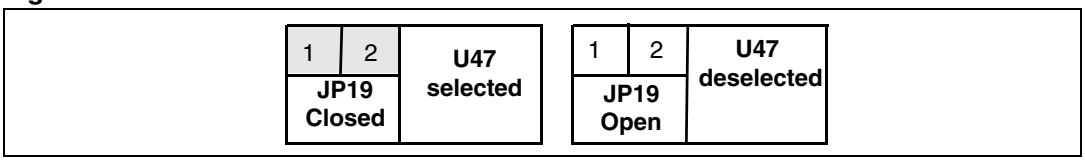
To enable M25P64 or M25P40, use SMI_CS0 with the JP12 jumpers set as shown in *Figure 6*.

Figure 6. Serial Flash M25P64 (U11) and M25P40 (U12) enable

5.3.2 NAND Flash

This block is based on Micron NAND Flash MT29F16G08 (U47) (2 GB: bus width = x8). If required, this chip can be replaced and another can be used. To do this, deselect the on-board Flash by removing jumper JP19, and connect an adapter board to J21, J22.

Figure 7. NAND Flash selection



5.3.3 NAND Flash expansion

Two 50-pin expansion connectors (J21, J22) enable the use of different Flash devices. When used, remove jumper JP19.

On the expansion connectors it is possible, through JP20, to select NAND_VDD between 3.3 V and 1.8 V to test different voltage devices. The NAND FLASH SPEAr I/O voltage has to be aligned with the Flash device voltage. Use JP20 and Strapping option SW2.1 & SW2.2 to set the correct voltage.

Figure 8. NAND Flash device voltage selector

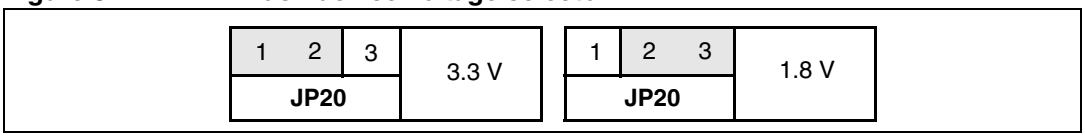
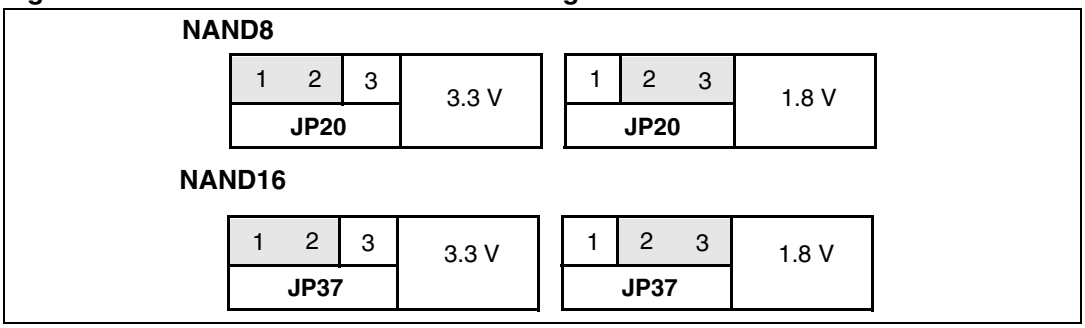


Figure 9. SPEAr NAND8/16 Flash I/O voltage selector



5.4 PCIe/SATA

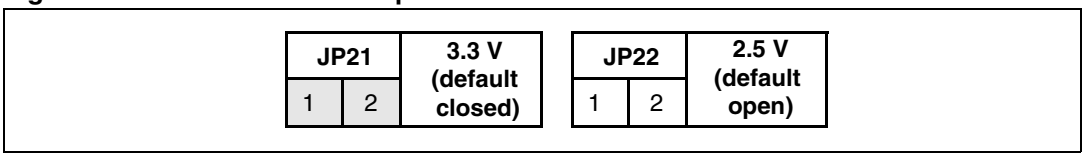
One standard x1 PCIe connector (J24) and one standard SATA connector (J25 plus J41 for Hdd Sata Power) are present on the board.

A single MPHY is shared through serial resistors.

If R470, R472, R474 and R476 (0 Ohm) are installed and R469, R471, R473, R475 are *not* installed the PCIe is available. Otherwise, if R143 (0 Ohm) R245 (200 Ohm) are installed and R456, R457, R257, R258 are *not* loaded, the SATA is available.

Note: SATA configuration is the default.

Figure 10. SPEAr MIPHY PLL power selectors



5.4.1 PCIe clock

The PCIe clock is generated by U23 ICS557-03 (differential clock generator). This device can generate 4 different clock frequencies. This depends on the settings of bits SS1, SS0, S1 and S0.

Table 4. PCIe clock settings (default settings)

SS1 (SW4-4)	SS0 (SW4-3)	S1(SW4-2)	S0 (SW4-1)	Spread %	Spread type	Output frequency
0	0	0	0	No spread	Not applicable	25
0	0	0	1	No spread	Not applicable	100
0	0	1	0	No spread	Not applicable	125
0	0	1	1	No spread	Not applicable	200
0	1	0	0	-0.5	Down	25
0	1	0	1	-0.5	Down	100
0	1	1	0	-0.5	Down	125
0	1	1	1	-0.5	Down	200
1	0	0	0	-0.75	Down	25

Table 4. PCIe clock settings (default settings) (continued)

SS1 (SW4-4)	SS0 (SW4-3)	S1(SW4-2)	S0 (SW4-1)	Spread %	Spread type	Output frequency
1	0	0	1	-0.75	Down	100
1	0	1	0	-0.75	Down	125
1	0	1	1	-0.75	Down	200
1	1	0	0	No spread	Not applicable	25
(1)	**(1)**	**(0)**	**(1)**	**No spread**	**Not applicable**	**100**
1	1	1	0	No spread	Not applicable	125
1	1	1	1	No spread	Not applicable	200

The output frequency must be set at 100 MHz. On the EVALS1340CPU board the default settings is: S1= 0, all others =1.

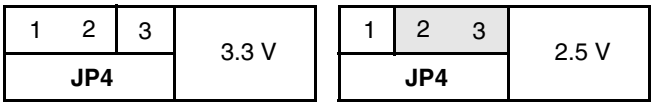
5.5 Ethernet subsystem

One RGMII chip PHY Micrel KSZ9031/9021RN (U9) is present on board, plus a transformer and Ethernet RJ45 connectors (J2).

The factory settings for the strapping options are fixed to support Ethernet speed 1000 with auto-negotiation, ID.

SPEAr GMII I/F VDD can be 3.3 V or 2.5 V. It is possible test this functionality by changing the position of jumper JP4 as shown below:

Figure 11. SPEAr GMII I/F voltage selector



5.5.1 Ethernet LEDs

Table 5. Ethernet LEDs

Reference	Description
LED1 (yellow) (on J2)	**DUPLEX STATUS:** The LED is lit when the PHY is in full duplex operation after the link is established.
LED2 (green) (on J2)	**GOOD LINK LED**: The LED output indicates that the PHY has established a good link.

6 USB 2.0 subsystem

6.1 Host ports

The board has two host ports that are fully compliant with the USB 2.0 specification (two controllers with one port each). This means that the two hosts can work in concurrent mode with the maximum possible bandwidth. Each host also has full control of the VBUS supplied by the TPS2052 power switch that also provides over current protection in case of a short circuit in the USB cable. The ports are equipped with LEDs showing the power status of each port (the green LED indicates the presence of VBUS and the red one the current limiter status).

6.2 Host LEDs

Table 6. USB host LEDs

Reference	Description
D5 Red	**USB HOST1 OVERCURRENT:** Abnormal current flowing on USB host 1 port
D6 Green	**USB HOST1 VBUS:** VBUS present on USB host port 1
D8 Green	**USB HOST2 VBUS:** VBUS present on USB host port 2
D10 Red	**USB HOST2 OVERCURRENT:** Abnormal current flowing on USB host 2 port

6.3 OTG USB

One OTG micro USB-AB connector is present on the board.

Table 7. OTG micro USB-AB LEDs

Reference	Description
D7 Red	USB OTG OVERCURRENT: Abnormal current flowing on OTG USB
D9 Green	USB OTG VBUS: VBUS present on OTG USB

7 A/D Interface

Eight analog input lines are provided on the J4 strip connector.

Table 8. J4 ADC connector ADC (optional)

Pin number	Signal
1	ADC_VDD2V5
2	ADC_VREFP
4 ... 18 (even only)	AIN0 ... AIN7
3 ... 19 (odd only)	AGND
20	ADC_VREFN

The connector also allows you to determine the conversion range by setting the conversion limits on pins J4.18 (lower limit) and J4.4 (upper limit). The default setting is to have pins 1-2 and 19-20 shorted by jumpers, which sets the conversion range to the maximum value of 0 to 2.5 V, with a granularity of 2.44 mV.

Removing the two jumpers and providing different values on pins 2 and 20 makes it possible to reduce the range, increasing the granularity. For example, an input of 1 V on J4.20 and 2 V on J4.4 provides a range of 1 to 2 V, in steps of less than 1 mV.

In any case, ensure the following relationships between the pins:

0 V	≤	J4.20	≤	J4 18 .. 43	≤	J4-2	≤	+2.5 V
AGND	≤	Vref_n	≤	ADC_In channels	≤	Vref_p	≤	AVDD

8 RTC (battery connector)

To avoid losing data even if the main power supply is switched off, the Real Time Clock can be powered with a 3 V external battery (BH1).

9 I²S audio bus

The bidirectional I²S bus drives the STM STA529 digital stereo audio amplifier. A 3.5 mm audio stereo jack (J39) and a 3.5 mm microphone jack (J40) are available on the board. Audio stereo channels are also available on Jumpers J12 & J14 (optional). A microphone input is available on jumper J16 (optional).

10 Memory SD card interface

An SD memory card interface connector (J23) is present on board. When the card is inserted it is auto-powered and detected. Led D11 and D12 show the status of the interface.

11 MEMS

The board can host an optional STM LSM303DLH and an STM L3G4200D micro electromechanical system (MEMS). The LSM303DLH is a high performance three-axis linear accelerometer and three-axis magnetometer. L3G4200D is a high performance three-axis gyroscope. Their function is to detect motion of the board in any direction, for applications like gaming, virtual reality, display orientation and so on. The MEMS communicate via the I2C serial bus.

12 LCD panel and touch screen function

The LCD used on board is a 10.4" TFT liquid crystal display module with capacitive touch screen capability. The DS90CF383B (U14) transmitter converts 28 bits of CMOS/TTL data into four LVDS (low voltage differential signaling) data streams. It has no internal registers and no startup sequence is necessary. J5 is the LCD connector, J6 is the LCD backlight power connector.

There is also an STMPE610 controller on the board. It communicates via the SPI serial bus. With this device it is possible manage the resistive touch screen. The signals are available on connector J33 (optional).

For this function, please use order code EVALSP1340LCD.

13 Debug interface

The following debug interfaces are provided:

- **The CPU JTAG interface:** this can be used for "static" debug, meaning that it is possible to set a breakpoint and, when the system stops, to verify the contents of the memory and/or registers and modify them if needed.

Table 9. J29 JTAG connector pin-out

Pin number	Signal
1, 2	VDD3V3
4 ... 20	GND
3	nTRST
5	TDI
7	TMS
9	TCK
13	TDO
15	Powergood
11,17,19	NC

- **The PCIe JTAG interface**: (reserved)
- **The CPU coresight interface.** (Trace 16 or 32) This can be used for "dynamic" debug. The coresight block embedded in the SPEAr1340 chip sends all the information about the AHB transactions during code execution to the external trace box and the external box stores this information in a local buffer. This makes it possible to stop the CPU activity in order to analyze the program flow. For example, if a particular data abort occurs, you can set a breakpoint on the data abort location and then, when the breakpoint is reached you can analyze the trace buffer. With this information, it becomes a simple task to identify the event that produced the problem.

Note: To use this feature is necessary to have the dedicated plugboard. Two mictor connectors are available (ETMv3 configuration) on this plugboard.

14 Strapping options

General purpose I/Os are present on the board. They are connected to DIP switches to allow the user to select/deselect them.

Immediately after reset phase, the SPEAr can be configured by means of the GPIO_A0 ... A3 strapping options.

2 µs after reset, pins can be used with GPIO features.

Note: Important: To use pins as input, the external pin driver must be in tri-state for the duration of the reset phase plus 2 µs.

Table 10. SW1 SPI Slave selection

Pin	Description (default settings)
1	SS1n (OFF)
2	SS2n (OFF)
3	SS3n (OFF)
4	SS0n (ON)

Note: When DIP switch SWx-x is in the ON position, the bit value is 0. When the DIP switch is in the OFF position, the bit value is 1.

Table 11. SW2 Voltage interface setting

Pin	Description (default settings)
1	8-bit NAND: ON = 1.8 V OFF = 3.3 V (OFF)
2	16-bit NAND: ON =1.8 V, OFF = 3.3 V (OFF)
3	GMII/RGMII: ON = 2.5 V, OFF = 3.3 V (ON)
4	Not used (OFF)

Note: When DIP switch SWx-x is in the ON position, the bit value is 0. When the DIP switch is in the OFF position, the bit value is 1.

Table 12. SW3 software boot options (default settings)

Boot Type	SW3-4	SW3-3	SW3-2	SW3-1
Bypass internal bootROM and jump to code in serial NOR Flash (SMI interface)	0	0	0	0
Boot from external serial NOR Flash (SMI).If the code not valid, boot from USB OTG is forced.	(0)	(0)	(0)	(1)
Boot from external serial NAND Flash (FSMC). If the code is invalid, boot from USB OTG is forced.	0	0	1	0
Boot from external parallel 16 bit-NOR Flash (FSMC). If the code is invalid, boot from USB OTG is forced.	0	1	0	0

Table 12. SW3 software boot options (default settings) (continued)

Boot Type	SW3-4	SW3-3	SW3-2	SW3-1
Boot MMC/SD memory card. If the code is invalid no boot from any other device.	1	1	0	1
Boot from UART (115 baud, no parity, 8 data bits, 1 stop bit)	0	1	0	1
Boot from USB device. (VID PID)	1	0	0	0

Note: When DIP switch SWx-x is in the ON position, the bit value is 0. When the DIP switch is in the OFF position, the bit value is 1.

15 Test modes

At reset, the SPEAr device can be configured in different modes through SW5.

Table 13. Test modes (default settings)

Boot type	SW5-5 TEST4	SW5-4 TEST3	SW5-3 TEST2	SW5-2 TEST1	SW5-1 TEST0
Normal functional mode	0	0	0	0	0
CPU JTAG debug mode	**(0)**	**(0)**	**(0)**	**(0)**	**(1)**

Note: When DIP switch SWx-x is in the ON position, the bit value is 0. When the DIP switch is in the OFF position, the bit value is 1.

16 LEDs

Several LEDs are present on the board. They display the following status information:

Table 14. Status LEDs

LED	Color	Status displayed
LED1 (on connector J2)	Yellow	GIG PHY activity
LED2 (on connector J2)	Green	GIG PHY link
D3	Green	LCD +3.3 V powered
D4	Red	LCD +3.3 V not powered or power failure
D5	Red	USB Host1 overcurrent
D6	Green	USB Host1 5 V
D7	Red	USB OTG overcurrent
D8	Green	USB Host2 5 V
D9	Green	USB OTG 5 V
D10	Red	USB Host2 overcurrent
D11	Green	SD memory card not detected
D12	Green	SD memory card +3.3 V detected and powered
D16	Green	+5V
D17	Green	VDD1V2
D18	Green	+5V
D19	Green	VDD3V3
D20	Green	VDD1V5
D21	Green	VDD2V5
D22	Green	VDD1V8

17 Jumper descriptions

The board has the following jumpers for settings or measurements:

Table 15. List of board jumpers

Jumper	Description
JP4	GMII voltage select (default 2-3 closed)
JP11	SPI memory Write Protect select (default 1-2 closed)
JP12	SMI memory Chip Select selector (see *Figure 6*) (default 1-2, 3&4 closed)
JP17	SPEAr 2V5 VREG2 selector (default 1-2 closed)
JP18	SPEAr 2V5 VREG1 selector (default 1-2 closed)
JP19	NAND Flash enable (default closed)
JP20	NAND8 supply voltage (default 1-2 closed)
JP21	SPEAr 3V3 MP_VREG_IN (default closed)
JP22	SPEAr 2V5 MIPHY PLL (open)
JP23	MIPHY 1V2 select (default 1-2 closed)
JP24	3V3 PCIe voltage (default 1-2 closed)
JP26	Secondary RS232 direct/cross (see schematics) (default open)
JP27	RTC battery enable (default closed)
JP28	Primary RS232 direct/cross (see schematics) (default 1-2, 3&4 closed)
JP30	1V2 enable (default closed)
JP31	2V5 enable (default closed)
JP32	3V3 enable (default closed)
JP33	DDR shutoff 1V5 enable (open)
JP34	DDR shutoff 1V2 enable (open)
JP35	SPEAr DDR3 1V2 power select (default closed)
JP36	SPEAr DDR3 1V5 power select (default closed)
JP37	NAND16/Keyboard supply voltage (default 1-2 closed)
JP38	Power Supply Enable (default closed)

18 Connectors

Table 16. List of board connectors

Connector	Description
J1	External Ethernet plugboard (optional)
J2	RJ45 Ethernet connector
J3	I2C strip connector
J4	A2D strip connector (optional)
J5	LCD connector (bottom side of board)
J6	LCD backlight power connector (bottom side of board)
J7	Video Out
J8	Video Out
J12	Audio out strip connector (optional)
J14	Audio out strip connector (optional)
J16	LCD Backlight power connector (bottom side of board)
J17	USB OTG connector
J18	USB Host double connector
J19	USB Host strip (optional)
J20	Keyboard strip connector (optional)
J21	Memory Card plugboard connector
J22	Memory Card plugboard connector
J23	SD Card connector
J24	PCIe HOST1 connector
J25	SATA connector
J27	UART Tx-Rx strip (optional)
J28	External battery connector
J29	JTAG connector
J30	Power board jack (+5V, +12V ext. AC adapter)
J31	Power board screw connector (optional)
J32	External Voltage regulator module for VCore (1.2 V, optional)
J33	Touch screen connector (optional)
J34	Primary RS232 connector
J35	Secondary RS232 connector (optional)
J36	JTAG MIPHY (optional)
J39	Stereo Audio Out jack

Table 16. List of board connectors (continued)

Connector	Description
J40	Mono Microphone In jack
J41	SATA power connector

19 Pushbuttons

P2 Reset switch

P1 Wakeup switch

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Revision history

Table 17. Document revision history

Date	Revision	Changes
16-Mar-2012	1	Initial release.
03-Apr-2012	2	Edited *Block diagram on page 8* Added: – "For this function, please use order code EVALSP1340LCD" to *Chapter 12: LCD panel and touch screen function* – Order code EVALSP1340HDM to *Plugboards on page 10* – 10" LCD kit - Order code EVALSP1340LCD and CLCD Video HDMI transmitter Plugboard - Order code EVALSP1340HDM to *Board features on page 7*
28-Sept-2012	3	Updated *Figure 2: Block diagram*: – Removed "camera plugboard connector" – Removed "GMII plugboard connector" – Changed "NAND 512 W3" in "NAND 2Gb". – Removed "STM25P40" on SMI bus. Removed the first note at page 10 "The signals for the Video/Camera input plugboard are available on connectors J9 and J10 (optional)". *Table 16: List of board connectors*: removed the two rows related to the connectors J9 and J10. Updated *Table 1: Summary of SPEAr1340 device features on the main board and plugboards*: – Removed the rows related to video camera available on plugboard. – deleted the availability of 2xI2C and GMAC on plugboard. *Section 3.1: Board features*: added the bullet "Camera module (1600x1200)". Updated *Figure 3: Connector locations (top)* inserting the rev2.2 layout. Updated *Section 3.3: Plugboards*

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