# MC10EP451, MC100EP451

# 3.3V / 5V  ECL 6-Bit Differential Register with Master Reset

## Description

The MC10/100EP451 is a 6–bit fully differential register with common clock and single–ended Master Reset (MR). It is ideal for very high frequency applications where a registered data path is necessary.

All inputs have a 75 kΩ pulldown resistor internally. Differential inputs have an override clamp. Unused differential register inputs can be left open and will default LOW. When the differential inputs are forced to $< V_{EE} + 1.2$ V, the clamp will override and force the output to a default state. When in the default state, and since the flip–flop is edge triggered, the output reaches a determined, but not predicted, valid state.

The positive transition of CLK (pin 4) will latch the registers. Master Reset (MR) HIGH will asynchronously reset all registers forcing Q outputs to go LOW.

The 100 Series contains temperature compensation.

## Features

- 450 ps Typical Propagation Delay
- Maximum Frequency > 3.0 GHz Typical
- Asynchronous Master Reset
- 20 ps Skew Within Device, 35 ps Skew Device–To–Device
- PECL Mode Operating Range: $V_{CC} = 3.0$ V to 5.5 V
  With $V_{EE} = 0$ V
- NECL Mode Operating Range: $V_{CC} = 0$ V
  With $V_{EE} = -3.0$ V to $-5.5$ V
- Open Input Default State
- Safety Clamp on Inputs
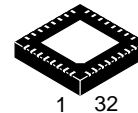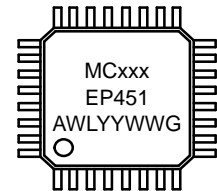- These Devices are Pb–Free and are RoHS Compliant

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### MARKING DIAGRAM*

**LQFP–32
FA SUFFIX
CASE 873A**

```
MCxxx
EP451
AWLYYWWG
○
```

**QFN32
MN SUFFIX
CASE 488AM**

1   32

```
1  ○
MCxx
EP451
AWLYYWW▪
        ▪
```

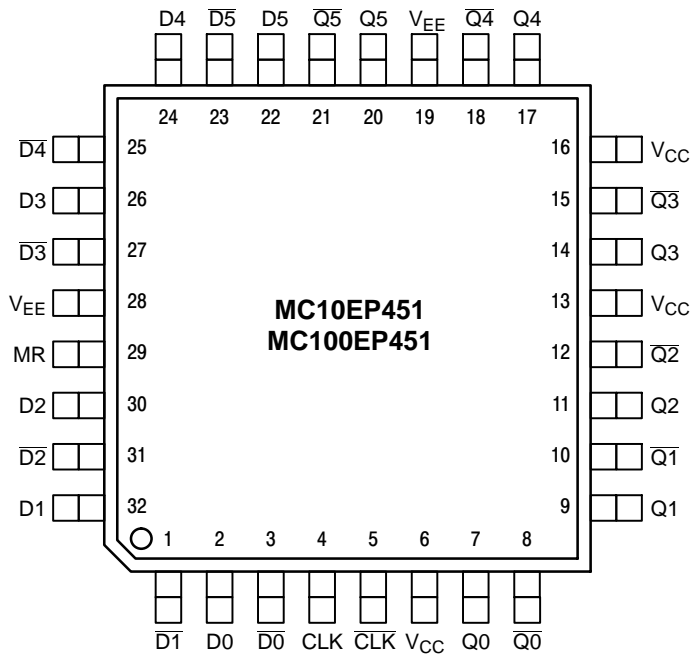| | |
|---|---|
| xxx | = 10 or 100 |
| A | = Assembly Location |
| WL | = Wafer Lot |
| YY | = Year |
| WW | = Work Week |
| G or ▪ | = Pb–Free Package |

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

# MC10EP451, MC100EP451



Warning: All $V_{CC}$ and $V_{EE}$ pins must be externally connected to Power Supply to guarantee proper operation.
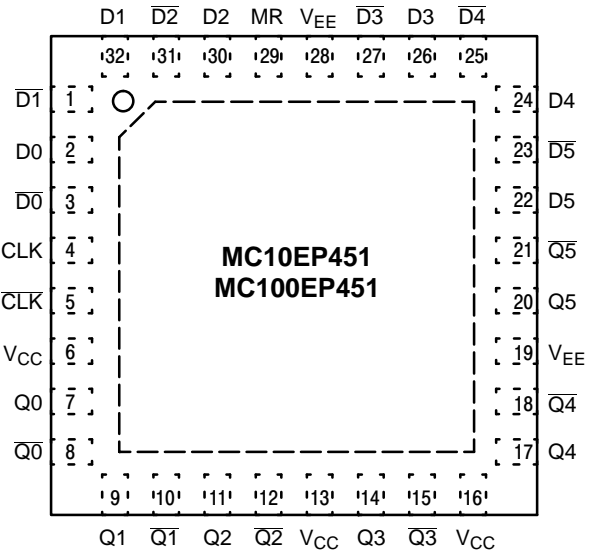
**Figure 1. LQFP–32 Pinout** (Top View)

**Figure 2. QFN–32 Pinout** (Top View)

**Table 1. PIN DESCRIPTION**

| PIN | FUNCTION |
|---|---|
| D [0:5]*, $\overline{D}$ [0:5]* | ECL Differential Data Inputs |
| MR* | ECL Master Reset Input |
| CLK*, $\overline{CLK}$* | ECL Differential Clock Inputs |
| Q [0:5], $\overline{Q}$ [0:5] | ECL Differential Data Outputs |
| $V_{CC}$ | Positive Supply |
| $V_{EE}$ | Negative Supply |
| EP for QFN–32, only | The Exposed Pad (EP) on the QFN–32 package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached to a heat–sinking conduit. The pad is electrically connected to $V_{EE}$. |

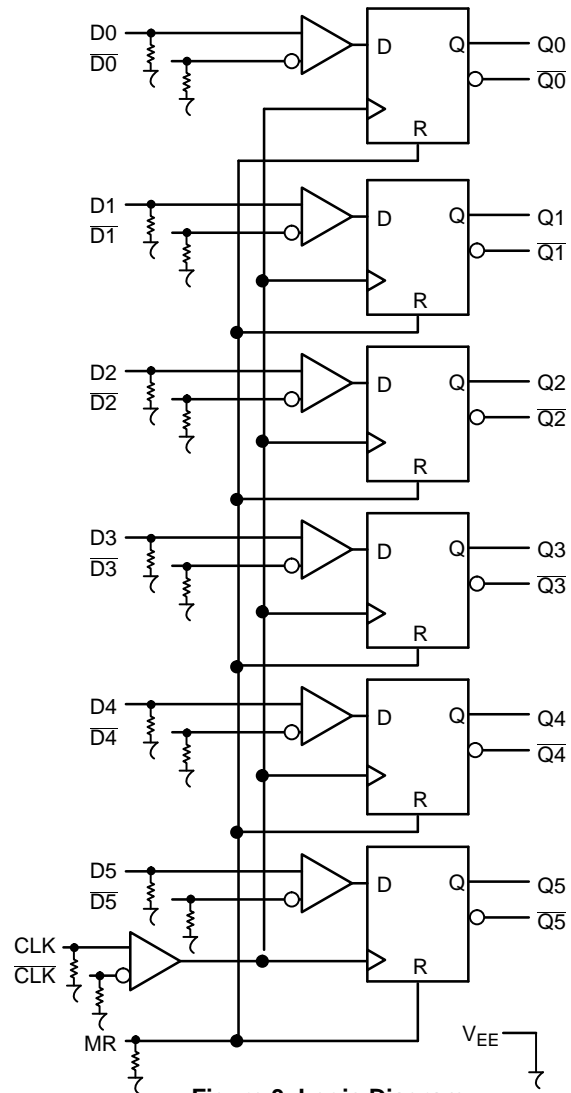\* Pins will default LOW when left open.

**Figure 3. Logic Diagram**

**Table 2. ATTRIBUTES**

| Characteristics | | Value | |
|---|---|---|---|
| Internal Input Pulldown Resistor | | 75 kΩ | |
| Internal Input Pullup Resistor | | N/A | |
| ESD Protection               Human Body Model<br>Machine Model<br>Charged Device Model | | > 2 kV<br>> 200 V<br>> 2 kV | |
| Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1) | | Pb Pkg | Pb−Free Pkg |
|                   LQFP−32<br>QFN−32 | | Level 2 | Level 2<br>Level 1 |
| Flammability Rating      Oxygen Index: 28 to 34 | | UL 94 V−0 @ 0.125 in | |
| Transistor Count | | 919 Devices | |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test | | | |

1. For additional information, see Application Note AND8003/D.

**Table 3. MAXIMUM RATINGS**

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | PECL Mode Power Supply | $V_{EE}$ = 0 V | | 6 | V |
| $V_{EE}$ | NECL Mode Power Supply | $V_{CC}$ = 0 V | | −6 | V |
| $V_I$ | PECL Mode Input Voltage<br>NECL Mode Input Voltage | $V_{EE}$ = 0 V<br>$V_{CC}$ = 0 V | $V_I \leq V_{CC}$<br>$V_I \geq V_{EE}$ | 6<br>−6 | V<br>V |
| $I_{out}$ | Output Current | Continuous<br>Surge | | 50<br>100 | mA<br>mA |
| $T_A$ | Operating Temperature Range | | | −40 to +85 | °C |
| $T_{stg}$ | Storage Temperature Range | | | −65 to +150 | °C |
| $\theta_{JA}$ | Thermal Resistance (Junction−to−Ambient) | 0 lfpm<br>500 lfpm | LQFP−32<br>LQFP−32 | 80<br>55 | °C/W<br>°C/W |
| $\theta_{JC}$ | Thermal Resistance (Junction−to−Case) | Standard Board | LQFP−32 | 12 to 17 | °C/W |
| $\theta_{JA}$ | Thermal Resistance (Junction−to−Ambient) | 0 lfpm<br>500 lfpm | QFN−32<br>QFN−32 | 31<br>27 | °C/W<br>°C/W |
| $\theta_{JC}$ | Thermal Resistance (Junction−to−Case) | 2S2P | QFN−32 | 12 | °C/W |
| $T_{sol}$ | Wave Solder           Pb−Free | | | 265 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

**Table 4. 10EP DC CHARACTERISTICS, PECL** $V_{CC}$ = 3.3 V, $V_{EE}$ = 0 V (Note 2)

| Symbol | Characteristic | −40°C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $I_{EE}$ | Power Supply Current | 80 | 95 | 125 | 80 | 95 | 125 | 80 | 95 | 125 | mA |
| $V_{OH}$ | Output HIGH Voltage (Note 3) | 2165 | 2290 | 2415 | 2230 | 2355 | 2480 | 2290 | 2415 | 2540 | mV |
| $V_{OL}$ | Output LOW Voltage (Note 3) | 1365 | 1490 | 1615 | 1430 | 1555 | 1680 | 1470 | 1615 | 1740 | mV |
| $V_{IH}$ | Input HIGH Voltage (Single−Ended) | 2090 | | 2415 | 2155 | | 2480 | 2215 | | 2540 | mV |
| $V_{IL}$ | Input LOW Voltage (Single−Ended) | 1365 | | 1690 | 1430 | | 1755 | 1490 | | 1815 | mV |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 4) | 2.0 | | 3.3 | 2.0 | | 3.3 | 2.0 | | 3.3 | V |
| $I_{IH}$ | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| $I_{IL}$ | Input LOW Current | 0.5 | | | 0.5 | | | 0.5 | | | μA |

**Table 5. 10EP DC CHARACTERISTICS, PECL** $V_{CC}$ = 5.0 V, $V_{EE}$ = 0 V (Note 5)

| Symbol | Characteristic | −40°C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $I_{EE}$ | Power Supply Current | 80 | 95 | 125 | 80 | 95 | 125 | 80 | 95 | 125 | mA |
| $V_{OH}$ | Output HIGH Voltage (Note 3) | 3865 | 3990 | 4115 | 3930 | 4055 | 4180 | 3990 | 4115 | 4240 | mV |
| $V_{OL}$ | Output LOW Voltage (Note 3) | 3065 | 3190 | 3315 | 3130 | 3255 | 3380 | 3170 | 3315 | 3440 | mV |
| $V_{IH}$ | Input HIGH Voltage (Single−Ended) | 3790 | | 4115 | 3855 | | 4180 | 3915 | | 4240 | mV |
| $V_{IL}$ | Input LOW Voltage (Single−Ended) | 3065 | | 3390 | 3130 | | 3455 | 3190 | | 3515 | mV |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 4) | 2.0 | | 5.0 | 2.0 | | 5.0 | 2.0 | | 5.0 | V |
| $I_{IH}$ | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| $I_{IL}$ | Input LOW Current | 0.5 | | | 0.5 | | | 0.5 | | | μA |

**Table 6. 10EP DC CHARACTERISTICS, NECL** $V_{CC}$ = 0 V, $V_{EE}$ = −5.5 V to −3.0 V (Note 6)

| Symbol | Characteristic | −40°C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $I_{EE}$ | Power Supply Current | 80 | 95 | 125 | 80 | 95 | 125 | 80 | 95 | 125 | mA |
| $V_{OH}$ | Output HIGH Voltage (Note 3) | −1135 | −1010 | −885 | −1070 | −945 | −820 | −1010 | −885 | −760 | mV |
| $V_{OL}$ | Output LOW Voltage (Note 3) | −1935 | −1810 | −1685 | −1870 | −1745 | −1620 | −1830 | −1685 | −1560 | mV |
| $V_{IH}$ | Input HIGH Voltage (Single−Ended) | −1210 | | −885 | −1145 | | −820 | −1085 | | −760 | mV |
| $V_{IL}$ | Input LOW Voltage (Single−Ended) | −1935 | | −1610 | −1870 | | −1545 | −1810 | | −1485 | mV |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 4) | $V_{EE}$+2.0 | | 0.0 | $V_{EE}$+2.0 | | 0.0 | $V_{EE}$+2.0 | | 0.0 | V |
| $I_{IH}$ | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| $I_{IL}$ | Input LOW Current | 0.5 | | | 0.5 | | | 0.5 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

2. Input and output parameters vary 1:1 with $V_{CC}$. $V_{EE}$ can vary +0.3 V to −2.2 V.
3. All loading with 50 Ω to $V_{CC}$ − 2.0 V.
4. $V_{IHCMR}$ min varies 1:1 with $V_{EE}$, $V_{IHCMR}$ max varies 1:1 with $V_{CC}$. The $V_{IHCMR}$ range is referenced to the most positive side of the differential input signal.
5. Input and output parameters vary 1:1 with $V_{CC}$. $V_{EE}$ can vary +2.0 V to −0.5 V.
6. Input and output parameters vary 1:1 with $V_{CC}$.

**Table 7. 100EP DC CHARACTERISTICS, PECL** $V_{CC}$ = 3.3 V, $V_{EE}$ = 0 V (Note 7)

| Symbol | Characteristic | −40°C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $I_{EE}$ | Power Supply Current | 85 | 105 | 135 | 85 | 105 | 135 | 85 | 105 | 135 | mA |
| $V_{OH}$ | Output HIGH Voltage (Note 8) | 2155 | 2280 | 2405 | 2155 | 2280 | 2405 | 2155 | 2280 | 2405 | mV |
| $V_{OL}$ | Output LOW Voltage (Note 8) | 1305 | 1480 | 1605 | 1305 | 1480 | 1605 | 1305 | 1480 | 1605 | mV |
| $V_{IH}$ | Input HIGH Voltage (Single−Ended) | 2075 | | 2420 | 2075 | | 2420 | 2075 | | 2420 | mV |
| $V_{IL}$ | Input LOW Voltage (Single−Ended) | 1305 | | 1675 | 1305 | | 1675 | 1305 | | 1675 | mV |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 9) | 2.0 | | 3.3 | 2.0 | | 3.3 | 2.0 | | 3.3 | V |
| $I_{IH}$ | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| $I_{IL}$ | Input LOW Current | 0.5 | | | 0.5 | | | 0.5 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

7. Input and output parameters vary 1:1 with $V_{CC}$. $V_{EE}$ can vary +0.3 V to −2.2 V.
8. All loading with 50 Ω to $V_{CC}$ − 2.0 V.
9. $V_{IHCMR}$ min varies 1:1 with $V_{EE}$, $V_{IHCMR}$ max varies 1:1 with $V_{CC}$. The $V_{IHCMR}$ range is referenced to the most positive side of the differential input signal.

**Table 8. 100EP DC CHARACTERISTICS, PECL** $V_{CC}$ = 5.0 V, $V_{EE}$ = 0 V (Note 10)

| Symbol | Characteristic | −40°C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $I_{EE}$ | Power Supply Current | 85 | 105 | 135 | 85 | 105 | 135 | 85 | 105 | 135 | mA |
| $V_{OH}$ | Output HIGH Voltage (Note 11) | 3855 | 3980 | 4105 | 3855 | 3980 | 4105 | 3855 | 3980 | 4105 | mV |
| $V_{OL}$ | Output LOW Voltage (Note 11) | 3005 | 3180 | 3305 | 3005 | 3180 | 3305 | 3005 | 3180 | 3305 | mV |
| $V_{IH}$ | Input HIGH Voltage (Single−Ended) | 3775 | | 4120 | 3775 | | 4120 | 3775 | | 4120 | mV |
| $V_{IL}$ | Input LOW Voltage (Single−Ended) | 3005 | | 3375 | 3005 | | 3375 | 3005 | | 3375 | mV |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 12) | 2.0 | | 5.0 | 2.0 | | 5.0 | 2.0 | | 5.0 | V |
| $I_{IH}$ | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| $I_{IL}$ | Input LOW Current | 0.5 | | | 0.5 | | | 0.5 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

10. Input and output parameters vary 1:1 with $V_{CC}$. $V_{EE}$ can vary +2.0 V to −0.5 V.
11. All loading with 50 Ω to $V_{CC}$ − 2.0 V.
12. $V_{IHCMR}$ min varies 1:1 with $V_{EE}$, $V_{IHCMR}$ max varies 1:1 with $V_{CC}$. The $V_{IHCMR}$ range is referenced to the most positive side of the differential input signal.

## Table 9. 100EP DC CHARACTERISTICS, NECL $V_{CC} = 0$ V, $V_{EE} = -5.5$ V to $-3.0$ V (Note 13)

| Symbol | Characteristic | −40°C Min | −40°C Typ | −40°C Max | 25°C Min | 25°C Typ | 25°C Max | 85°C Min | 85°C Typ | 85°C Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_{EE}$ | Power Supply Current | 85 | 105 | 135 | 85 | 105 | 135 | 85 | 105 | 135 | mA |
| $V_{OH}$ | Output HIGH Voltage (Note 14) | −1145 | −1020 | −895 | −1145 | −1020 | −895 | −1145 | −1020 | −895 | mV |
| $V_{OL}$ | Output LOW Voltage (Note 14) | −1995 | −1820 | −1695 | −1995 | −1820 | −1695 | −1995 | −1820 | −1695 | mV |
| $V_{IH}$ | Input HIGH Voltage (Single−Ended) | −1225 | | −880 | −1225 | | −880 | −1225 | | −880 | mV |
| $V_{IL}$ | Input LOW Voltage (Single−Ended) | −1995 | | −1625 | −1995 | | −1625 | −1995 | | −1625 | mV |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 15) | $V_{EE}$+2.0 | | 0.0 | $V_{EE}$+2.0 | | 0.0 | $V_{EE}$+2.0 | | 0.0 | V |
| $I_{IH}$ | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| $I_{IL}$ | Input LOW Current | 0.5 | | | 0.5 | | | 0.5 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

13. Input and output parameters vary 1:1 with $V_{CC}$.
14. All loading with 50 Ω to $V_{CC} - 2.0$ V.
15. $V_{IHCMR}$ min varies 1:1 with $V_{EE}$, $V_{IHCMR}$ max varies 1:1 with $V_{CC}$. The $V_{IHCMR}$ range is referenced to the most positive side of the differential input signal.

## Table 10. AC CHARACTERISTICS $V_{CC} = 0$ V; $V_{EE} = -3.0$ V to $-5.5$ V or $V_{CC} = 3.0$ V to 5.5 V; $V_{EE} = 0$ V (Note 16)

| Symbol | Characteristic | | −40°C Min | −40°C Typ | −40°C Max | 25°C Min | 25°C Typ | 25°C Max | 85°C Min | 85°C Typ | 85°C Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $V_{OUTpp}$ | Output Voltage Amplitude @ 3 GHz (Figure 4) (Note 17) | | 540 | 670 | | 520 | 650 | | 450 | 580 | | mV |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay to Output Differential | CLK to Q, $\overline{Q}$ MR to Q, $\overline{Q}$ | 330 430 | 430 530 | 530 630 | 350 450 | 450 550 | 550 650 | 390 490 | 490 590 | 590 690 | ps |
| $t_{RR}$ | Reset Recovery | MR to CLK | 240 | 145 | | 250 | 150 | | 260 | 160 | | ps |
| $t_S$ $t_H$ | Setup Time Hold Time | D to CLK CLK to D | 80 80 | 40 40 | | 80 80 | 40 40 | | 80 80 | 40 40 | | ps |
| $t_{PW}$ | Minimum Pulse Rate | MR | 400 | | | 400 | | | 400 | | | ps |
| $t_{SKEW}$ | Within−Device Skew (Note 18) Device−To−Device Skew (Note 19) | | | 20 35 | 40 100 | | 20 35 | 40 100 | | 20 35 | 40 100 | |
| $t_{JITTER}$ | CLOCK Random Jitter (RMS) @ ≤3.0 GHz (Figure 4) | | | 0.2 | 1 | | 0.2 | 1 | | 0.2 | 1 | ps |
| $t_r$ $t_f$ | Output Rise/Fall Times (20% – 80%) | Q, $\overline{Q}$ | 100 100 | 150 150 | 250 250 | 110 110 | 160 160 | 260 260 | 130 130 | 180 180 | 280 280 | ps |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

16. Measured using a 750 mV source, 50% duty cycle clock source. All loading with 50 Ω to $V_{CC} - 2.0$ V.
17. $V_{OL}$ and $V_{OH}$ specifications not guaranteed for $F_{max}$ testing.
18. Skew is measured between outputs under identical transitions and conditions on any one device.
19. Device−To−Device skew for identical transitions at identical $V_{CC}$ levels.
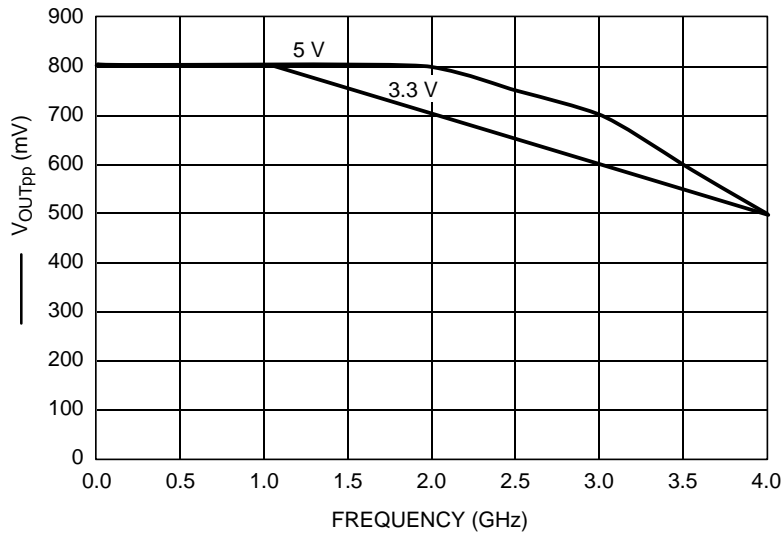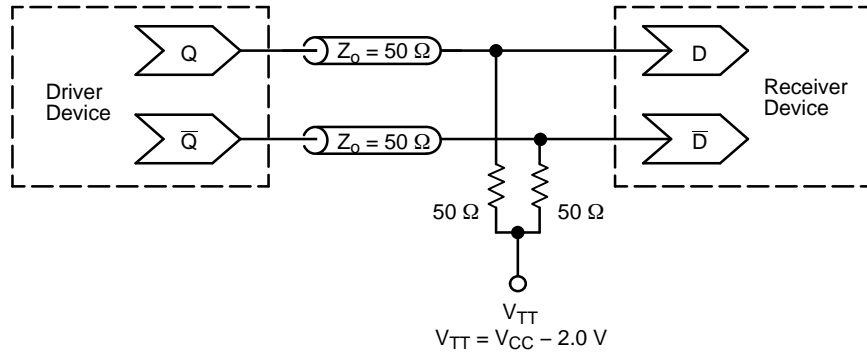
**Figure 4. F$_{max}$ Typical**



**Figure 5. Typical Termination for Output Driver and Device Evaluation**
**(See Application Note AND8020/D – Termination of ECL Logic Devices.)**

**ORDERING INFORMATION**

| Device | Package | Shipping† |
|---|---|---|
| MC10EP451FAG | LQFP–32 (Pb–Free) | 250 Units / Tray |
| MC10EP451FAR2G | | 2000 / Tape & Reel |
| MC10EP451MNG | QFN–32 (Pb–Free) | 72 Units / Tray |
| MC10EP451MNR4G | | 1000 / Tape & Reel |
| MC100EP451FAG | LQFP–32 (Pb–Free) | 250 Units / Tray |
| MC100EP451FAR2G | | 2000 / Tape & Reel |
| MC100EP451MNG | QFN–32 (Pb–Free) | 72 Units / Tray |
| MC100EP451MNR4G | | 1000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

**Resource Reference of Application Notes**

**AN1405/D** – ECL Clock Distribution Techniques

**AN1406/D** – Designing with PECL (ECL at +5.0 V)

**AN1503/D** – ECLinPS™ I/O SPiCE Modeling Kit

**AN1504/D** – Metastability and the ECLinPS Family

**AN1568/D** – Interfacing Between LVDS and ECL

**AN1642/D** – The ECL Translator Guide

**AND8001/D** – Odd Number Counters Design

**AND8002/D** – Marking and Date Codes

**AND8020/D** – Termination of ECL Logic Devices

**AND8066/D** – Interfacing with ECLinPS

**AND8090/D** – AC Characteristics of ECL Devices

## PACKAGE DIMENSIONS

**32 LEAD LQFP**
CASE 873A–02
ISSUE C

DETAIL Y

DETAIL AD

SECTION AE–AE

DETAIL AD
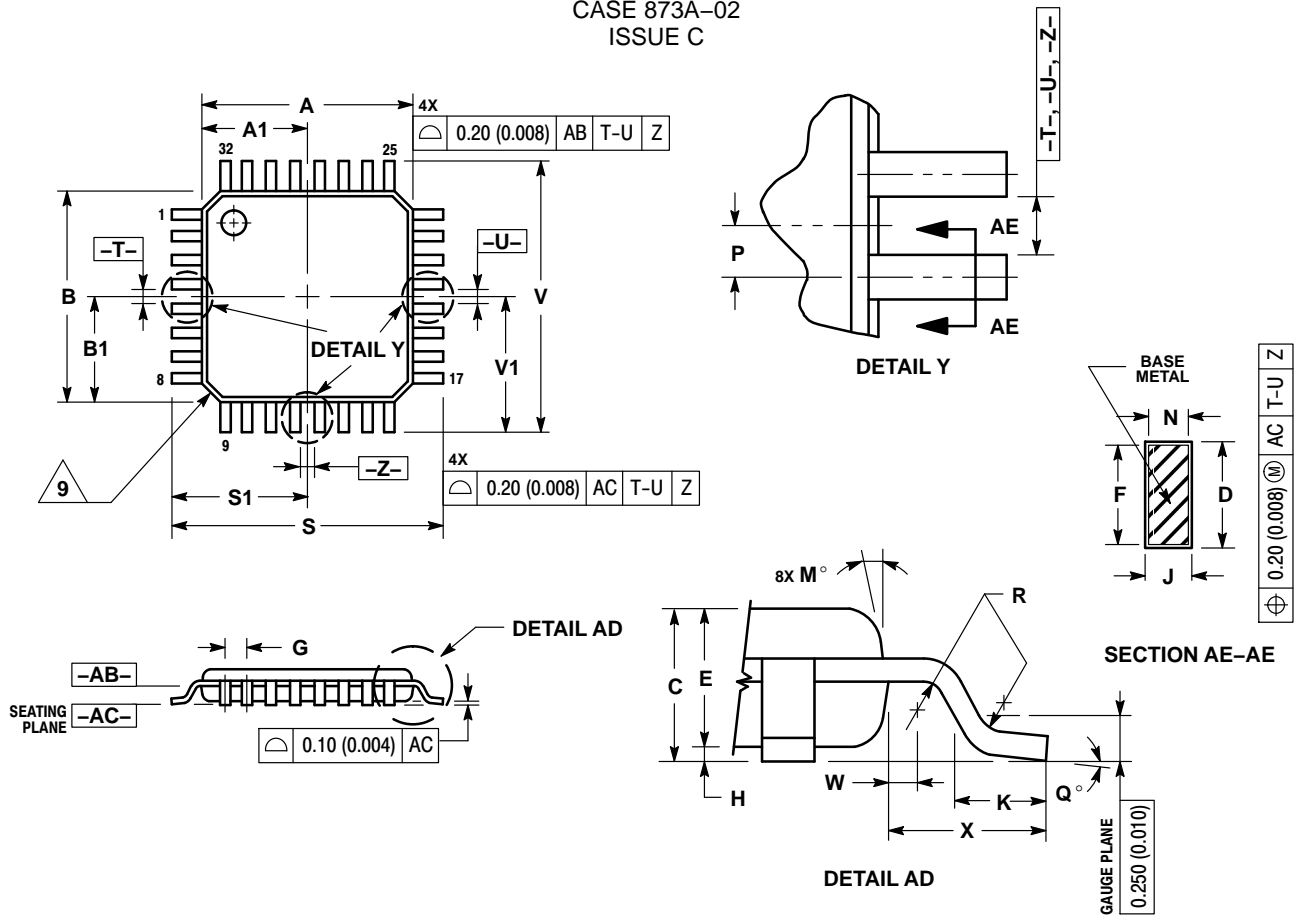
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –AB– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –T–, –U–, AND –Z– TO BE DETERMINED AT DATUM PLANE –AB–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –AC–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –AB–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.520 (0.020).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

| DIM | MILLIMETERS | | INCHES | |
|-----|------|------|------|------|
|     | MIN  | MAX  | MIN  | MAX  |
| A   | 7.000 BSC | | 0.276 BSC | |
| A1  | 3.500 BSC | | 0.138 BSC | |
| B   | 7.000 BSC | | 0.276 BSC | |
| B1  | 3.500 BSC | | 0.138 BSC | |
| C   | 1.400 | 1.600 | 0.055 | 0.063 |
| D   | 0.300 | 0.450 | 0.012 | 0.018 |
| E   | 1.350 | 1.450 | 0.053 | 0.057 |
| F   | 0.300 | 0.400 | 0.012 | 0.016 |
| G   | 0.800 BSC | | 0.031 BSC | |
| H   | 0.050 | 0.150 | 0.002 | 0.006 |
| J   | 0.090 | 0.200 | 0.004 | 0.008 |
| K   | 0.450 | 0.750 | 0.018 | 0.030 |
| M   | 12° REF | | 12° REF | |
| N   | 0.090 | 0.160 | 0.004 | 0.006 |
| P   | 0.400 BSC | | 0.016 BSC | |
| Q   | 1° | 5° | 1° | 5° |
| R   | 0.150 | 0.250 | 0.006 | 0.010 |
| S   | 9.000 BSC | | 0.354 BSC | |
| S1  | 4.500 BSC | | 0.177 BSC | |
| V   | 9.000 BSC | | 0.354 BSC | |
| V1  | 4.500 BSC | | 0.177 BSC | |
| W   | 0.200 REF | | 0.008 REF | |
| X   | 1.000 REF | | 0.039 REF | |

## PACKAGE DIMENSIONS

**QFN32 5x5, 0.5P**
CASE 488AM
ISSUE A
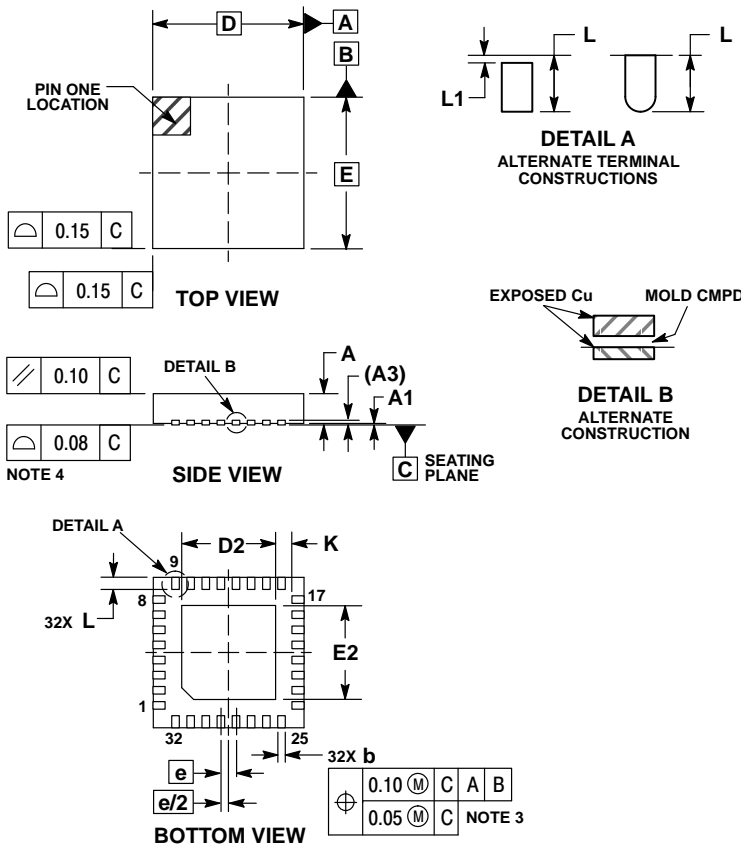
NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| DIM | MILLIMETERS | |
| --- | --- | --- |
| | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | ––– | 0.05 |
| A3 | 0.20 REF | |
| b | 0.18 | 0.30 |
| D | 5.00 BSC | |
| D2 | 2.95 | 3.25 |
| E | 5.00 BSC | |
| E2 | 2.95 | 3.25 |
| e | 0.50 BSC | |
| K | 0.20 | ––– |
| L | 0.30 | 0.50 |
| L1 | ––– | 0.15 |

**TOP VIEW**

**DETAIL A**
ALTERNATE TERMINAL CONSTRUCTIONS

**DETAIL B**
ALTERNATE CONSTRUCTION

**SIDE VIEW**

**BOTTOM VIEW**

**RECOMMENDED SOLDERING FOOTPRINT\***

DIMENSION: MILLIMETERS
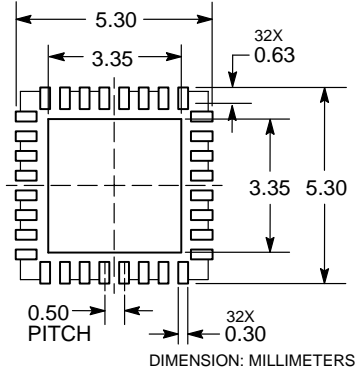
*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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**MC10EP451/D**