Triple Noninverting Schmitt-Trigger Buffer

The NL37WZ17 is a high performance buffer with Schmitt-Trigger inputs operating from a 1.65 to 5.5 V supply.

The NL37WZ17 can be used as a line receiver which will receive slow input signals. The NL37WZ17 is capable of transforming slowly changing input signals into sharply defined, jitter—free output signals. In addition, it has a greater noise margin than conventional inverters. The NL37WZ17 has hysteresis between the positive—going and the negative—going input thresholds (typically 1.0 V) which is determined internally by transistor ratios and is essentially insensitive to temperature and supply voltage variations.

Features

- Designed for 1.65 V to 5.5 V V_{CC} Operation
- Over Voltage Tolerant Inputs and Outputs
- LVTTL Compatible Interface Capability with 5 V TTL Logic with V_{CC} = 3 V
- LVCMOS Compatible
- 24 mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current Substantially Reduces System Power Requirements
- Current Drive Capability is 24 mA at the Outputs
- Chip Complexity: FET = 94
- Pb–Free Package is Available

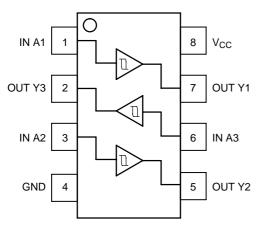


Figure 1. Pinout

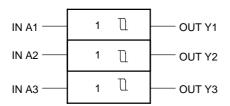
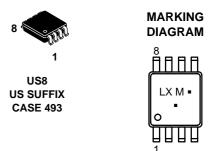


Figure 2. Logic Symbol



ON Semiconductor®

http://onsemi.com



LX = Device Code

M = Date Code*

= Pb-Free Package

= PD-Free Package(Note: Microdot may be in either location)

*Date Code orientation may vary depending upon manufacturing location.

PIN ASSIGNMENT

1	IN A1
2	OUT Y3
3	IN A2
4	GND
5	OUT Y2
6	IN A3
7	OUT Y1
8	V _{CC}

FUNCTION TABLE

A Input	∀ Output
L	L
Н	н

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

MAXIMUM RATINGS

Symbol		Parameter	Value	Unit
V _{CC}	DC Supply Voltage	OC Supply Voltage		V
VI	DC Input Voltage		$-0.5 \le V_1 \le +7.0$	V
Vo	DC Output Voltage	Output in Z or LOW State (Note 1)	$-0.5 \le V_O \le 7.0$	V
I _{IK}	DC Input Diode Current	V _I < GND	-50	mA
I _{OK}	DC Output Diode Current	V _O < GND	-50	mA
Io	DC Output Sink Current		±50	mA
I _{CC}	DC Supply Current per Supply	Pin	±100	mA
I _{GND}	DC Ground Current per Ground	d Pin	±100	mA
T _{STG}	Storage Temperature Range		-65 to +150	°C
TL	Lead Temperature, 1 mm from	Case for 10 Seconds	260	°C
TJ	Junction Temperature under Bi	as	+ 150	°C
θ_{JA}	Thermal Resistance	(Note 2)	333	°C/W
P _D	Power Dissipation in Still Air at	85°C	200	mW
MSL	Moisture Sensitivity		Level 1	
F _R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	
V _{ESD}	ESD Withstand Voltage	Human Body Model (Note 3) Machine Model (Note 4) Charged Device Model (Note 5)	> 2000 > 200 N/A	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

- I_O absolute maximum rating must be observed.
 Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2-ounce copper trace with no air flow.
- 3. Tested to EIA/JESD22-A114-A.
- 4. Tested to EIA/JESD22-A115-A.
- 5. Tested to JESD22-C101-A.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	Supply Voltage	Operating Data Retention Only	2.3 1.5	5.5 5.5	V
VI	Input Voltage	(Note 6)	0	5.5	V
Vo	Output Voltage	(HIGH or LOW State)	0	5.5	V
T _A	Operating Free-Air Temperature		-40	+85	°C
Δt/ΔV	Input Transition Rise or Fall Rate	$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$ $V_{CC} = 3.0 \text{ V} \pm 0.3 \text{ V}$ $V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$	0 0 0	No Limit No Limit No Limit	ns/V

6. Unused inputs may not be left open. All inputs must be tied to a high-logic voltage level or a low-logic input voltage level.

DC ELECTRICAL CHARACTERISTICS

Symbol Parameter Condition (V) Min Typ Max Min Max Unit				V _{CC}	T _A = 25°C		-40°C ≤ 7	Γ _A ≤ 85°C		
Voltage 2.7 1.2 1.7 2.0 1.2 2.0 3.0 1.3 1.9 2.2 1.3 2.2 4.5 1.9 2.7 3.1 1.9 3.1 5.5 2.2 3.3 3.6 2.2 3.6 3.6 3.7 3.1	Symbol	Parameter	Condition		Min	Тур	Max	Min	Max	Unit
V _T	V _T +			2.3	1.0	1.5	1.8	1.0	1.8	V
V _T		voitage		2.7	1.2	1.7	2.0	1.2	2.0	
V _T				3.0	1.3	1.9	2.2	1.3	2.2	
V _T				4.5	1.9	2.7	3.1	1.9	3.1	
Voltage Vol				5.5	2.2	3.3	3.6	2.2	3.6	
2.7 0.5 0.87 1.4 0.5 1.4 0.5 1.4 0.5 1.4 0.5 1.5 0.6 0.6 1.5 0.6 0.	V _T -			2.3	0.4	0.75	1.15	0.4	1.15	V
V _H Input Hysteresis Voltage V _{IN} = V _{IL} Output Voltage V _{IN} = V _{IH} or V _{IL} Input P _I V _{IL} Output Voltage V _{IN} = V _I Output Voltage		voltage		2.7	0.5	0.87	1.4	0.5	1.4	
No				3.0	0.6	1.0	1.5	0.6	1.5	
V _H Input Hysteresis Voltage				4.5	1.0	1.5	2.0	1.0	2.0	
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$				5.5	1.2	1.9	2.3	1.2	2.3	
Note	V _H	Input Hysteresis Voltage		2.3	0.25	0.75	1.1	0.25	1.1	V
Voh High-Level Output Voltage I _{OH} = -100 μA 1.65 to 5.5 V _{CC} = 0.1 V _{CC} V _{CC} V _{CC} = 0.1 V _{CC} V _{CC} V _{CC} V _{CC} = 0.1 V _{CC} V _{CC} V _{CC} V _{CC} = 0.1 V _{CC} V _{CC}				2.7	0.3	0.83	1.15	0.3	1.15	
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$				3.0	0.4	0.93	1.2	0.4	1.2	
$\begin{array}{c} V_{OH} \\ V_{IN} = V_{IH} \text{ or } V_{IL} \\ V_{IN} = V_{IH} \text{ or } V_{IL} \\ \end{array} \begin{array}{c} I_{OH} = -100 \ \mu A \\ I_{OH} = -3 \ mA \\ I_{OH} = -8 \ mA \\ I_{OH} = -12 \ mA \\ I_{OH} = -12 \ mA \\ I_{OH} = -24 \ mA \\ I_{OH} = -32 \ mA \\ \end{array} \begin{array}{c} 2.3 \\ 2.2 \\ 2.4 \\ 2.7 \\ 2.4 \\ 2.3 \\ 2.5 \\ 2.3 \\ 3.8 \\ \end{array} \begin{array}{c} 2.4 \\ 2.2 \\ 2.4 \\ 2.2 \\ 2.4 \\ 2.2 \\ 2.4 \\ 2.2 \\ 2.4 \\ 2.2 \\ 2.4 \\ 2.2 \\ 2.4 \\ 2.2 \\ 2.4 \\ 2.2 \\ 2.4 \\ 2.2 \\ 2.4 \\ 2.2 \\ 2.4 \\ 2.2 \\ 2.4 \\ 2.2 \\ 2.4 \\ 2.2 \\ 2.4 \\ 2.2 \\ 2.3 \\ 3.8 \\ 4.0 \\ \end{array} \\ \begin{array}{c} V_{OL} \\ V_{OL} \\ V_{IN} = V_{IH} \text{ or } V_{IL} \\ \end{array} \begin{array}{c} I_{OL} = 100 \ \mu A \\ I_{OL} = 100 \ \mu A \\ I_{OL} = 4 \ mA \\ I_{OL} = 8 \ mA \\ 2.3 \\ I_{OL} = 12 \ mA \\ I_{OL} = 12 \ mA \\ I_{OL} = 100 \ \mu A \\ I_{OL} = $				4.5	0.6	1.2	1.5	0.6	1.5	
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$				5.5	0.7	1.4	1.7	0.7	1.7	
I _{OH} = -3 mA	V _{OH}	High-Level Output Voltage	I _{OH} = -100 μA	1.65 to 5.5	V _{CC} -0.1	V_{CC}		V _{CC} −0.1		V
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$		VIN = VIH OI VIL	$I_{OH} = -3 \text{ mA}$	1.65	1.29	1.52		1.29		
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$			$I_{OH} = -8 \text{ mA}$	2.3	1.9	2.1		1.9		
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$			$I_{OH} = -12 \text{ mA}$	2.7	2.2	2.4		2.2		
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$			$I_{OH} = -16 \text{ mA}$	3.0	2.4	2.7		2.4		
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$			$I_{OH} = -24 \text{ mA}$	3.0	2.3	2.5		2.3		
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$			$I_{OH} = -32 \text{ mA}$	4.5	3.8	4.0		3.8		
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	V _{OL}	Low-Level Output Voltage	I _{OL} = 100 μA	1.65 to 5.5			0.1		0.1	V
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$		$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 4 \text{ mA}$	1.65		0.08	0.24		0.24	
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$			$I_{OL} = 8 \text{ mA}$	2.3		0.2	0.3		0.3	
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$			I _{OL} = 12 mA	2.7		0.22	0.4		0.4	
$I_{OL} = 32 \text{ mA}$ 4.5 0.42 0.55 0.55 I_{IN} Input Leakage Current $V_{IN} = V_{CC}$ or GND 0 to 5.5 ± 0.1 ± 1.0 μ I_{OFF} Power Off–Output Leakage $V_{OUT} = 5.5 V$ 0 1 1 10 μ			I _{OL} = 16 mA	3.0		0.28	0.4		0.4	
I_{IN} Input Leakage Current $V_{IN} = V_{CC}$ or GND 0 to 5.5 ± 0.1 ± 1.0 μ I_{OFF} Power Off–Output Leakage $V_{OUT} = 5.5$ V 0 1 1 10 μ			I _{OL} = 24 mA	3.0		0.38	0.55		0.55	
I_{OFF} Power Off–Output Leakage $V_{OUT} = 5.5 \text{ V}$ 0 1 10 μ			I _{OL} = 32 mA	4.5		0.42	0.55		0.55	
	I _{IN}	Input Leakage Current	$V_{IN} = V_{CC}$ or GND	0 to 5.5			±0.1		±1.0	μΑ
	l _{OFF}	Power Off-Output Leakage Current	V _{OUT} = 5.5 V	0			1		10	μΑ
I_{CC} Quiescent Supply Current $V_{IN} = V_{CC}$ or GND 5.5 1 1 10 μ	I _{CC}	Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND	5.5			1		10	μΑ

AC ELECTRICAL CHARACTERISTICS (Input $t_{\text{f}} = t_{\text{f}} = 3.0 \text{ ns}$)

			V _{CC}	-	T _A = 25°C		$-40^{\circ}\text{C}\leqT_{A}\leq85^{\circ}\text{C}$		
Symbol	Parameter	Condition	(V)	Min	Тур	Max	Min	Max	Unit
t _{PLH}	Propagation Delay	$R_L = 1 \text{ M}\Omega$, $C_L = 15 \text{ pF}$	2.5 ± 0.2	1.8	4.3	7.4	1.8	8.1	ns
t _{PHL}	Input A to Y (Figures 3 and 4)	$R_L = 1 \text{ M}\Omega$, $C_L = 15 \text{ pF}$	3.3 ± 0.3	1.5	3.3	5.0	1.5	5.5	
		$R_L = 500 \Omega, C_L = 50 pF$		1.8	4.0	5.0	1.8	6.6	
		$R_L = 1 \text{ M}\Omega$, $C_L = 15 \text{ pF}$	5.0 ± 0.5	1.0	2.7	4.1	1.0	4.5	
		$R_L = 500 \Omega, C_L = 50 pF$		1.2	3.2	4.9	1.2	5.4	

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C _{IN}	Input Capacitance	$V_{CC} = 5.5 \text{ V}, V_I = 0 \text{ V or } V_{CC}$	2.5	pF
C _{PD}	Power Dissipation Capacitance	10 MHz, V_{CC} = 3.3 V, V_{I} = 0 V or V_{CC}	9	pF
	(Note 7)	10 MHz, V_{CC} = 5.5 V, V_{I} = 0 V or V_{CC}	11	

^{7.} C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}. C_{PD} is used to determine the no–load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

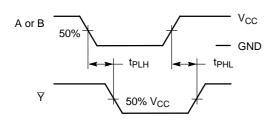
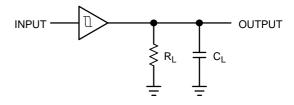


Figure 3. Switching Waveforms



A 1–MHz square input wave is recommended for propagation delay tests.

Figure 4. Test Circuit

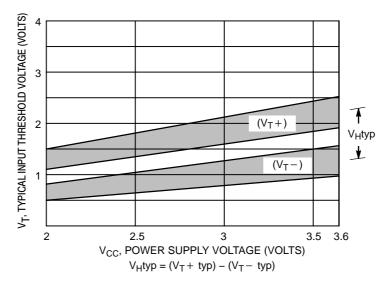
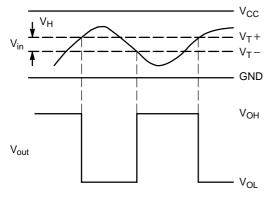
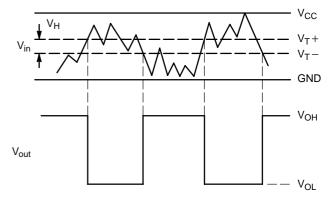


Figure 5. Typical Input Threshold, $V_T +$, $V_T -$ versus Power Supply Voltage





(a) A Schmitt–Trigger Squares Up Inputs With Slow Rise and Fall Times

(b) A Schmitt-Trigger Offers Maximum Noise Immunity

Figure 6. Typical Schmitt-Trigger Applications

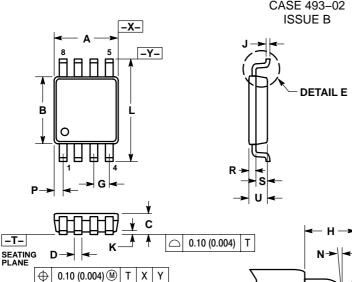
DEVICE ORDERING INFORMATION

Device Order Number	Package Type	Tape and Reel Size [†]
NL37WZ17US	US8	178 mm, 3000 Units / Tape & Reel
NL37WZ17USG	US8 (Pb-Free)	178 mm, 3000 Units / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

US8 US SUFFIX CASE 493-02 ISSUE B



NOTES:

R 0.10 TYP

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSION "A" DOES NOT INCLUDE MOLD
- DIMENSION "A" DOES NOT INCLUDE MOL FLASH, PROTRUSION OR GATE BURR. MOLD FLASH. PROTRUSION AND GATE BURR SHALL NOT EXCEED 0.140 MM (0.0055") PER SIDE.
- (0.0055") PER SIDE.

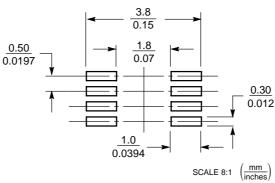
 4. DIMENSION "B" DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSION. INTER-LEAD FLASH AND PROTRUSION SHALL NOT E3XCEED 0.140 (0.0055") PER SIDE.
- 5. LEAD FINISH IS SOLDER PLATING WITH THICKNESS OF 0.0076–0.0203 MM. (300–800 °). 6. ALL TOLERANCE UNLESS OTHERWISE
- ALL TOLERANCE UNLESS OTHERWISE SPECIFIED ±0.0508 (0.0002 ").

	MILLIMETERS		INC	HES
DIM	MIN	MAX	MIN	MAX
Α	1.90	2.10	0.075	0.083
В	2.20	2.40	0.087	0.094
С	0.60	0.90	0.024	0.035
D	0.17	0.25	0.007	0.010
F	0.20	0.35	0.008	0.014
G	0.50	BSC	0.020	BSC
Н	0.40	REF	0.016	REF
J	0.10	0.18	0.004	0.007
K	0.00	0.10	0.000	0.004
L	3.00	3.20	0.118	0.126
M	0 °	6 °	0 °	6 °
N	5 °	10 °	5 °	10 °
Р	0.23	0.34	0.010	0.013
R	0.23	0.33	0.009	0.013
S	0.37	0.47	0.015	0.019
U	0.60	0.80	0.024	0.031
V	0.12	BSC	0.005	BSC

SOLDERING FOOTPRINT*

DETAIL E

F



*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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