MC74ACT564

Octal D-Type Flip-Flop with 3-State Outputs

The MC74ACT564 is a high−speed, low power octal flip−flop with a buffered common Clock (CP) and a buffered common Output Enable ($\overline{OE}$).

The information presented to the D inputs is stored in the flip−flops on the LOW−to−HIGH Clock (CP) transition.

The MC74ACT564 device is functionally indentical to the MC74ACT574, but with inverted outputs.

Features

- Inputs and Outputs on the Opposite Sides of the Package Allowing Easy Interface with Microprocessors
- Useful as Input or Output Port for Microprocessor
- Functionally Indentical to the MC74ACT574 but with Inverted Outputs
- 3−State Outputs for Bus−Oriented Applications
- Outputs Source/Sink 24 mA
- TTL Compatible Inputs
- Pb−Free Packages are Available*

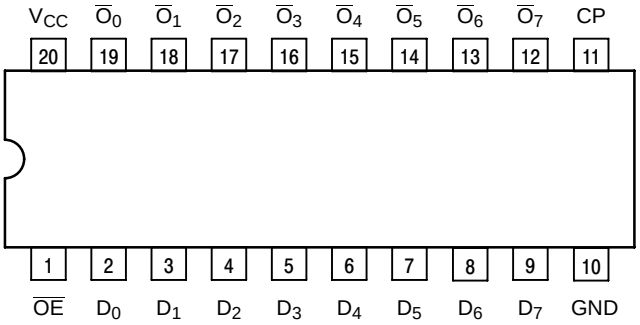

Figure 1. Pinout: 20−Lead Packages Conductors
(Top View)

PIN ASSIGNMENT

PIN	FUNCTION
D_0−D_7	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	3−State Output Enable Input
$\overline{O}_0$−$\overline{O}_7$	3−State Outputs

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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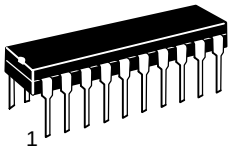
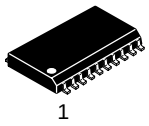


PDIP−20
N SUFFIX
CASE 738



SOIC−20W
DW SUFFIX
CASE 751D

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 5 of this data sheet.

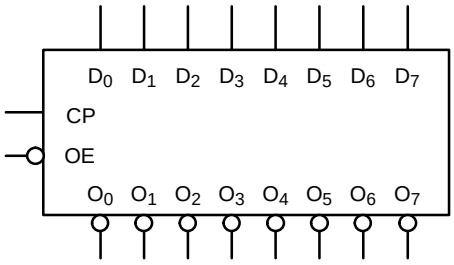
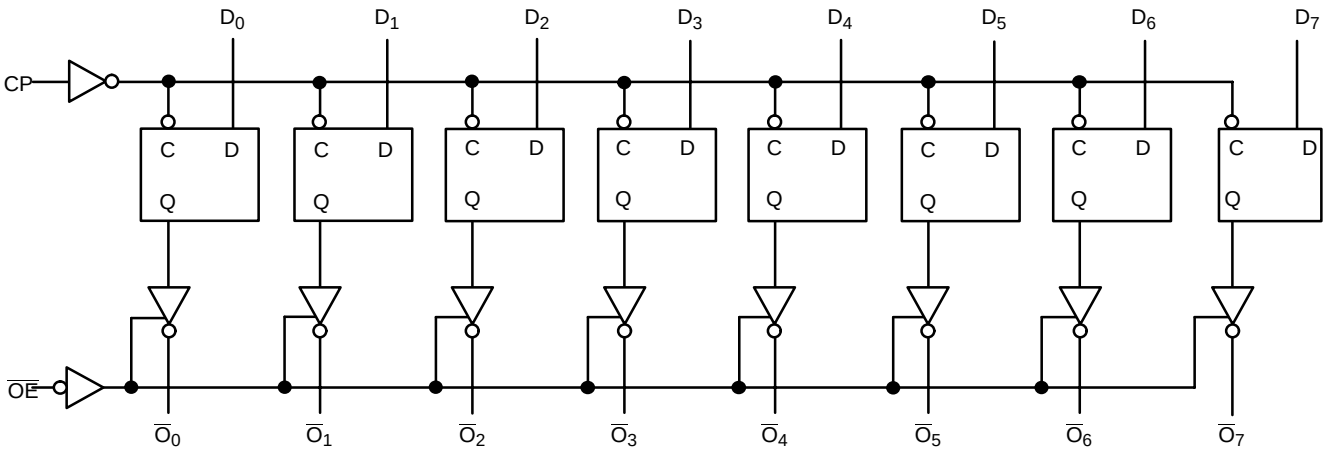


Figure 2. Logic Symbol



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Figure 3. Logic Diagram

FUNCTION TABLE

Inputs			Internal	Outputs	Function
$\overline{OE}$	CP	D	Q	O	
H	H	L	NC	Z	Hold
H	H	H	NC	Z	Hold
H	⌐¬	L	H	Z	Load
H	⌐¬	H	L	Z	Load
L	⌐¬	L	H	H	Data Available
L	⌐¬	H	L	L	Data Available
L	H	L	NC	NC	No Change in Data
L	H	H	NC	NC	No Change in Data

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
⌐¬ = LOW−to−HIGH Transition
NC = No Change

FUNCTIONAL DESCRIPTION

The MC74ACT564 consists of eight edge−triggered flip−flops with individual D−type inputs and 3−state complementary outputs. The buffered clock and buffered Output Enable are common to all flip−flops. The eight flip−flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW−to−HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip−flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip−flops.

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to +7.0	V
V_I	DC Input Voltage		$-0.5 \le V_I \le V_{CC} + 0.5$	V
V_O	DC Output Voltage (Note 1)		$-0.5 \le V_O \le V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current		±20	mA
I_{OK}	DC Output Diode Current		±50	mA
I_O	DC Output Sink/Source Current		±50	mA
I_{CC}	DC Supply Current per Output Pin		±50	mA
I_{GND}	DC Ground Current per Output Pin		±50	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
T_J	Junction Temperature under Bias		+150	°C
θ_{JA}	Thermal Resistance	PDIP SOIC	67 96	°C/W
P_D	Power Dissipation in Still Air at 85°C	PDIP SOIC	750 500	mW
MSL	Moisture Sensitivity		Level 1	
F_R	Flammability Rating	Oxygen Index: 30% − 35%	UL 94−V0 @ 0.125 in	
V_{ESD}	ESD Withstand Voltage	Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	> 2000 > 200 > 1000	V
$I_{Latchup}$	Latchup Performance	Above V_{CC} and Below GND at 85°C (Note 5)	±100	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. I_O absolute maximum rating must be observed.
2. Tested to EIA/JESD22−A114−A.
3. Tested to EIA/JESD22−A115−A.
4. Tested to JESD22−C101−A.
5. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	DC Input Voltage (Referenced to GND)		4.5		5.5	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0		V_{CC}	V
T_A	Operating Temperature, All Package Types		−40	25	+85	°C
t_r, t_f	Input Rise and Fall Time (Note 7)	V_{CC} = 4.5 V V_{CC} = 5.5 V	0 0	10 8.0	10 8.0	ns/V
T_J	Junction Temperature (PDIP)				140	°C
I_{OH}	Output Current − High				−24	mA
I_{OL}	Output Current − Low				24	mA

6. Unused Inputs may not be left open. All inputs must be tied to a high voltage level or low logic voltage level.
7. V_{in} from 0.8 V to 2.0 V; refer to individual Data Sheets for devices that differ from the typical input rise and fall times.

DC CHARACTERISTICS

Symbol	Parameter	V_{CC} (V)	T_A = +25°C Typ	T_A = −40°C to +85°C Guaranteed Limits		Unit	Conditions
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V V	V_{OUT} = 0.1 V or V_{CC} − 0.1 V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V V	V_{OUT} = 0.1 V or V_{CC} − 0.1 V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	V V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.76 4.76	V V	*V_{IN} = V_{IL} or V_{IH} −24 mA I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.44 0.44	V V	*V_{IN} = V_{IL} or V_{IH} 24 mA I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V_I = V_{CC}, GND
ΔI_{CCT}	Additional Max. I_{CC}/Input	5.5	0.6		1.5	mA	V_I = V_{CC} − 2.1 V
I_{OZ}	Maximum 3−State Current	5.5		±0.5	±5.0	μA	V_I (OE) = V_{IL}, V_{IH} V_I = V_{CC}, GND V_O = V_{CC}, GND
I_{OLD} I_{OHD}	†Minimum Dynamic Output Current	5.5 5.5			75 −75	mA mA	V_{OLD} = 1.65 V Max V_{OHD} = 3.85 V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 2.0 ms, one output loaded at a time.

AC CHARACTERISTICS t_r = t_f = 3.0 ns (For Figures and Waveforms, See Figures 4, 5, and 6.)

Symbol	Parameter	V_{CC}* (V)	T_A = +25°C, C_L = 50 pF			T_A = −40°C to +85°C, C_L = 50 pF		Unit
			Min	Typ	Max	Min	Max	
f_{max}	Maximum Clock Frequency	5.0	85	−	−	75	−	MHz
t_{PLH}	Propagation Delay CP to $\overline{Q}_n$	5.0	2.0	−	10.5	1.5	11.5	ns
t_{PHL}	Propagation Delay CP to $\overline{Q}_n$	5.0	1.5	−	9.5	1.5	10.5	ns
t_{PZH}	Output Enable Time	5.0	1.5	−	9.0	1.5	9.5	ns
t_{PZL}	Output Enable Time	5.0	1.5	−	8.5	1.0	9.5	ns
t_{PHZ}	Output Disable Time	5.0	1.5	−	10.5	1.5	11.5	ns
t_{PLZ}	Output Disable Time	5.0	1.5	−	8.0	1.0	8.5	ns

*Voltage Range 5.0 V is 5.0 V ±0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter		V_{CC}* (V)	T_A = +25°C C_L = 50 pF	T_A = −40°C to +85°C C_L = 50 pF		Unit
				Typ	Guaranteed Minimum		
t_s	Setup Time, HIGH or LOW	D_n to C_P	5.0	−	2.5	3.0	ns
t_h	Hold Time, HIGH or LOW	D_n to C_P	5.0	−	1.0	1.0	ns
t_w	C_P Pulse Width	HIGH or LOW	5.0	−	3.0	3.5	ns

*Voltage Range 3.3 V is 3.3 V ±0.3 V.
*Voltage Range 5.0 V is 5.0 V ±0.5 V.

CAPACITANCE

Symbol	Parameter	Value Typ	Unit	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	50	pF	V_{CC} = 5.0 V

ORDERING INFORMATION

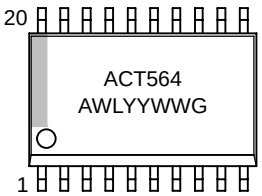
Device	Package	Shipping†
MC74ACT564N	PDIP−20	18 Units / Rail
MC74ACT564NG	PDIP−20 (Pb−Free)	
MC74ACT564DWR2	SOIC−20	1000 / Tape & Reel
MC74ACT564DWR2G	SOIC−20 (Pb−Free)	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MARKING DIAGRAMS

PDIP−20

SOIC−20W



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

SWITCHING WAVEFORMS

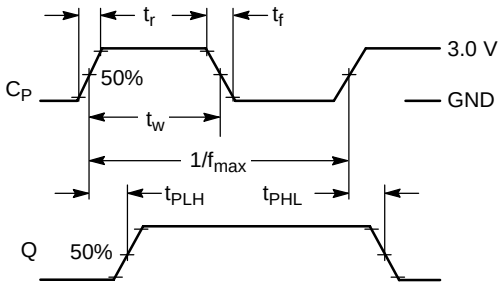


Figure 4.

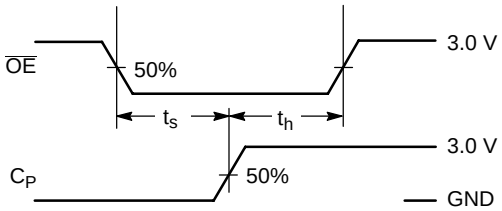


Figure 5.

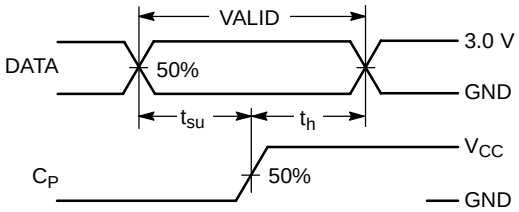
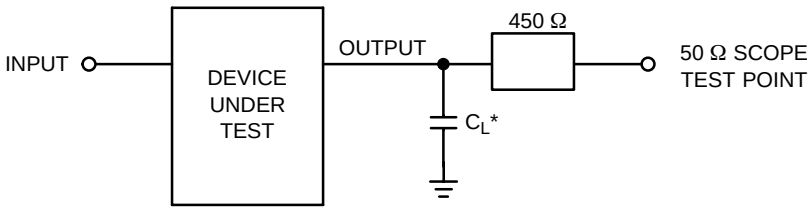


Figure 6.

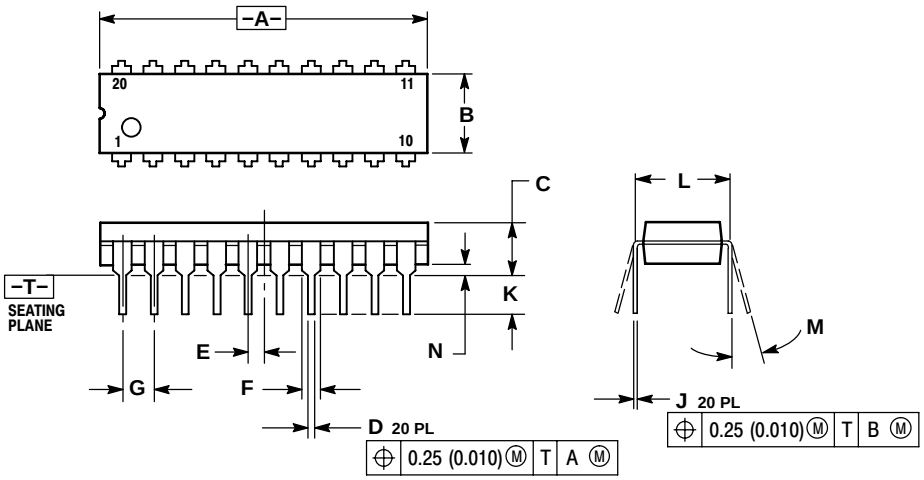


*Includes all probe and jig capacitance

Figure 7. Test Circuit

PACKAGE DIMENSIONS

PDIP−20
N SUFFIX
PLASTIC DIP PACKAGE
CASE 738−03
ISSUE E



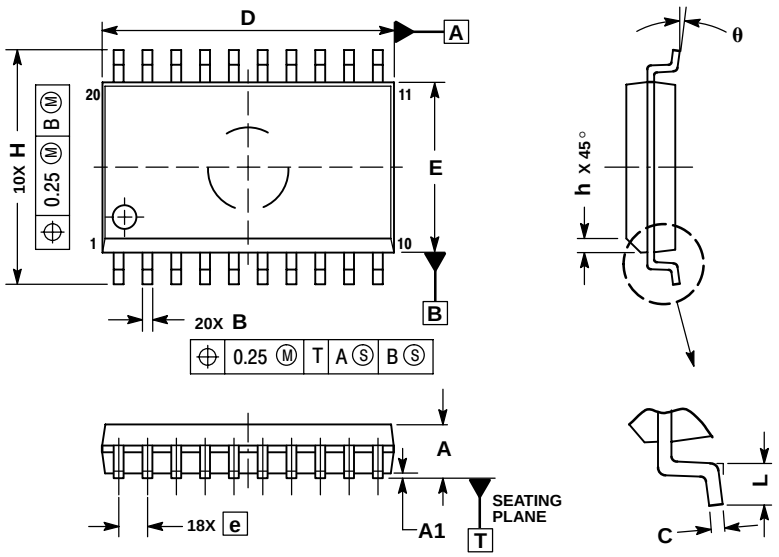
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.010	1.070	25.66	27.17
B	0.240	0.260	6.10	6.60
C	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
E	0.050 BSC		1.27 BSC	
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

MC74ACT564

PACKAGE DIMENSIONS

SOIC−20W
DW SUFFIX
CASE 751D−05
ISSUE G



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
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Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
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