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FAIRCHILD SEMICONDUCTOR®

April 2007

74ACQ374, 74ACTQ374
Quiet Series™ Octal D-Type Flip-Flop with 3-STATE Outputs

Features

- I_{CC} and I_{OZ} reduced by 50%
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Improved latch-up immunity
- Buffered positive edge-triggered clock
- 3-STATE outputs drive bus lines or buffer memory address registers
- Outputs source/sink 24mA
- Faster prop delays than the standard AC/ACT374

General Description

The ACQ/ACTQ374 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable ($\overline{OE}$) are common to all flip-flops.

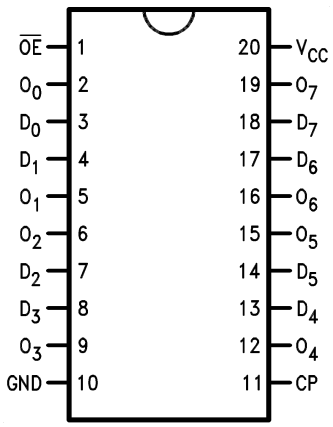
The ACQ/ACTQ374 utilizes FACT Quiet Series™ technology to guarantee quiet output switching and improve dynamic threshold performance. FACT Quiet Series features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

Ordering Information

Order Number	Package Number	Package Description
74ACQ374SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Body
74ACQ374SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ACTQ374SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Body
74ACTQ374SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ACTQ374QSC	MQA20	20-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

Connection Diagram



Pin Description

Pin Names	Description
D_0–D_7	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	3-STATE Output Enable Input
O_0–O_7	3-STATE Outputs

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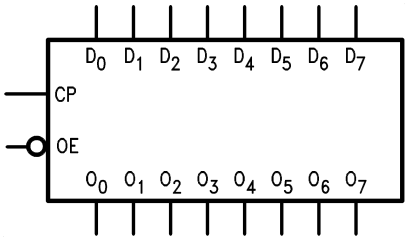
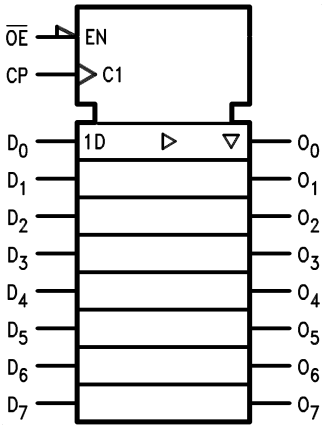
Logic Symbol



IEEE/IEC



Functional Description

The ACQ/ACTQ374 consists of eight edge-triggered flip-flops with individual D-type inputs and 3-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D-type inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Truth Table

Inputs			Outputs
D_n	CP	$\overline{OE}$	O_n
H	⌐	L	H
L	⌐	L	L
X	X	H	Z

H = HIGH Voltage Level

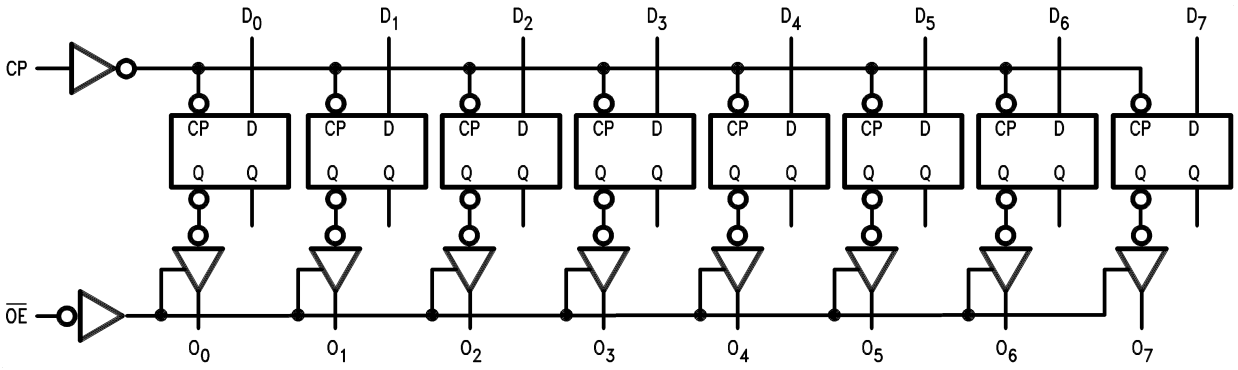
L = LOW Voltage Level

X = Immaterial

Z = High Impedance

⌐ = LOW-to-HIGH Transition

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

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Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	–0.5V to +7.0V
I_{IK}	DC Input Diode Current	
	$V_I = –0.5V$	–20mA
	$V_I = V_{CC} + 0.5V$	+20mA
V_I	DC Input Voltage	–0.5V to V_{CC} + 0.5V
I_{OK}	DC Output Diode Current	
	$V_O = –0.5V$	–20mA
	$V_O = V_{CC} + 0.5V$	+20mA
V_O	DC Output Voltage	–0.5V to V_{CC} + 0.5V
I_O	DC Output Source or Sink Current	±50mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current per Output Pin	±50mA
T_{STG}	Storage Temperature	–65°C to +150°C
	DC Latch-Up Source or Sink Current	±300mA
T_J	Junction Temperature	140°C

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	
	ACQ	2.0V to 6.0V
	ACTQ	4.5V to 5.5V
V_I	Input Voltage	0V to V_{CC}
V_O	Output Voltage	0V to V_{CC}
T_A	Operating Temperature	–40°C to +85°C
$\Delta V / \Delta t$	Minimum Input Edge Rate, ACQ Devices:	125mV/ns
	V_{IN} from 30% to 70% of V_{CC}, V_{CC} @ 3.0V, 4.5V, 5.5V	
$\Delta V / \Delta t$	Minimum Input Edge Rate, ACTQ Devices:	125mV/ns
	V_{IN} from 0.8V to 2.0V, V_{CC} @ 4.5V, 5.5V	

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DC Electrical Characteristics for ACQ

Symbol	Parameter	V_{CC} (V)	Conditions	T_A = +25°C	T_A = –40°C to +85°C		Units
				Typ.	Guaranteed Limits		
V_{IH}	Minimum HIGH Level Input Voltage	3.0	V_{OUT} = 0.1V or V_{CC} – 0.1V	1.5	2.1	2.1	V
		4.5		2.25	3.15	3.15	
		5.5		2.75	3.85	3.85	
V_{IL}	Maximum LOW Level Input Voltage	3.0	V_{OUT} = 0.1V or V_{CC} – 0.1V	1.5	0.9	0.9	V
		4.5		2.25	1.35	1.35	
		5.5		2.75	1.65	1.65	
V_{OH}	Minimum HIGH Level Output Voltage	3.0	I_{OUT} = –50µA	2.99	2.9	2.9	V
		4.5		4.49	4.4	4.4	
		5.5		5.49	5.4	5.4	
		3.0	V_{IN} = V_{IL} or V_{IH}: I_{OH} = –12mA		2.56	2.46	
		4.5	I_{OH} = –24mA		3.86	3.76	
		5.5	I_{OH} = –24mA(1)		4.86	4.76	
V_{OL}	Maximum LOW Level Output Voltage	3.0	I_{OUT} = 50µA	0.002	0.1	0.1	V
		4.5		0.001	0.1	0.1	
		5.5		0.001	0.1	0.1	
		3.0	I_{OL} = 12mA		0.36	0.44	
		4.5	I_{OL} = 24mA		0.36	0.44	
		5.5	I_{OL} = 24mA(1)		0.36	0.44	
I_{IN}(3)	Maximum Input Leakage Current	5.5	V_I = V_{CC}, GND		±0.1	±1.0	µA
I_{OLD}	Minimum Dynamic Output Current(2)	5.5	V_{OLD} = 1.65V Max.			75	mA
I_{OHD}		5.5	V_{OHD} = 3.85V Min.			–75	mA
I_{CC}(3)	Maximum Quiescent Supply Current	5.5	V_{IN} = V_{CC} or GND		4.0	40.0	µA
I_{OZ}	Maximum 3-STATE Leakage Current	5.5	V_I (OE) = V_{IL}, V_{IH}; V_I = V_{CC}, GND; V_O = V_{CC}, GND		±0.25	±2.5	µA
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	5.0	Figures 1 & 2(4)	1.1	1.5		V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	5.0	Figures 1 & 2(4)	–0.6	–1.2		V
V_{IHD}	Minimum HIGH Level Dynamic Input Voltage	5.0	(5)	3.1	3.5		V
V_{ILD}	Maximum LOW Level Dynamic Input Voltage	5.0	(5)	1.9	1.5		V

Notes:

1. All outputs loaded; thresholds on input associated with output under test.
2. Maximum test duration 2.0ms, one output loaded at a time.
3. I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
4. Max number of outputs defined as (n). Data inputs are driven 0V to 5V. One output @ GND.
5. Max number of data inputs (n) switching. (n–1) inputs switching 0V to 5V (ACQ). Input-under-test switching: 5V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1MHz.

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DC Electrical Characteristics for ACTQ

Symbol	Parameter	V_{CC} (V)	Conditions	T_A = +25°C	T_A = –40°C to +85°C		Units
				Typ.	Guaranteed Limits		
V_{IH}	Minimum HIGH Level Input Voltage	4.5	V_{OUT} = 0.1V or V_{CC} – 0.1V	1.5	2.0	2.0	V
		5.5		1.5	2.0	2.0	
V_{IL}	Maximum LOW Level Input Voltage	4.5	V_{OUT} = 0.1V or V_{CC} – 0.1V	1.5	0.8	0.8	V
		5.5		1.5	0.8	0.8	
V_{OH}	Minimum HIGH Level Output Voltage	4.5	I_{OUT} = –50µA	4.49	4.4	4.4	V
		5.5		5.49	5.4	5.4	
		4.5	V_{IN} = V_{IL} or V_{IH}: I_{OH} = –24mA		3.86	3.76	V
		5.5	I_{OH} = –24mA[6]		4.86	4.76	
V_{OL}	Maximum LOW Level Output Voltage	4.5	I_{OUT} = 50µA	0.001	0.1	0.1	V
		5.5		0.001	0.1	0.1	
		4.5	V_{IN} = V_{IL} or V_{IH}: I_{OL} = 24mA		0.36	0.44	
		5.5	I_{OL} = 24mA[6]		0.36	0.44	
I_{IN}[3]	Maximum Input Leakage Current	5.5	V_I = V_{CC}, GND		±0.1	±1.0	µA
I_{OZ}	Maximum 3-STATE Current	5.5	V_I = V_{IL}, V_{IH}; V_O = V_{CC}, GND		±0.25	±2.5	µA
I_{CCT}	Maximum I_{CC}/Input[3]	5.5	V_I = V_{CC} – 2.1V	0.6		1.5	mA
I_{OLD}	Minimum Dynamic Output Current[6]	5.5	V_{OLD} = 1.65V Max.			75	mA
I_{OHD}			V_{OHD} = 3.85V Min.			–75	mA
I_{CC}[3]	Maximum Quiescent Supply Current	5.5	V_{IN} = V_{CC} or GND		4.0	40.0	µA
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	5.0	Figures 1 & 2[8]	1.1	1.5		V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	5.0	Figures 1 & 2[8]	–0.6	–1.2		V
V_{IHD}	Minimum HIGH Level Dynamic Input Voltage	5.0	[9]	1.9	2.2		V
V_{ILD}	Maximum LOW Level Dynamic Input Voltage	5.0	[9]	1.2	0.8		V

Notes:

6. All outputs loaded; thresholds on input associated with output under test.
7. Maximum test duration 2.0ms, one output loaded at a time.
8. Max number of outputs defined as (n). Data inputs are driven 0V to 3V. One output @ GND
9. Max number of data inputs (n) switching. (n–1) inputs switching 0V to 3V (ACTQ). Input-under-test switching: 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1MHz.

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AC Electrical Characteristics for ACQ

Symbol	Parameter	V_{CC} (V)[10]	T_A = +25°C, C_L = 50pF			T_A = –40°C to +85°C, C_L = 50pF		Units
			Min.	Typ.	Max.	Min.	Max.	
f_{MAX}	Maximum Clock Frequency	3.3	75			70		MHz
		5.0	90			85		
t_{PLH}, t_{PHL}	Propagation Delay, CP to O_n	3.3	3.0	9.5	13.0	3.0	13.5	ns
		5.0	2.0	6.5	8.5	2.0	9.0	
t_{PZL}, t_{PZH}	Output Enable Time	3.3	3.0	9.5	13.0	3.0	13.5	ns
		5.0	2.0	6.5	8.5	2.0	9.0	
t_{PHZ}, t_{PLZ}	Output Disable Time	3.3	1.0	9.5	14.5	1.0	15.0	ns
		5.0	1.0	8.0	9.5	1.0	10.0	
t_{OSHL}, t_{OSLH}	Output to Output Skew, CP to O_n[11]	3.3		1.0	1.5		1.5	ns
		5.0		0.5	1.0		1.0	

Notes:

10. Voltage range 5.0 is 5.0V ± 0.5V. Voltage range 3.3 is 3.3V ± 0.3V.

11. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}). Parameter guaranteed by design.

AC Operating Requirements for ACQ

Symbol	Parameter	V_{CC} (V)[12]	T_A = +25°C, C_L = 50pF	T_A = –40°C to +85°C, C_L = 50pF		Units
			Typ.	Guaranteed Minimum		
t_S	Setup Time, HIGH or LOW, D_n to CP	3.3	0	3.0	3.0	ns
		5.0	0	3.0	3.0	
t_H	Hold Time, HIGH or LOW, D_n to CP	3.3	0	1.5	1.5	ns
		5.0	2.0	1.5	1.5	
t_W	CP Pulse Width, HIGH or LOW	3.3	2.0	4.0	4.0	ns
		5.0	2.0	4.0	4.0	

Note:

12. Voltage range 5.0 is 5.0V ± 0.5V. Voltage range 3.3 is 3.3V ± 0.3V

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AC Electrical Characteristics for ACTQ

Symbol	Parameter	V_{CC} (V)[13]	T_A = +25°C, C_L = 50pF			T_A = –40°C to +85°C, C_L = 50pF		Units
			Min.	Typ.	Max.	Min.	Max.	
f_{MAX}	Maximum Clock Frequency	5.0	85			80		MHz
t_{PLH}, t_{PHL}	Propagation Delay, CP to O_n	5.0	2.0	7.0	9.0	2.0	9.5	ns
t_{PZL}, t_{PZH}	Output Enable Time	5.0	2.0	7.5	9.0	2.0	9.5	ns
t_{PHZ}, t_{PLZ}	Output Disable Time	5.0	1.0	8.0	10.0	1.0	10.5	ns
t_{OSHL}, t_{OSLH}	Output to Output Skew, CP to O_n[14]	5.0		0.5	1.0		1.0	ns

Notes:

13. Voltage range 5.0 is 5.0V ± 0.5V.

14. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}). Parameter guaranteed by design.

AC Operating Requirements for ACTQ

Symbol	Parameter	V_{CC} (V)[15]	T_A = +25°C, C_L = 50pF	T_A = –40°C to +85°C, C_L = 50pF		Units
			Typ.	Guaranteed Minimum		
t_S	Setup Time, HIGH or LOW, D_n to CP	5.0	0	3.0	3.0	ns
t_H	Hold Time, HIGH or LOW, D_n to CP	5.0	0	1.5	1.5	ns
t_H	CP Pulse Width, HIGH or LOW	5.0	2.0	4.0	4.0	ns

Note:

15. Voltage range 5.0 is 5.0V ± 0.5V

Capacitance

Symbol	Parameter	Conditions	Typ.	Units
C_{IN}	Input Capacitance	V_{CC} = OPEN	4.5	pF
C_{PD}	Power Dissipation Capacitance	V_{CC} = 5.0V	42.0	pF

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FACT Noise Characteristics

The setup of a noise characteristics measurement is critical to the accuracy and repeatability of the tests. The following is a brief description of the setup used to measure the noise characteristics of FACT.

Equipment:

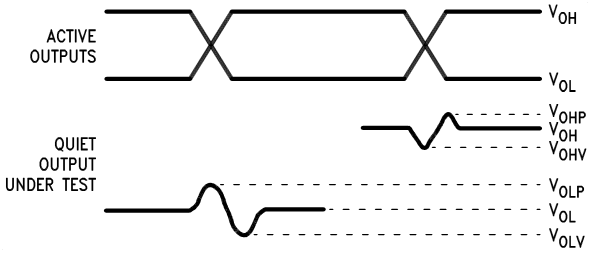
Hewlett Packard Model 8180A Word Generator

PC-163A Test Fixture

Tektronics Model 7854 Oscilloscope

Procedure:

1. Verify Test Fixture Loading: Standard Load 50pF, 500Ω.
2. Deskew the HFS generator so that no two channels have greater than 150ps skew between them. This requires that the oscilloscope be deskewed first. It is important to deskew the HFS generator channels before testing. This will ensure that the outputs switch simultaneously.
3. Terminate all inputs and outputs to ensure proper loading of the outputs and that the input levels are at the correct voltage.
4. Set the HFS generator to toggle all but one output at a frequency of 1MHz. Greater frequencies will increase DUT heating and effect the results of the measurement.
5. Set the HFS generator input levels at 0V LOW and 3V HIGH for ACT devices and 0V LOW and 5V HIGH for AC devices. Verify levels with an oscilloscope.



Notes:

16. V_{OHV} and V_{OLP} are measured with respect to ground reference.
17. Input pulses have the following characteristics: f = 1MHz, t_r = 3ns, t_f = 3ns, skew < 150ps.

Figure 1. Quiet Output Noise Voltage Waveforms

V_{OLP}/V_{OLV} and V_{OHP}/V_{OHV}:

- Determine the quiet output pin that demonstrates the greatest noise levels. The worst case pin will usually be the furthest from the ground pin. Monitor the output voltages using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- Measure V_{OLP} and V_{OLV} on the quiet output during the worst case transition for active and enable. Measure V_{OHP} and V_{OHV} on the quiet output during the worst case active and enable transition.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

V_{ILD} and V_{IHD}:

- Monitor one of the switching outputs using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- First increase the input LOW voltage level, V_{IL}, until the output begins to oscillate or steps out a min of 2ns. Oscillation is defined as noise on the output LOW level that exceeds V_{IL} limits, or on output HIGH levels that exceed V_{IH} limits. The input LOW voltage level at which oscillation occurs is defined as V_{ILD}.
- Next decrease the input HIGH voltage level, V_{IH}, until the output begins to oscillate or steps out a min of 2ns. Oscillation is defined as noise on the output LOW level that exceeds V_{IL} limits, or on output HIGH levels that exceed V_{IH} limits. The input HIGH voltage level at which oscillation occurs is defined as V_{IHD}.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

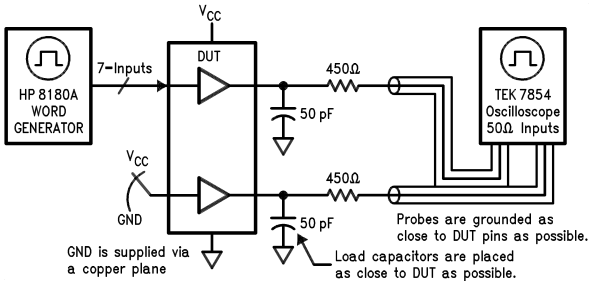


Figure 2. Simultaneous Switching Test Circuit

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Physical Dimensions

Dimensions are in inches (millimeters) unless otherwise noted.

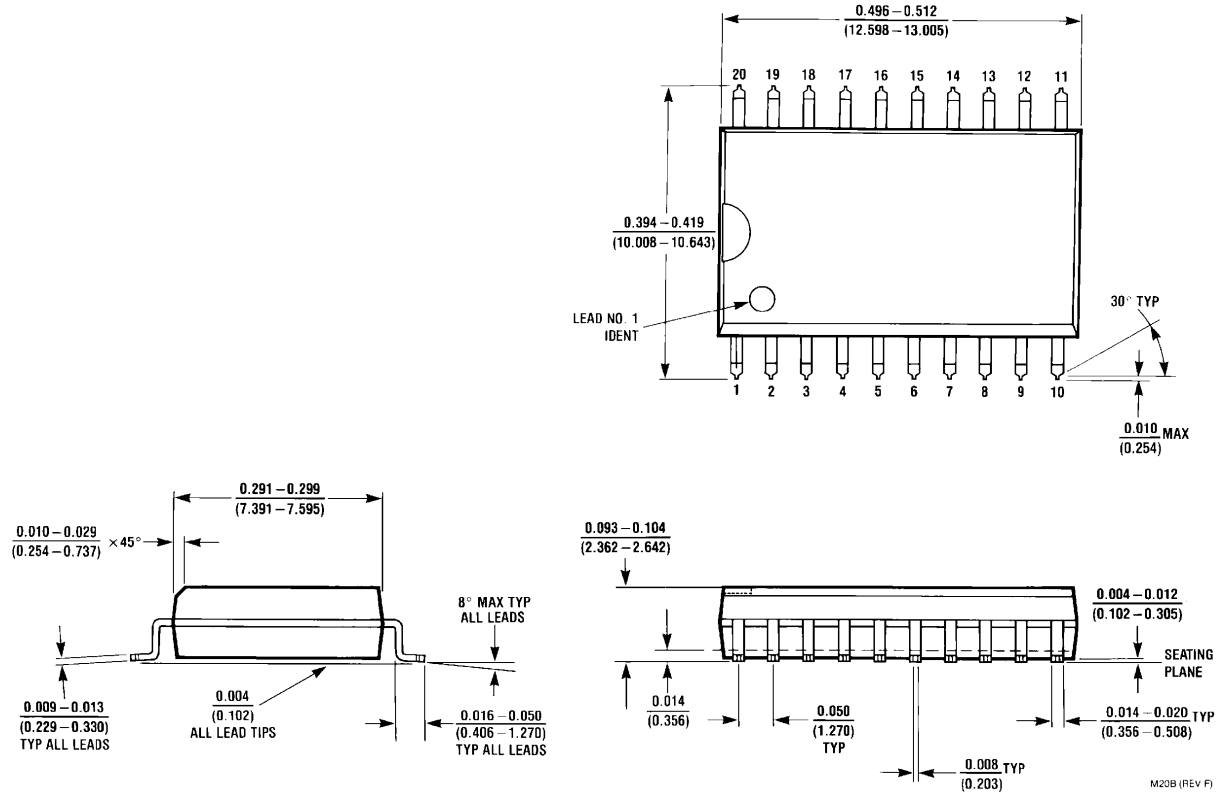

Figure 3. 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M20B

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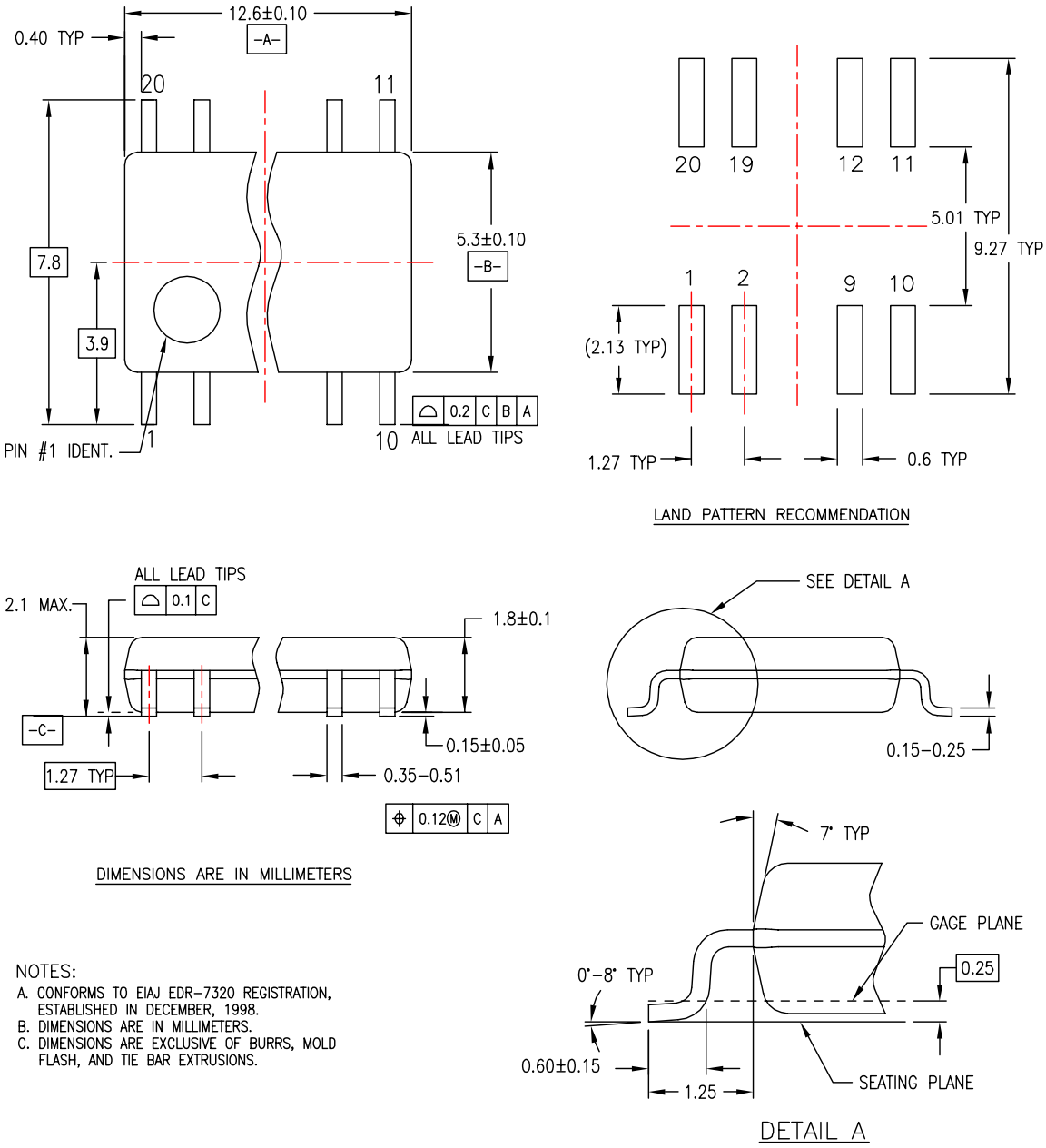
Physical Dimensions (Continued)

Dimensions are in millimeters unless otherwise noted.



NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DREVC

Figure 4. 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M20D

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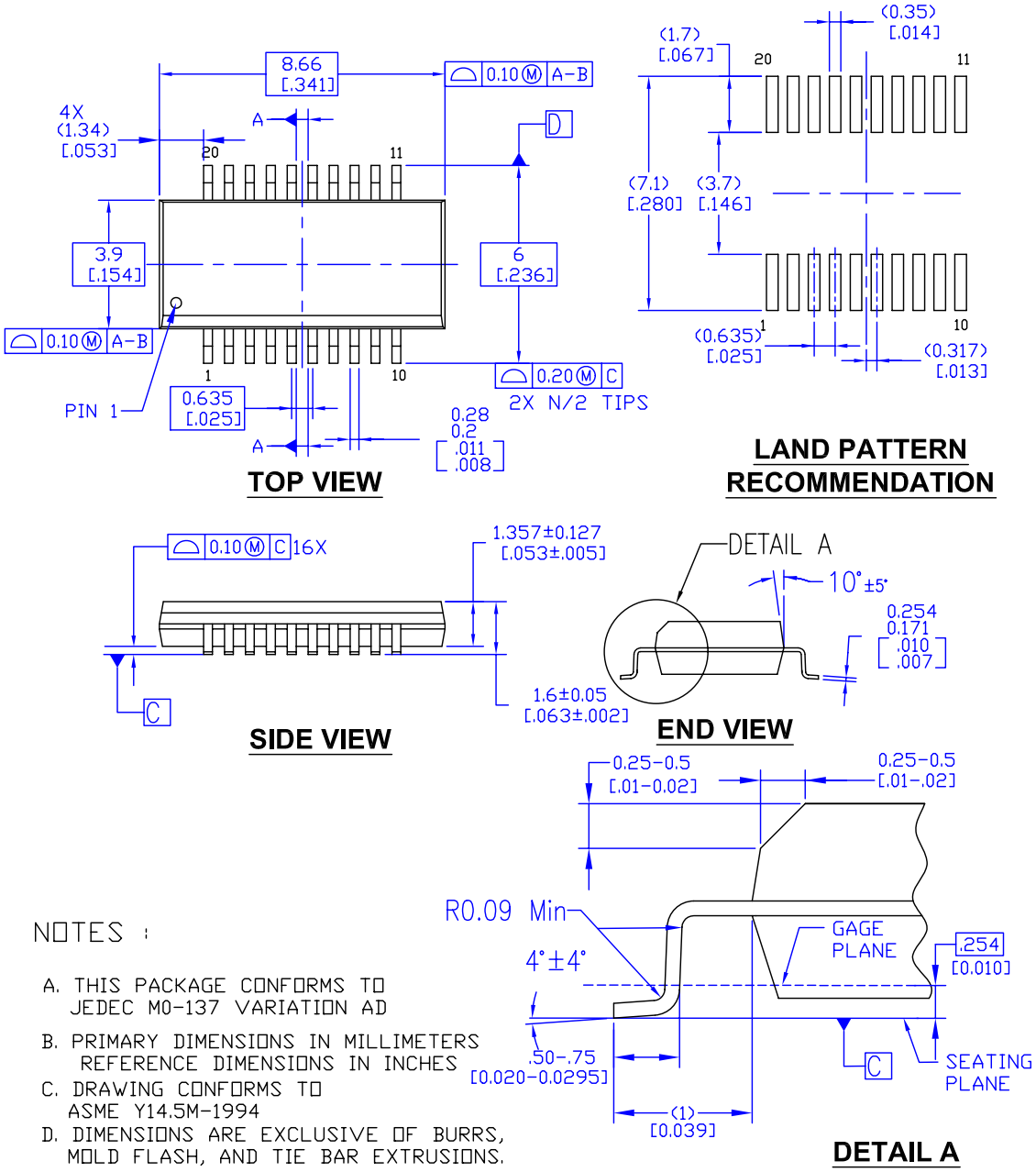
Physical Dimensions (Continued)

Dimensions are in millimeters unless otherwise noted.



NOTES :

A. THIS PACKAGE CONFORMS TO JEDEC MO-137 VARIATION AD

B. PRIMARY DIMENSIONS IN MILLIMETERS REFERENCE DIMENSIONS IN INCHES

C. DRAWING CONFORMS TO ASME Y14.5M-1994

D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

MQA20REVA

Figure 5. 20-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150" Wide
Package Number MQA20

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