

MT29F128G08AMCDBJ5-6

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MT29F128G08AMCDBJ5-6:D

Orderable Part Information

Status	Production	Alternative Part	N/A
FBGA Code	NW609	SPD Data	N/A
MBQual Data	N/A	Shipping Media	N/A
PLP	No	Start Date	N/A

Specs

Density	128Gb	Status	Production
RoHS	Yes	Width	x8
Voltage	3.3V	Package	TBGA
Pin Count	132-ball	MT/s	333 MT/s
I/O	Common		

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Date	What was added
07/2014	DSV: MT29FJ32_64_128_256]G SLC DSV
01/2014	IBIS: 32Gb 64Gb 128Gb 256Gb Async Sync NAND

FAQs

- » Do you support small block devices?
- » How much ECC do I need to support your devices?
- » I am using the correct amount of error correction code (ECC) for the NAND device, but I'm still seeing bitbyte errors in data I read back from the NAND device.
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Sim Models & Software

Title & Description	Secure	ID	Updated
HSpice: 32Gb 64Gb 128Gb 256Gb Async Sync NAND: Rev 2.0		M83C	01/2014
IBIS: 32Gb 64Gb 128Gb 256Gb Async Sync NAND: Rev 2.0		M83C	01/2014

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- [+](#) Do you support small block devices?
- [+](#) How much ECC do I need to support your devices?
- [+](#) I am using the correct amount of error correction code (ECC) for the NAND device, but I'm still seeing bitbyte errors in data I read back from the NAND device.

- [+](#) How do I achieve greater PROGRAM/READ throughput for the NAND device?
- [+](#) How is Nvb specified?
- [+](#) I am seeing a lot of READ DISTURB errors. Can you tell me if there is a problem with your part?
- [+](#) I've heard that NAND has too many errors to boot from. Is this true?
- [+](#) Should I be marking blocks bad due to READ errors?
- [+](#) When I issue a Read ID command (90h) to a two-die NAND device, I get a device ID back that states it is a one-die NAND device.
- [+](#) Where can I find additional technical information about Micron NAND devices that is not covered in the device data sheets?
- [+](#) Where can I find simulation models for NAND Flash devices?
- [+](#) Why am I getting a bitbyte error reading back the information I programmed into the NAND device?
- [+](#) Why doesn't the NAND Flash device respond correctly to commands issued to it?
- [+](#) What is a "bank"?
- [+](#) What is the impedance tolerance of the driver in match-impedance mode relative to the expected value base on the perfect reference resistor connected to ZQ pin?
- [+](#) Does thermal information change for IT parts?
- [+](#) My design was based on a specification stating the JTAG was relative to VDD (1.8V), but now we've discovered that JTAG is actually relative to VDDQ (1.5V). It's a fairly significant board spin to change this; what do I risk by leaving the design as-is? I assume that the specification is still for VDDQ + 0.3V = 1.8V, but with CMOS parts there's no way I can guarantee that it won't assume past that on transitions.
- [+](#) Should the ECC memory chip share chip select and CKE signals with the other two main memory chips in our point-to-point application?

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