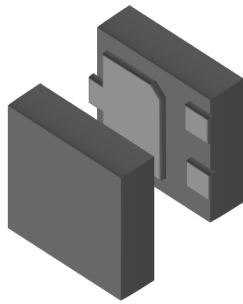
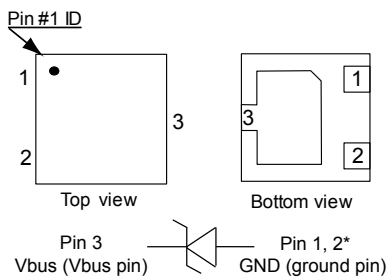


High power transient voltage suppressor



QFN package



*Pin 1 and Pin 2 must be connected together.

Product status link

[ESDA24P140-1U3M](#)

Features

- Low clamping voltage
- Peak pulse power:
 - 4500 W (8/20 μ s)
- Stand off voltage 22 V
- Unidirectional diode
- Low leakage current:
 - 0.20 μ A at 25°C
- Complies with the following standards: IEC 61000-4-2 level 4
 - \pm 30 kV (air discharge)
 - \pm 30 kV (contact discharge)

Application

Where transient over voltage protection in ESD sensitive equipment is required, such as:

- Smartphones, mobile phones, tablets, portable multimedia
- USB V_{bus} protection
- Power supply protection
- Battery protection

Description

The ESDA24P140-1U3M is a unidirectional single line TVS diode designed to protect the power line against EOS & ESD transients.

The device is ideal for applications where high power TVS and board space saving is required.

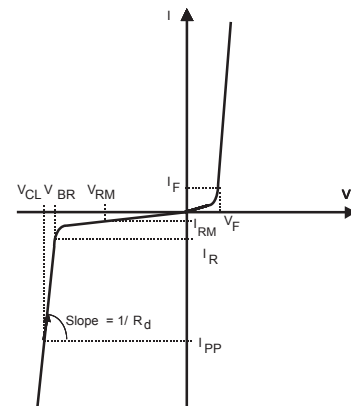
1 Characteristics

Table 1. Absolute maximum ratings ($T_{amb} = 25\text{ }^{\circ}\text{C}$)

| Symbol | Parameter | | Value | Unit |
|-----------|---|---------------------------------|------------|--------------------|
| V_{pp} | Peak pulse voltage | IEC 61000-4-2 contact discharge | >30 | kV |
| | | IEC 61000-4-2 air discharge | >30 | |
| P_{pp} | Peak pulse power (8/20 μs) | | 4500 | W |
| I_{pp} | Peak pulse current (8/20 μs) | | 140 | A |
| P_{pp} | Peak pulse power (10/1000 μs) | | 330 | W |
| I_{pp} | Peak pulse current (10/1000 μs) | | 10 | A |
| T_{op} | Operating junction temperature range | | -55 to 150 | $^{\circ}\text{C}$ |
| T_{stg} | Storage junction temperature range | | -55 to 150 | $^{\circ}\text{C}$ |

Figure 1. Electrical characteristics (definitions)

| | | |
|----------|---|----------------------------|
| Symbol | = | Parameter |
| V_{BR} | = | Breakdown voltage |
| V_{CL} | = | Clamping voltage |
| I_{RM} | = | Leakage current @ V_{RM} |
| V_{RM} | = | Stand-off voltage |
| I_{PP} | = | Peak pulse current |
| R_D | = | Dynamic resistance |
| I_R | = | Breakdown current |
| V_F | = | Forward voltage |
| I_F | = | Forward current |


Table 2. Electrical characteristics (values) ($T_{amb} = 25\text{ }^{\circ}\text{C}$)

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|----------|--|------|------|------|----------|
| V_{RM} | | | | 22 | V |
| V_{BR} | $I_R = 1\text{ mA}$ | 22.7 | 24 | 25.2 | V |
| I_{RM} | $V_{RM} = 22\text{ V}$ | | | 200 | nA |
| V_{CL} | $I_{PP} = 100\text{ A } 8/20\mu\text{s}$ | | 30 | 34 | V |
| | $I_{PP} = 140\text{ A } 8/20\mu\text{s}$ | | 33.6 | 38 | |
| R_D | 8/20 μs | | 0.07 | | Ω |
| V_{CL} | $I_{PP} = 10\text{ A } 10/1000\ \mu\text{s}$ | | 29.5 | 33 | V |
| R_D | 10/1000 μs | | 0.5 | | Ω |
| V_F | $I_F = 10\text{ mA}$ | | 0.7 | | V |

1.1 Characteristics (curves)

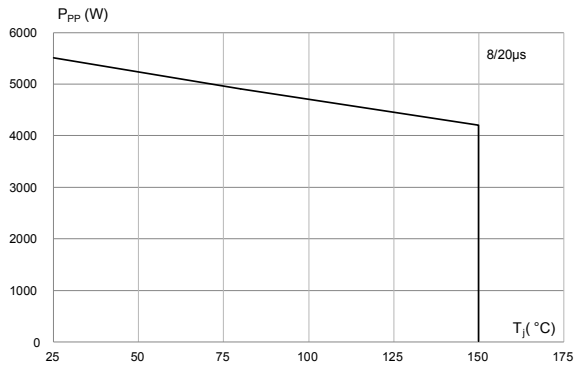
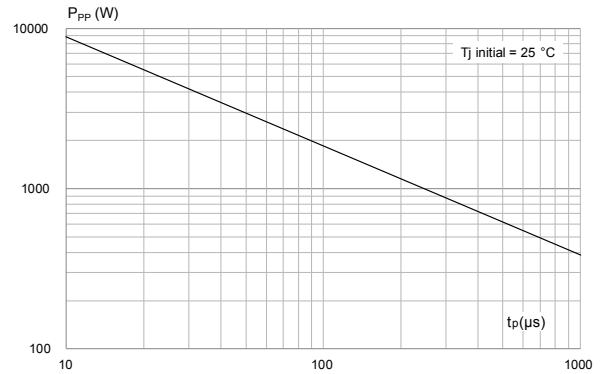
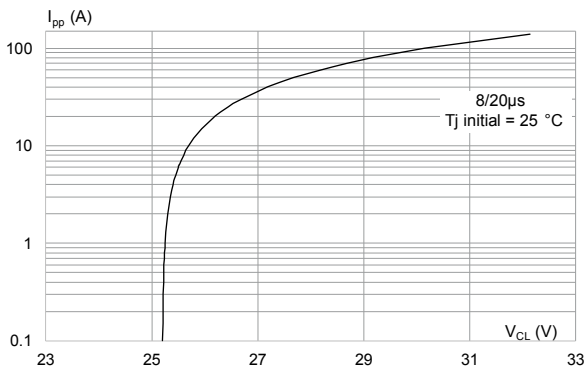
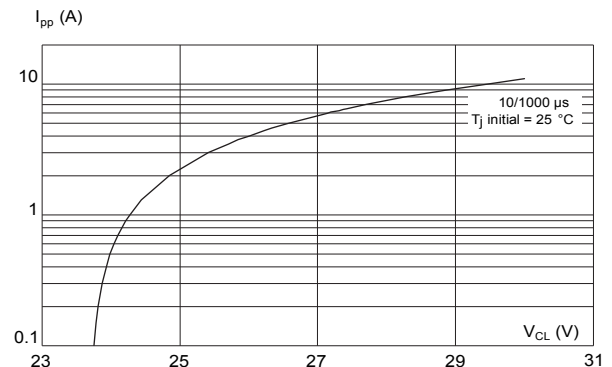
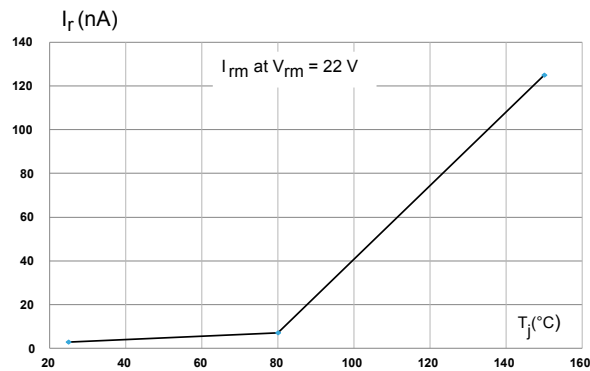
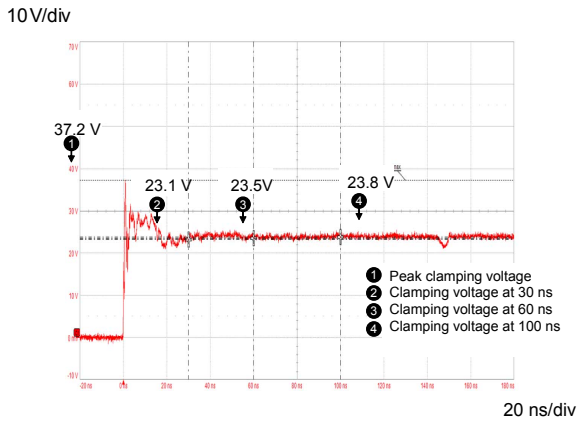
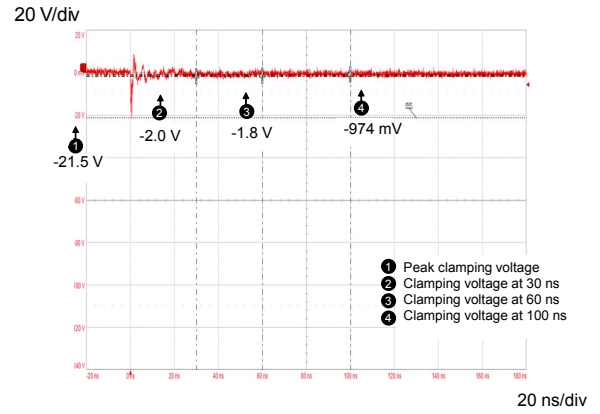
Figure 2. Peak pulse power dissipation versus initial temperature (typical value)

Figure 3. Peak pulse power versus exponential pulse duration (typical value)

Figure 4. Peak pulse current versus clamping voltage (max value, 8/20 µs)

Figure 5. Peak pulse current versus clamping voltage (max value, 10/1000 µs)

Figure 6. Leakage current versus junction temperature (typical value)


Figure 7. ESD response to IEC 61000-4-2 (+8 kV contact discharge)

Figure 8. ESD response to IEC 61000-4-2 (-8 kV contact discharge)


2 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

2.1 QFN package information

Figure 9. QFN package outline

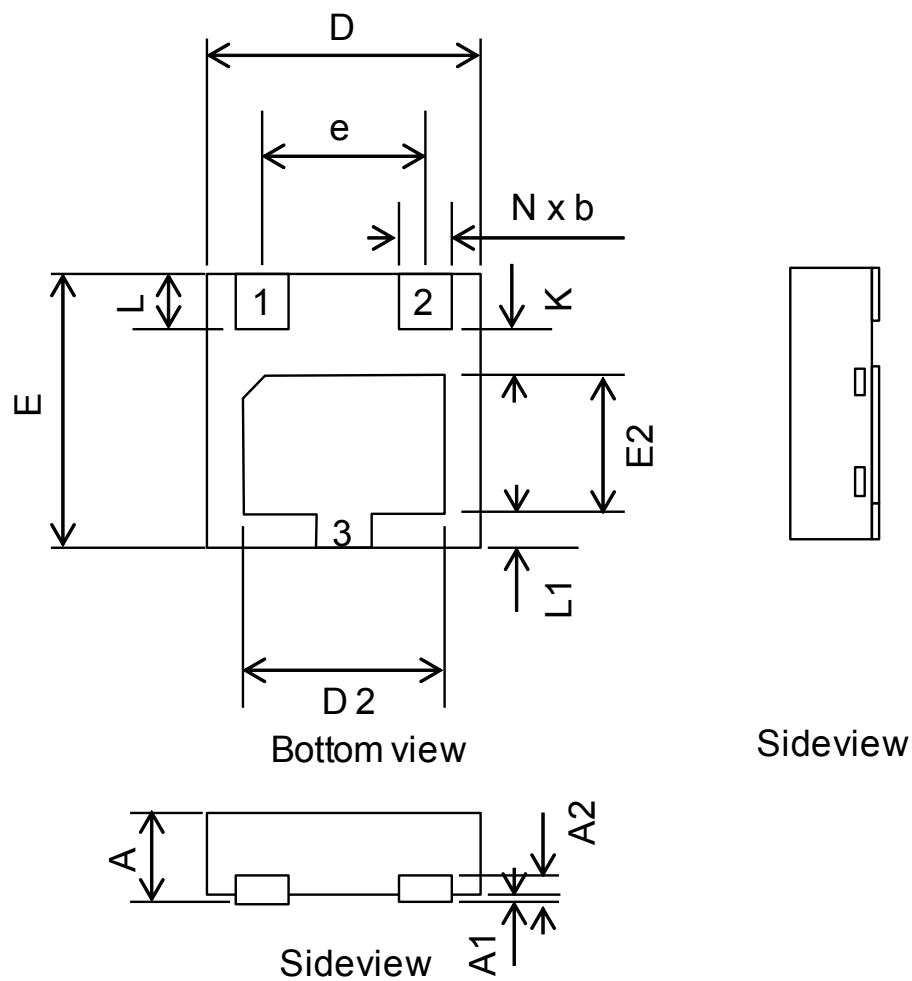


Table 3. QFN package mechanical data

| Ref. | Dimensions | | |
|------|-------------|------|------|
| | Millimeters | | |
| | Min. | Typ. | Max. |
| A | 0.51 | 0.55 | 0.60 |
| A1 | 0.00 | 0.02 | 0.05 |
| A2 | | 0.15 | |
| b | 0.25 | 0.30 | 0.35 |
| D | | 2.00 | |
| E | | 2.00 | |
| e | | 1.30 | |
| D2 | 1.40 | 1.50 | 1.60 |
| E2 | 0.90 | 1.00 | 1.10 |
| K | 0.20 | | |
| L1 | | 0.25 | |
| L | 0.35 | 0.40 | 0.45 |
| N | | 3 | |

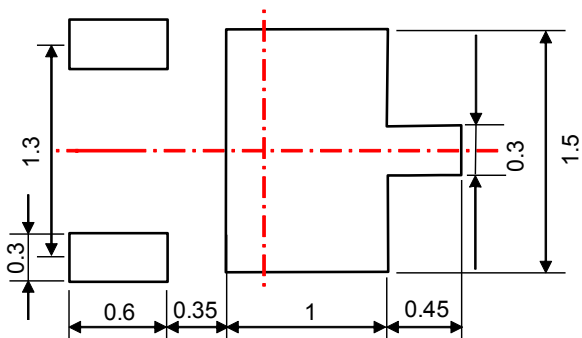
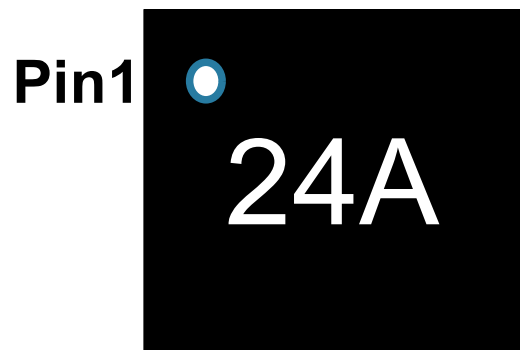
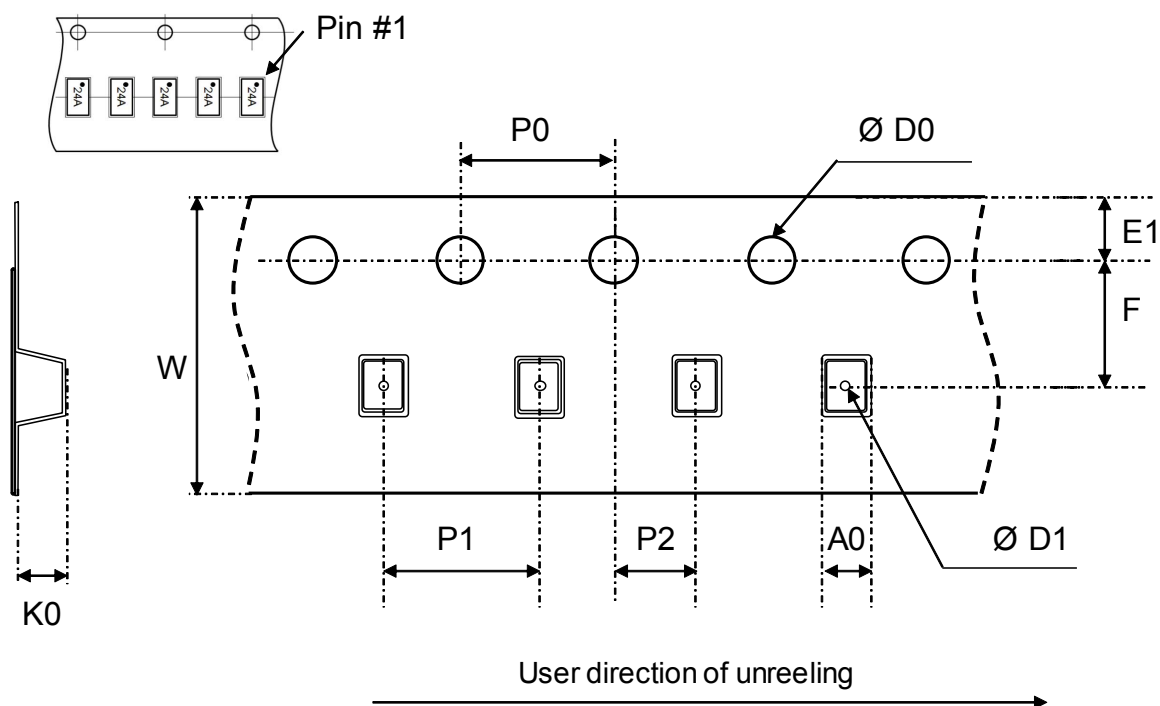
Figure 10. Recommended footprint in mm

Figure 11. Marking


Figure 12. Tape outline


Note: Pocket dimensions are not on scale
 Pocket shape may vary depending on package

Table 4. Tape and reel dimensions

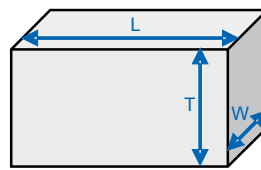
| Ref. | Dimensions (millimeters) | | |
|------|--------------------------|------|------|
| | Millimeters | | |
| | Min. | Typ. | Max. |
| P1 | 3.90 | 4.00 | 4.10 |
| P0 | 3.90 | 4.00 | 4.10 |
| Ø D0 | 1.50 | 1.55 | 1.60 |
| Ø D1 | 1.00 | | |
| F | 3.40 | 3.50 | 3.60 |
| E1 | 1.65 | 1.75 | 1.85 |
| K0 | 0.65 | 0.75 | 0.85 |
| P2 | 1.95 | 2.00 | 2.05 |
| W | 7.70 | 8.00 | 8.30 |
| A0 | 2.15 | 2.25 | 2.35 |

3 Recommendation on PCB assembly

3.1 Stencil opening design

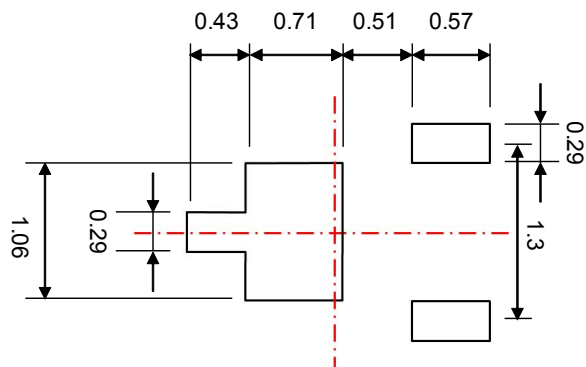
1. General recommendation on stencil opening design
 - a. Stencil opening dimensions: L (Length), W (Width), T (Thickness).

Figure 13. Stencil opening recommendation



- b. General design rule
 - Stencil thickness (T) = 75 ~ 125 μm
 - $\frac{W}{T} \geq 1.5$
 - $\frac{L \times W}{2T(L + W)} \geq 0.66$
1. Reference design
 - a. Stencil opening thickness: 100 μm
 - b. Stencil opening for leads: Opening to footprint ratio is 90%
 - c. Stencil opening for expose pad: Opening to footprint ratio is 50%

Figure 14. Recommended stencil window position in mm



3.2 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste is recommended.
3. Offers a high tack force to resist component movement during high speed.
4. Use solder paste with fine particles: powder particle size 20-45 μm .

3.3 Placement

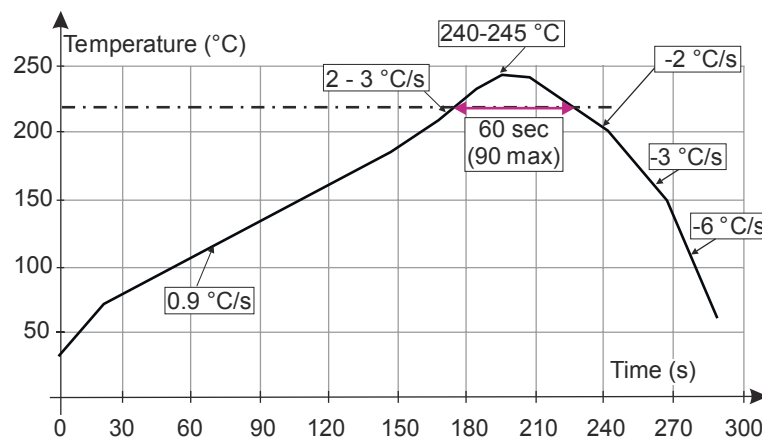
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering
3. Standard tolerance of ± 0.05 mm is recommended.
4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

3.4 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. A symmetrical layout is recommended, to avoid any tilt phenomena caused by asymmetrical solder paste due to solder flow away.

3.5 Reflow profile

Figure 15. ST ECOPACK[®] recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement.

4 Ordering information

Figure 16. Ordering information scheme

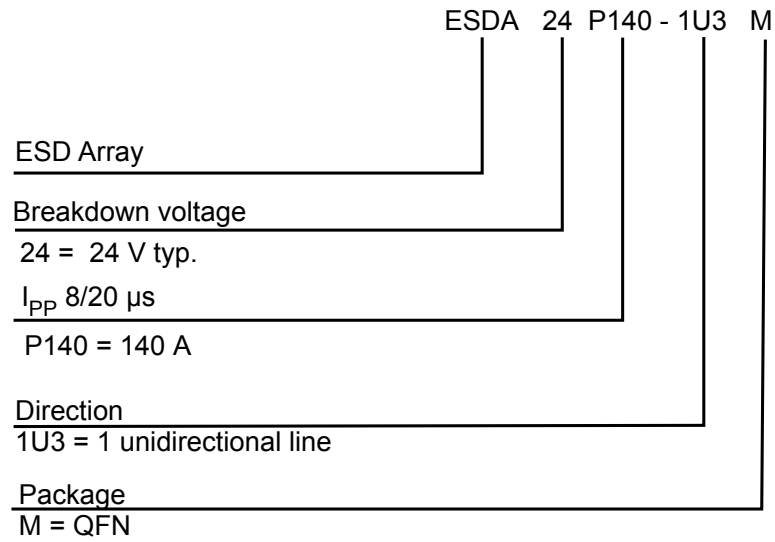


Table 5. Ordering information

| Order code | Marking | Weight | Base qty. | Delivery mode |
|-----------------|---------|--------|-----------|---------------|
| ESDA24P140-1U3M | 24A | 7 mg | 5000 | Tape and reel |

1. The marking can be rotated by multiples of 90° to differentiate assembly location.

Revision history

Table 6. Document revision history

| Date | Revision | Changes |
|-------------|----------|--------------|
| 22-May-2018 | 1 | First issue. |

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